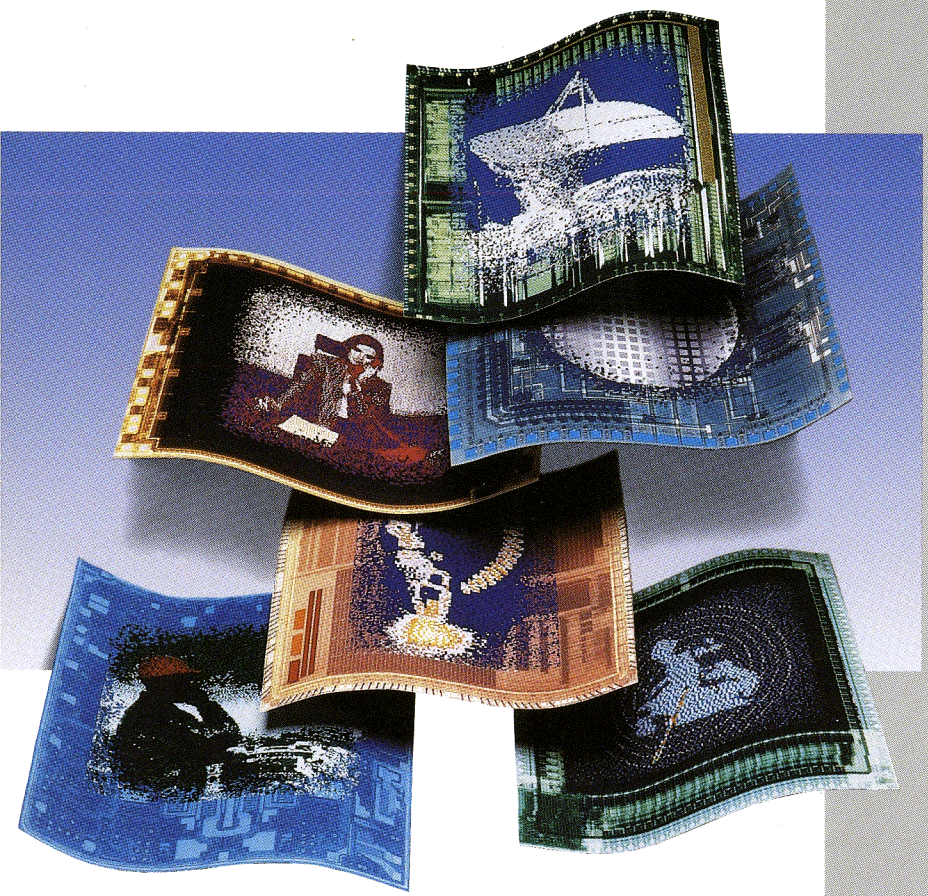
Telecoms

IC Handbook

October 1991



GEC PLESSEY

SEMICONDUCTORS

TELECOMS

IC Handbook

GEC PLESSEY

SEMICONDUCTORS

Foreword

GEC Plessey Semiconductors is committed to the development of highly sophisticated and innovative products for the Telecommunications Industry.

Technical experience and close links with major equipment manufacturers have resulted in a wide range of IC products ideally suited to all aspects of telecommunications equipment, from Central Office and PBX to Subscriber.

Dedication to customer needs is demonstrated by a wide range of high voltage bipolar SLIC (Subscriber Line Interface Circuit) devices, designed to cater for a variety of line lengths and conditions.

To complement the SLICs, the low voltage CMOS MV3010 SLAC (Subscriber Line Audio Circuit) brings the accuracy and repeatability of DSP (Digital Signal Processing) to the traditionally analog line card. Significant benefits of the DSP approach include a greater degree of flexibility and the ability to adapt automatically to different line conditions. The rigorously tested and completely robust echo cancellation algorithm ensures dynamically that optimum Echo Return Loss is achieved over a wide range of line lengths and terminating impedances. The GPS combination of SLICs and SLAC is believed to offer the ultimate high performance, cost effective, line card solution.

In addition to innovative new products, GPS offers a comprehensive range of industry standard devices, including Pulse, DTMF and switchable Pulse/DTMF Diallers (approved in most European countries), Codecs, Digital Switch Modules and PCM circuits (up to 34Mbits) with a custom design option – all backed up by a dedicated customer support team.

GPS is continually assessing the needs of equipment manufacturers and is actively engaged in carrying out an expansion of its range of products for the future needs of the Telecommunications Industry.

Personal Communications

GEC Plessey Semiconductors has also created a range of products specific to applications in the growing markets for radio- communications equipment (such as CT2, DECT, GSM and radiopagers). Technical details for these devices can be found in the Personal Communications IC Handbook.

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Section 1
Telephone Circuits

Pulse, DTMF and Dual Mode Dialler ICs - Selection Guide

The GEC Plessey Semiconductors range of diallers is the most comprehensive available, comprising Pulse, DTMF and switchable Pulse/DTMF devices.

The majority of switchable dual-mode Pulse/DTMF diallers are part of a pin-compatible family – allowing a single circuit and PCB design to provide a range of telephones simply by exchanging chips. An extensive selection of mask-programmable options allows each device to offer different dialling parameters, keypad options and protocols for various countries while different output polarities and configurations allow optimisation of telephone design for minimum component cost.

GPS dialler chips are comprehensively tested and quality controlled during manufacture and are used in telephones approved by most European PTTs. All are available in DIL and surface mount miniature DIL packages.

Type number	Dialling mode	Last number redial	Memories	Dedicated memory keys	Member of pin-compatible family	Selectable break/make and IDP options	Timed flash options 100-600ms	Extensive metal mask options	Internal on-hook timeout	Page
MV4320	Pulse	√				√				1-3
MV5087	DTMF									1-7
MV5089	DTMF									1-12
MA535	DTMF	√					√	√	√	1-17
MA526[1]	Pulse/DTMF	√			√	√	√	√	√	-
MA527[2]	↓	√	10		√	√	√	√	√	-
MA541		√			√	√	√	√	√	1-23
MA545		√	10	√	√	√	√	√	√	1-31
MA547		√	10		√	√	√	√	√	1-38
MA585		√	20	√[3]	√	√	√	√	√	1-45
MA587		√	20	√	√	√	√	√	√	1-52
MA589		√	20		√	√	√	√	√	1-59
MA552		√				√	√	√	√	1-67
MA525	↓	√	Fully micro controlled, all parameters programmable						√	1-76

NOTES: 1. Use MA541 for new designs. 2. Use MA545 for new designs. 3. For 10 memories. 4. All MA5xx devices use an inexpensive 560kHz ceramic resonator.

DS3124-1.0

MV4320

KEYPAD PULSE DIALLER

The MV4320 is fabricated using ISO-CMOS high density technology. The device is a pin-for-pin replacement for the DF320 Loop Disconnect Dialler and offers wider operating supply voltage range and lower power dissipation. The MV4320 accepts up to 20 digits from a standard 2 of 7 keypad and has a REDIAL option which is activated by the # key. The device provides dial pulsing and muting outputs and has a HOLD pin for interrupting a dialling sequence. Outpulsing, mark/space ratio and dialling speed are pin selectable.

The MV4320 is available in Ceramic DIL (DG, −40°C to +85°C).

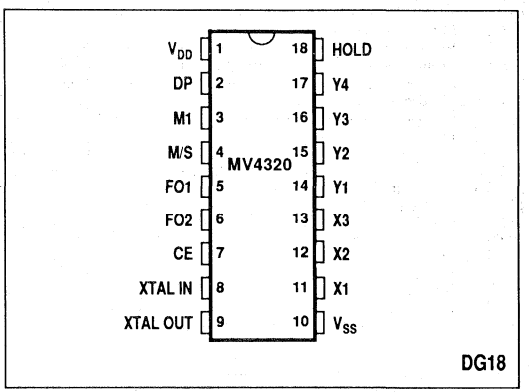


Fig.1 Pin connections - top view

FEATURES

- Pin for Pin Replacement for the DF320
- 2.5V to 5.5V Supply Voltage Operating Range
- 375μW Dynamic Power Dissipation at 3V
- Uses Inexpensive 3.58 MHz Ceramic Resonator or Crystal
- Stores up to 20 Digits
- Selectable Outpulsing Mark/Space Ratio
- Selectable Dialling Speeds of 10, 16, 20 and 932 Hz
- Low Cost

APPLICATIONS

- Pushbutton Telephones
- Tone to Pulse Converters
- Mobile Telephone
- Repertory Dialers

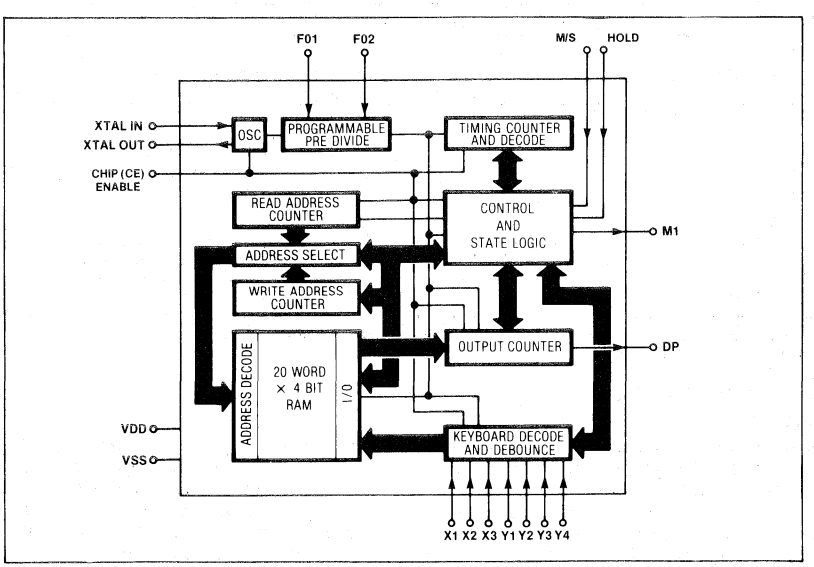


Fig.2 MV4320 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = 3.0V; T_{amb} = +25°C; f_{CLK} = 3.579545MHz
All voltages wrt V_{SS}

		CHARACTERISTICS		SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.5		5.5	V		
2		Standby Supply Current		I_{DDS}		1.0	10.0	μA	CE = V_{SS}	
3		Operating Supply Current		I_{DD}		125	200	μA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	-0.5	-3.0	-12.0	μA	$V_{IN} = V_{SS}$	X_1, X_2, X_3
5		Input Leakage Current		I_{IH}		0.1		nA	$V_{IN} = V_{DD}$	Y_1, Y_2, Y_3, Y_4
6		Input Leakage Current		I_{IL}		-0.1		nA	$V_{IN} = V_{SS}$	M/S, IDP, F01,
7		Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	12.0	μA	$V_{IN} = V_{DD}$	F02, FD, HOLD
8		Logic '0' Level		V_{IL}			0.9	V	All inputs	
9		Logic '1' Level		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	
11			High-level	V_{OH}	2.99	3		V		
12		Drive Current	N-Channel Sink	I_{OL}	0.8	2.0		mA	V_{OUT} = 2.3V	DP, M1/M2
13			P-Channel Source	I_{OH}	-0.8	-2.0		mA	V_{OUT} = 0.7V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = 3.0V; T_{amb} = +25°C; f_{CLK} = 3.579545MHz
All voltages wrt V_{SS}

		CHARACTERISTICS	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS
14	DYNAMIC	Output Rise Time	t_R		1.0		us	DP, M_1.
15		Output Fall Time	t_F		1.0		us	C_L = 50pF
16		Maximum Clock Frequency	t_{CLK}	3.58			MHz	3.579545 MHz Crystal
17		Mark to Space Ratio	M/S		2:1			Note 1
18					3:2			
19		Impulsing Rate = $\frac{1}{T}$			10		Hz	Note 1
20					16			
21					20			
22					932			
23		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE '1'
24		Input Capacitance	C_{in}		5.0		pF	Any Input

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

NOTES:
1. See Pin Function, Table 1.

OPERATING NOTES

The first key entered in any dialling sequence initiates the oscillator by internally taking CE high. Digits may be entered asynchronously from the keypad. Dialling and mute functions are output as shown in figures 3 and 4. Figure 3 shows use of the circuits with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialler circuit. In this mode, the pulse occurring on M1 when CE is taken high, with no keypad input, can be used to initiate the bistable latching relay. Figure 4 shows the timing diagram for the CE internal control mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously.

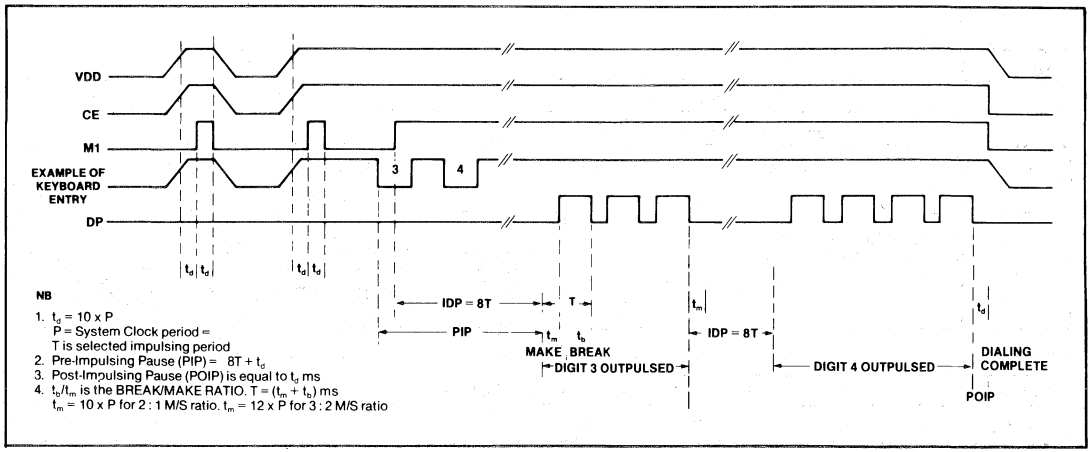


Fig.3 Keypad pulse dialer timing diagram, CE-External control

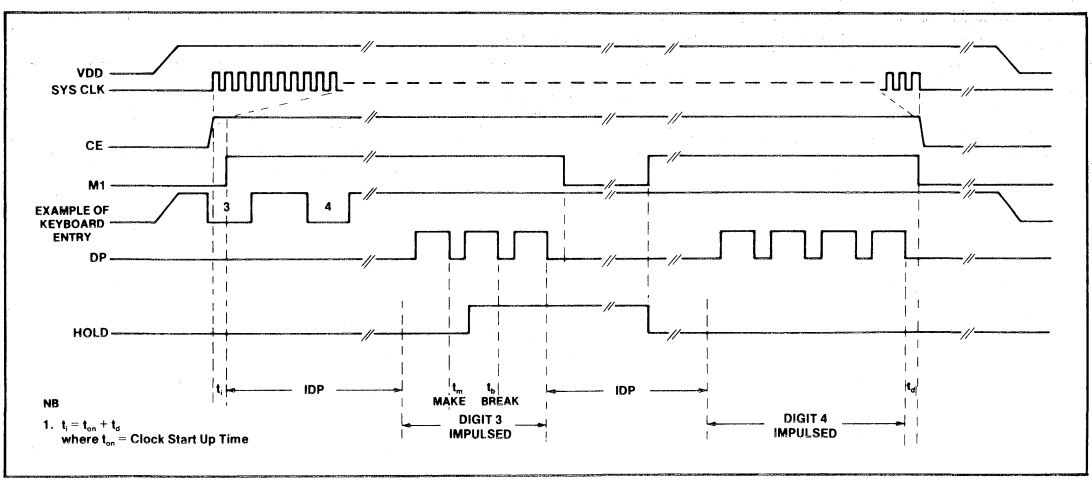


Fig.4 Keypad pulse dialer timing diagram, CE-Internal control

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

	MIN.	MAX.
V_{DD}-V_{SS}	-0.3V	10V
Voltage on any pin	V_{SS} -0.3V	V_{DD} +0.3V
Current at any pin		10mA
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C
Power Dissipation		1000mW

Derate 16mW/°C above 75°C. All leads soldered to PC board.

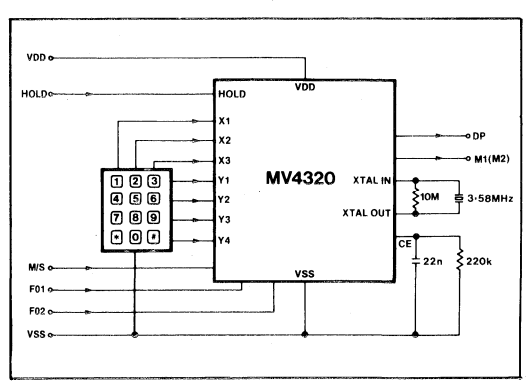


Fig.5 Application diagram

PIN FUNCTIONS

<table>
<tr><td>V_{DD}</td><td colspan="6">Positive voltage supply</td></tr>
<tr><td>DP</td><td colspan="6">Dial Pulsing Output Buffer</td></tr>
<tr><td>M1</td><td colspan="6">Mute Output (Off Normal) Buffer</td></tr>
<tr><td>M/S</td><td colspan="4">Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}.
Note: O/C = Open Circuit</td><td>O/C
V_{DD}</td><td>2:1
3:2</td></tr>
<tr><td>F01,F02</td><td colspan="6">Impulsing Rate Selection. On-chip pull-down transistor to V_{SS}.
* Assumes f_{CLK} = 3.579545MHz.
<table>
<tr><th>F01</th><th>F02</th><th>Nominal Impulsing Rate</th><th>Actual* Inpulsing Rate</th><th>System Clock frequency</th></tr>
<tr><td>O/C</td><td>O/C</td><td>10Hz</td><td>10.13Hz</td><td>303.9Hz</td></tr>
<tr><td>O/C</td><td>V_{DD}</td><td>20Hz</td><td>19.42Hz</td><td>582.6Hz</td></tr>
<tr><td>V_{DD}</td><td>O/C</td><td>932Hz</td><td>932.17Hz</td><td>27,965.1Hz</td></tr>
<tr><td>V_{DD}</td><td>V_{DD}</td><td>16Hz</td><td>15.54Hz</td><td>466.1Hz</td></tr>
</table></td></tr>
<tr><td>CE</td><td colspan="6">Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.</td></tr>
<tr><td>XTAL IN</td><td colspan="6">Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.</td></tr>
<tr><td>XTAL OUT</td><td colspan="6">Crystal Output Buffer to drive crystal.</td></tr>
<tr><td>V_{SS}</td><td colspan="6">System ground</td></tr>
<tr><td>X_1, X_2, X_3</td><td colspan="6">Column keyboard Inputs. On-chip pull-up transistors to V_{DD}.
Active LOW.</td></tr>
<tr><td>Y_1, Y_2, Y_3, Y_4</td><td colspan="6">Row keyboard Inputs. On-chip pull-up transistors to V_{DD}.
Active LOW.</td></tr>
<tr><td>HOLD</td><td colspan="6">O/C — Normal Operation
V_{DD} — No impulsing. If activated during impulsing, hold occurs when the current digit is complete
Prevents further impulsing. On-chip pull-down transistor to V_{SS}.</td></tr>
</table>

DS3125-1.0

MV5087

DTMF GENERATOR

The MV5087 is fabricated using ISO-CMOS high density technology and offers low power and wide voltage operation. An inexpensive 3.58MHz TV crystal completes the reference oscillator. From this frequency are derived 8 different sinusoidal frequencies which, when appropriately mixed, provide Dual-Tone Multi-Frequency (DTMF) tones.

Inputs are compatible with either a standard 2-of-8 or a single contact (form A) keyboard. The keyboard entries determine the correct division of the reference frequency by the row and column counters.

D-to-A conversion, using R-2R ladder networks, results in a staircase approximation of a sinewave with low total distortion.

Frequency and amplitude stability over operating voltage and temperature range are maintained within industry specifications.

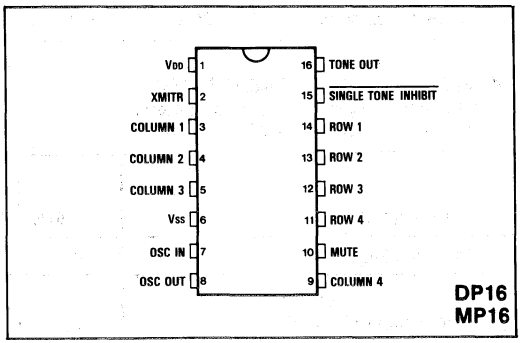


Fig.1 Pin connections - top view

FEATURES

- Pin-for-Pin Replacement for MK5087
- Low Standby Power
- Minimum External Parts Count
- 3.5V to 10V Operation
- 2-of-8 Keyboard or Calculator-Type Single Contact (Form A) Keyboard Input
- On-Chip Regulation of Output Tone
- Mute and Transmitter Drivers On-Chip
- High Accuracy Tones Provided by 3.58MHz Crystal Oscillator
- Pin-Selectable Inhibit of Single Tone Generation

APPLICATIONS

DTMF Signalling for

- Telephone Sets
- Mobile Radio
- Remote Control
- Point-of-Sale and Banking Terminals
- Process Control

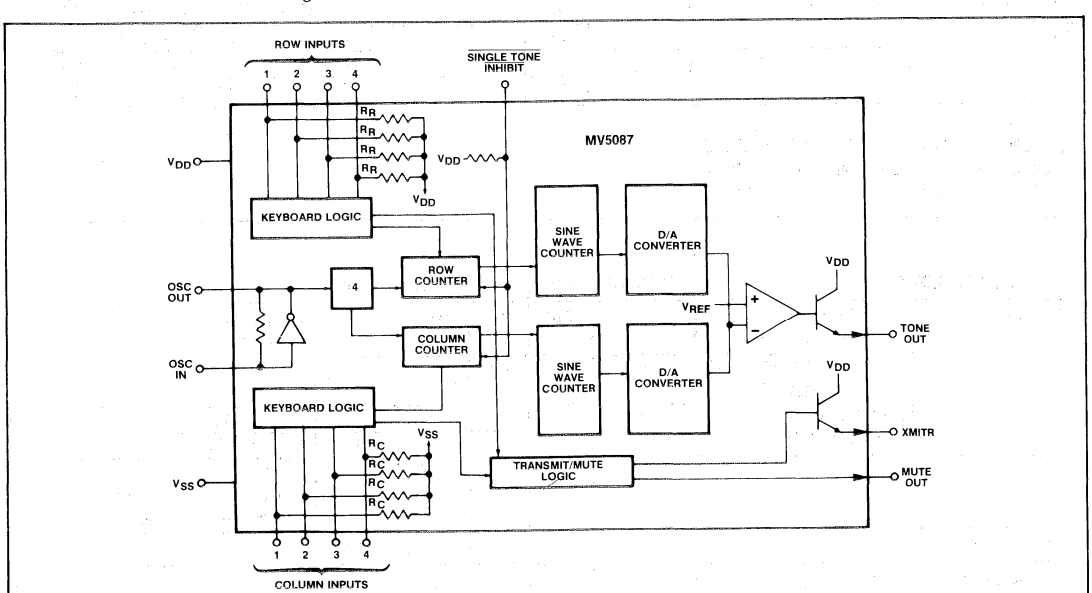


Fig.2 Functional block diagram

ABSOLUTE MAXIMUM RATINGS

	MIN.	MAX.		MIN.	MAX.
V_{DD} - V_{SS}	-0.3V	10.5V	Power dissipation		850 mW
Voltage on any pin	V_{SS} - 0.3V	V_{DD} + 0.3V	Derate 16 mW/°C above 75°C		
Current on any pin		10 mA	(All leads soldered to PCB)		
Operating temperature	-40°C	+85°C			
Storage temperature	-65°C	+150°C			

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3.5V to 10V

	CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS		
SUPPLY	Operating Supply Voltage		V_{DD}	3.5		10	V	Ref. to V_{SS}	
	Standby Supply Current		I_{DDS}		0.2	100	uA	V_{DD} = 3.5V	No Key Depressed
					0.5	200	uA	V_{DD} = 10V	All outputs Unloaded
	Operating Supply Current		I_{DD}		1.0	2.0	mA	V_{DD} = 3.5V	One Key Depressed
					5.0	10.0	mA	V_{DD} = 10V	All outputs Unloaded
INPUTS	$\overline{\text{SINGLE TONE}}$ $\overline{\text{INHIBIT}}$	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}		V_{DD}	V		
		INPUT LOW VOLTAGE	V_{IL}	0		0.3V_{DD}	V		
		INPUT RESISTANCE	R_{IN}		60		KΩ		
	ROW 1-4	INPUT HIGH VOLTAGE	V_{IH}	0.9V_{DD}			V		
		INPUT LOW VOLTAGE	V_{IL}			0.3V_{DD}	V		
	COLUMN 1-4	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}			V		
		INPUT LOW VOLTAGE	V_{IL}			0.1V_{DD}	V		
OUTPUTS	XMITR	SOURCE CURRENT	I_{OH}	-15	-25		mA	V_{DD} = 3.5V, V_{OH} = 2.5V	No Keyboard Entry
				-50	-100		mA	V_{DD} = 10V, V_{OH} = 8V	
		LEAKAGE CURRENT	I_{OZ}		0.1	10	uA	V_{DD} = 10V, V_{OH} = OV	Keyboard Entry
	MUTE	SINK CURRENT	I_{OL}	0.5			mA	V_{DD} = 3.5V, V_{OL} = 0.5V	No Keyboard Entry
				1.0			mA	V_{DD} = 10V, V_{OL} = 0.5V	
		SOURCE CURRENT	I_{OH}	-0.5			mA	V_{DD} = 3.5V, V_{OH} = 3.0V	Keyboard Entry
				-1.0			mA	V_{DD} = 10V, V_{OH} = 9.5V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3.5V to 10V

CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS	
TONE OUT	ROW TONE OUTPUT VOLTAGE	V_{OR}	320	400	500	mV_{RMS}	Single Tone R_L = 1KΩ
	COLUMN TONE OUTPUT VOLTAGE	V_{OC}	400	500	630	mV_{RMS}	
	EXTERNAL LOAD IMPEDANCE	R_L	700			Ω	V_{DD} = 3.5V
			330			Ω	V_{DD} = 10V
OUTPUT DISTORTION					-20	dB	Total out-of-band power relative to sum of row and column fundamental power
PRE EMPHASIS, High Band			1		3	dB	
Tone Output Rise Time		t_r		3	5	ms	

PIN FUNCTIONS

PIN	NAME	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	XMITR	Emitter output of a bipolar transistor whose collector is connected to V_{DD}. With no keyboard input this output remains at V_{DD} and a keyboard input changes the output to a high impedance state. The state of Single Tone Inhibit input has no effect on XMITR output.
3,4,5,9	Column 1-4	These inputs are held at V_{SS} by resistors Rc and sense a valid logic level (approx $^1/_2$ V_{DD}) when tied to a Row input.
6	V_{SS}	Negative Power Supply (OV)
7,8	OSC In, OSC Out	On-chip inverter completes the oscillator when a 3,579545 MHz crystal is connected to these pins. OSC In is the inverter input and OSC Out is the output.
10	Mute	This CMOS Output switches to V_{SS} with no keyboard input and to V_{DD} with a keyboard input. This output is unaffected by the state of Single Tone Inhibit.
11,12,13,14	Row 1-4	These inputs are held at V_{DD} by resistors R_R and sense a valid logic level (Approx $^1/_2$ V_{DD}) when tied to a column input.
15	Single Tone Inhibit	This input has a pull-up resistor to V_{DD} and when left unconnected or tied to V_{DD}, single or dual tones may be generated. When V_{SS} is applied dual tones only are generated and no input combinations will cause generation of a single tone.
16	Tone Out	Emitter output of a bipolar NPN transistor whose collector is tied to V_{DD}. Input to this transistor is from an op-amp which mixes, and regulates the output level of, the row and column tones.

ROW AND COLUMN INPUTS

These inputs are compatible with the standard 2-of-8 keyboard, single contact (form A) keyboard and electronic input. Figures 3 and 4 show these input configurations, and Fig. 5 shows the internal structure of these inputs.

When operating with a keyboard, dual tones are generated when any single button is pushed. Single tones are generated when more than one button is pushed in any row or column. No tones are generated when diagonally-positioned buttons are simultaneously pressed.

An electronic input to a single column generates that single column tone. Inputs to multiple columns generates no tone. An electronic input to a single row generates no tone and a single row tone may be generated only by activating 2 columns and the desired row.

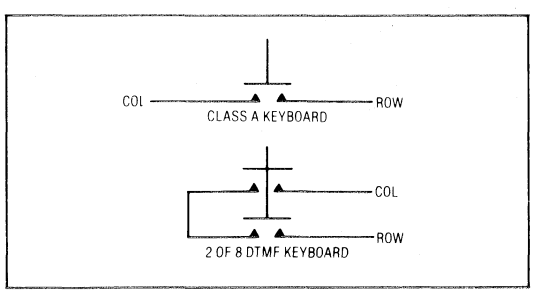


Fig.3 Keyboard configuration

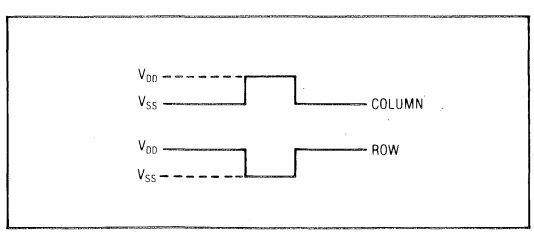


Fig.4 Electronic input

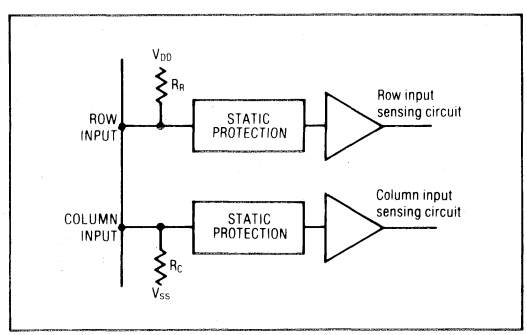


Fig.5 Row and column inputs

OUTPUT FREQUENCY

Table 1 shows the output frequency deviation from the standard DTMF frequencies when a 3.58MHz crystal is used as the reference.

The row and column output waveforms are digitally synthesised using R-2R D-to-A converters (see Fig.6), resulting in a 'staircase' approximation to a sinewave. An op-amp mixes these tones to produce a dual-tone waveform. Single tone distortion is typically better than 7% and all distortion components of the mixed dual-tone should be -30dB relative to the strongest fundamental (column tone).

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
Row	f_1	697	701.3	+0.62	Low Group
	f_2	770	771.4	+0.19	
	f_3	852	857.2	+0.61	
	f_4	941	935.1	-0.63	
Column	f_5	1209	1215.9	+0.57	High Group
	f_6	1336	1331.7	-0.32	
	f_7	1477	1471.9	-0.35	
	f_8	1633	1645.0	+0.73	

Table 1 Output frequency deviation

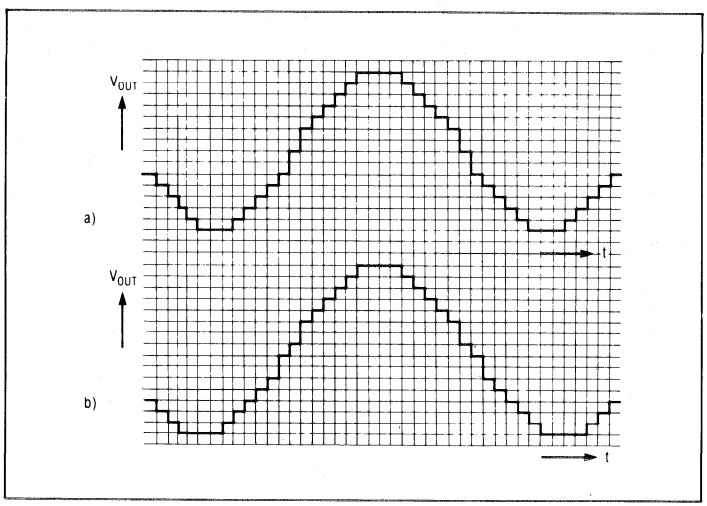


Fig.6 Typical sinewave output (a) Row tones (b) Column tones

DISTORTION MEASUREMENTS

THD for the single tone is defined by:

$$100\left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \text{----} V_{nf}^2}}{V_{fundamental}}\right)\%$$

Where V_{2f} -- V_{nf} are the Fourier components of the waveform.

THD for the dual tone is defined by:

$$100\left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 \text{--} V_{nR}^2 + V_{2C}^2 + V_{3C}^2 \text{---} V_{nc}^2 + V_{IMD}^2}}{\sqrt{V_{ROW}^2 + V_{COL}^2}}\right)$$

where V_{ROW} is the row fundamental amplitude
V_{COL} is the column fundamental amplitude
V_{2R} -- V_{nR} are the Fourier component amplitudes of the row frequencies
V_{2C} -- V_{nC} are the Fourier component amplitudes of the column frequencies
V_{IMD} is the sum of all intermodulation components.

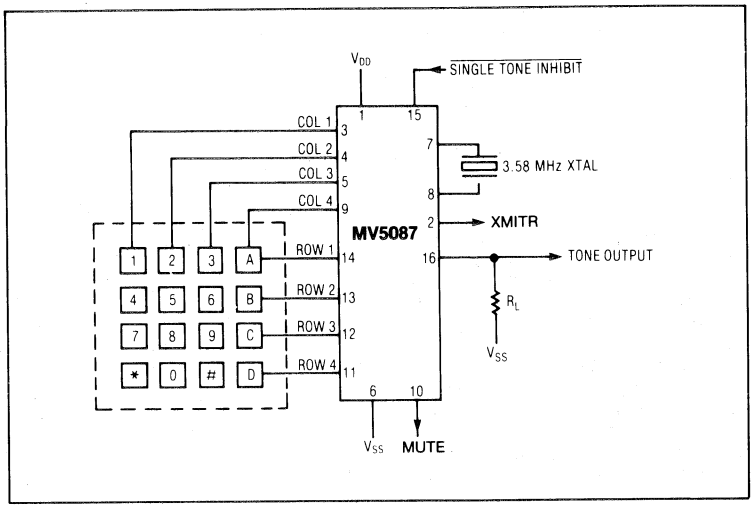


Fig.7 Connection diagram

DS3126-1.0

MV5089

DTMF GENERATOR

The MV5089 is fabricated using ISO-CMOS high density technology and offers low power and wide voltage operation. An inexpensive 3.58MHz TV crystal completes the reference oscillator. From this frequency are derived 8 different sinusoidal frequencies which, when appropriately mixed, provide Dual-Tone Multi-Frequency (DTMF) tones.

Inputs are compatible with a standard 2-of-8 active-low keyboard and the keyboard entries determine the correct division of the reference frequency by the row and column counters.

D-to-A conversion, using R-2R ladder networks, results in a staircase approximation of a sinewave with low total distortion.

Frequency and amplitude stability over operating voltage and temperature range are maintained within industry specifications.

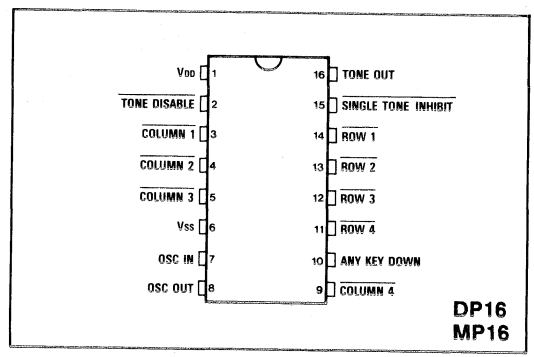


Fig.1 Pin connections - top view

FEATURES

- Pin-for-Pin Replacement for MK5089
- Low Standby Power
- Minimum External Parts Count
- 2.75V to 10V Operation
- 2-of-8 Keyboard Input
- High Accuracy Tones Provided by 3.58MHz Crystal Oscillator
- Pin-Selectable Inhibit of Single Tone Generation

APPLICATIONS

DTMF Signalling for

- Telephone Sets
- Mobile Radio
- Remote Control
- Point of Sale and Banking Terminals
- Process Control

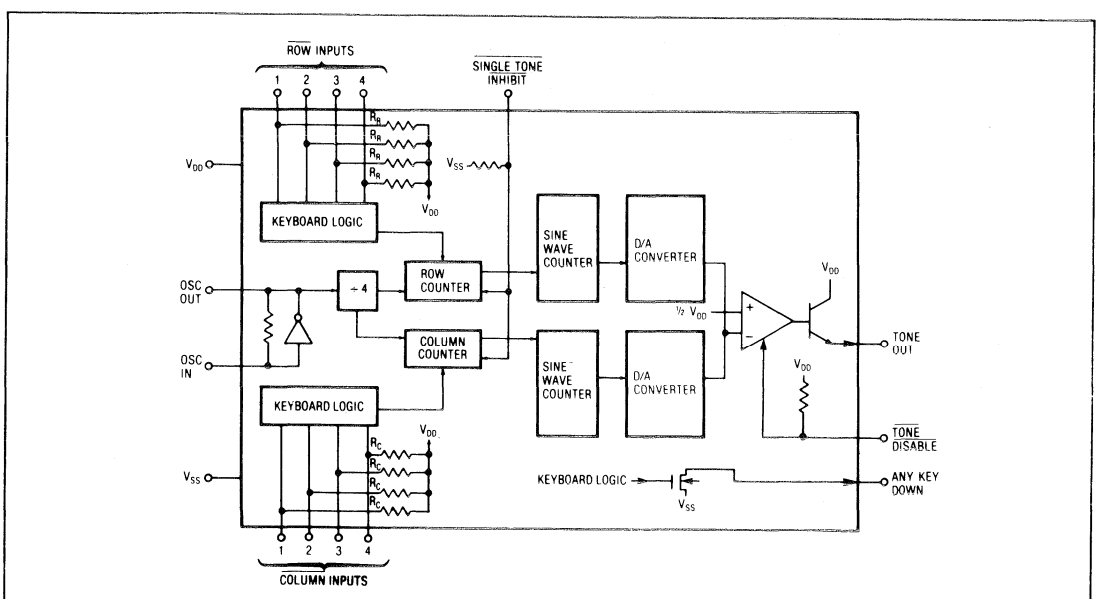


Fig.2 Functional block diagram

OUTPUT FREQUENCY

Table 1 shows the output frequency deviation from the standard DTMF frequencies when a 3.58MHz crystal is used as the reference.

The row and column output waveforms are digitally synthesised using R-2R D-to-A converters (see Fig.6) resulting in staircase approximations to a sinewave. An op-amp mixes these tones to produce a dual-tone waveform. Single tone distortion is typically better than 7% and all distortion components of the mixed dual-tone should be -30dB relative to the strongest fundamental (column tone).

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
Row	f_1	697	701.3	+0.62	Low Group
	f_2	770	771.4	+0.19	
	f_3	852	857.2	+0.61	
	f_4	941	935.1	−0.63	
Column	f_5	1209	1215.9	+0.57	High Group
	f_6	1336	1331.7	−0.32	
	f_7	1477	1471.9	−0.35	
	f_8	1633	1645.0	+0.73	

Table 1 Output frequency deviation

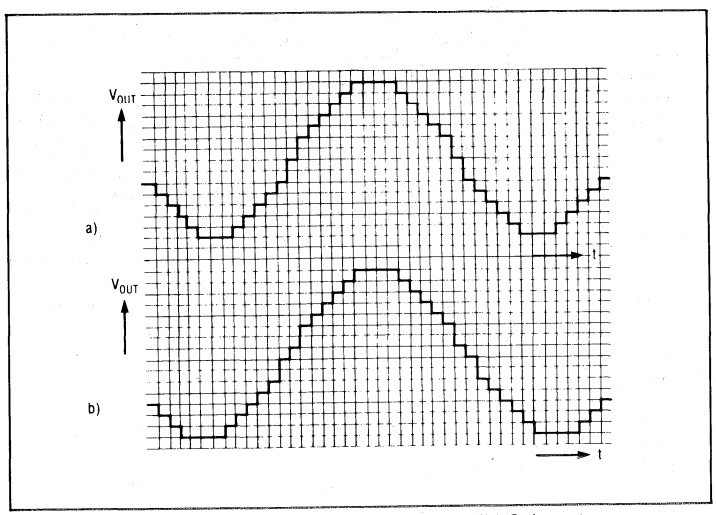


Fig.6 Typical sinewave output (a) Row tones (b) Column tones

DISTORTION MEASUREMENTS

THD for the single tone is defined by:

$$100\left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \cdots V_{nf}^2}}{V_{fundamental}}\right)\%$$

Where V_{2f} -- V_{nf} are the Fourier components of the waveform.

THD for the dual tone is defined by:

$$100\left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 \cdots V_{nR}^2 + V_{2C}^2 + V_{3C}^2 \cdots V_{nc}^2 + V_{IMD}^2}}{\sqrt{V_{ROW}^2 + V_{COL}^2}}\right)$$

where V_{ROW} is the row fundamental amplitude
V_{COL} is the column fundamental amplitude
V_{2R} -- V_{nR} are the Fourier component amplitudes of the row frequencies
V_{2C} -- V_{nC} are the Fourier component amplitudes of the column frequencies
V_{IMD} is the sum of all intermodulation components.

PIN FUNCTIONS

PIN	NAME	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	$\overline{\text{TONE DISABLE}}$	This input has an internal pull-up resistor to V_{DD}. When connected to V_{SS} no tones are generated by any key depression allowing the keyboard to be used for purposes other than DTMF signalling.
3,4,5,9	$\overline{\text{COLUMN 1-4}}$	These CMOS inputs are held at V_{DD} by an internal pull-up resistor and are activated by the application of V_{SS}.
6	V_{SS}	Negative Power Supply (OV)
7,8	OSC IN, OSC OUT	On-chip inverter completes the oscillator when a 3,58 MHz Crystal is connected to these pins. OSC IN is the inverter input and OSC OUT is the output.
10	Any Key Down	This is an NMOS transistor output which switches to V_{SS} while any key is depressed. Otherwise this output is high impedance. Switching is independent of Tone Disable and Single Tone Inhibit.
11,12,13,14	$\overline{\text{Row 1-4}}$	As $\overline{\text{Column 1-4}}$ inputs.
15	$\overline{\text{Single Tone Inhibit}}$	This input has a pull-down resistor to V_{SS}. When left unconnected or tied to V_{SS}, dual tones may be generated, but keyboard input combinations resulting in single tone generation are inhibited. When V_{DD} is applied single or dual tones may be generated.
16	Tone Out	Emitter output of a bipolar NPN transistor whose collector is tied to V_{DD}. Input to this transistor is from an op-amp which mixes the Row and Column tones.

ROW AND COLUMN INPUTS

These inputs are compatible with the standard 2-of-8 keyboard or with an electronic input. Figures 3 and 4 show these input configurations and Fig.5 shows the internal chip structure of these inputs.

When operating with a keyboard, dual tones are generated when any single button is pushed.

With Single Tone Inhibit at V_{DD}, connection of V_{SS} to a single column causes the generation of that Column tone. Connection of V_{SS} to more than one Column will result in no Column tones being generated. Connection of V_{SS} to Rows only generates no tone - a Column must be connected to V_{SS}.

A single Row tone only may be generated by connecting 2 columns, and the desired row, to V_{SS}.

OUTPUT TONE LEVEL

The output tone level of the MV5089 is proportional to the applied DC supply voltage.

A regulated supply will normally be used which may be designed to provide stability over the temperature range.

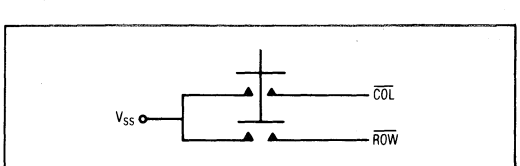


Fig.3 2 of 8 DTMF keyboard

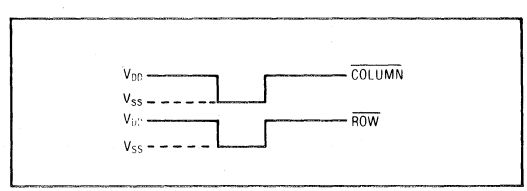


Fig.4 Electronic input

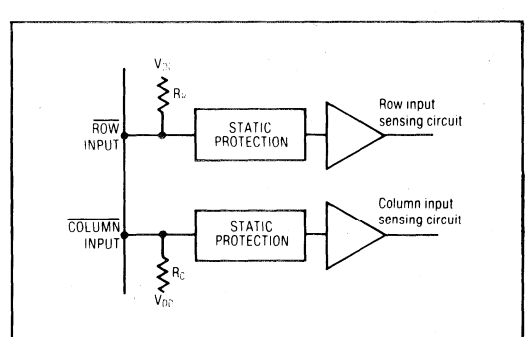


Fig.5 Row and Column inputs

ABSOLUTE MAXIMUM RATINGS

	MIN.	MAX.		MIN.	MAX.
V_{DD} - V_{SS}	-0.3V	10.5V	Power dissipation		850 mW
Voltage on any pin	V_{SS} - 0.3V	V_{DD} + 0.3V	Derate 16 mW/°C above 75°C		
Current on any pin		10 mA	(All leads soldered to PCB)		
Operating temperature	-40°C	+85°C			
Storage temperature	-65°C	+150°C			

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3V to 10V

	CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS		
SUPPLY	Operating Supply Voltage		V_{DD}	2.75		10	V	Ref. to V_{SS}	
	Standby Supply Current		I_{DDS}		0.2	100	uA	V_{DD} = 3V	No Key Depressed
					0.5	200	uA	V_{DD} = 10V	All outputs Unloaded
	Operating Supply Current		I_{DD}		1.0	2.0	mA	V_{DD} = 3V	One Key Depressed
					5.0	10.0	mA	V_{DD} = 10V	All outputs Unloaded
INPUTS	$\overline{\text{SINGLE TONE}}$	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}		V_{DD}	V		
	$\overline{\text{INHIBIT}}$	INPUT LOW VOLTAGE	V_{IL}	0		0.3V_{DD}	V		
	$\overline{\text{TONE DISABLE}}$	INPUT RESISTANCE	R_{IN}		60		KΩ		
	$\overline{\text{ROW 1-4}}$	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}		V_{DD}	V		
	$\overline{\text{COLUMN 1-4}}$	INPUT LOW VOLTAGE	V_{IL}	0		0.3V_{DD}	V		
OUTPUTS	ANY KEY DOWN	SINK CURRENT	I_{OL}	0.5			mA	V_{DD} = 3V, V_{OL} = 0.5V	
				1.0			mA	V_{DD} = 10V, V_{OL} = 0.5V	
		LEAKAGE CURRENT	I_{OZ}		1		uA	V_{DD} = 3V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3V to 10V

CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS	
TONE OUT	OUTPUT LEVEL, ROW	V_{OUT}	-10	– 8	-7	dBm	V_{DD} = 3V. Single Tone. R_L = 100KΩ
PRE EMPHASIS, High Band			2.4	2.7	3.0	dB	
OUTPUT DISTORTION (Dual Tone)					– 20	dB	Total out-of-band power relative to sum of row and column fundamental power
Tone Output Rise Time		t_r		3	5	ms	Time for waveform to reach 90% of magnitude of either frequency from initial key stroke

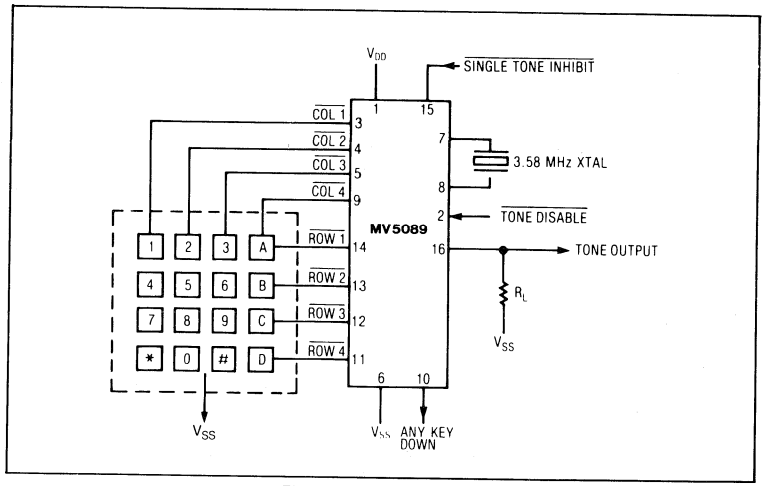


Fig.7 connection diagram

DS3147-1.1
Supersedes CD804D-2.1

MA535

DTMF DIALLER WITH REDIAL

The MA535 is a low power CMOS DTMF dialler with a 21-digit last number redial store. The device is capable of generating all 16 DTMF characters including *, #, A, B, C and D.

The 21-digit LNR store will automatically retain the digits dialled in a call for redial later. A PIN (Personal Identification Number) confidentiality feature ensures that security codes are not retained. The store contents are maintained by a minimal current leaked from the telephone line whilst on-hook.

The MA535 can also generate an accurate Timed Break Recall (Flash) signal and offers a common operating protocol for Earth Loop Recall. Mask options are available for various TBR (Flash) periods and DTMF tone on/off periods.

The oscillator circuit is of the 'single pin' type and requires no external components other than an inexpensive 560kHz ceramic resonator, resulting in substantial cost savings compared with crystal based oscillator circuits.

For applications where tone filtering is required, an on-chip unity-gain amplifier is provided, requiring only passive external components to implement a second-order low pass filter.

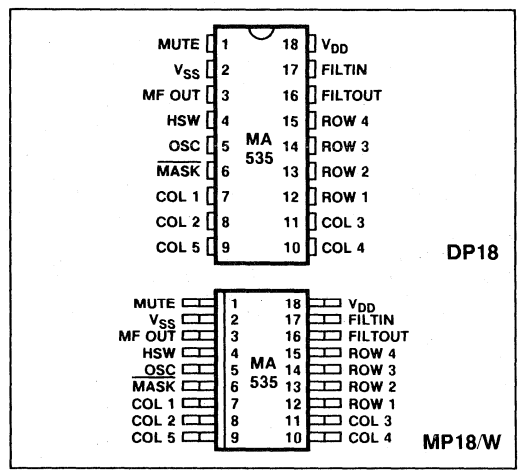


Fig.1 Pin connections - top view (not to scale)

FEATURES

- Full 16 Tone Pairs with Controlled Minimum Tone Burst.
- 21 Digit Last Number Redial.
- Timed Break Recall (Flash)
- Common Protocol for TBR (Flash) and Earth Recall.
- Uses Inexpensive 560kHz Ceramic Resonator.
- Low Power CMOS.
- Mask Programmable Options to suit Application.
- PIN (Personal Identification Number) Confidentiality Feature.
- No Signalling Output for Simultaneous Key Depressions.

PIN FUNCTIONS

Pin number	Pin Name	Function
1	MUTE	Output active during keying and tone transmission (see note 1)
2	V_{SS}	Negative supply
3	MF OUT	Unfiltered DTMF output
4	HSW	Hookswitch input - a logic 1 at this pin indicates 'Off-Hook'
5	OSC	Connect a 560 kHz ceramic resonator between this pin and V_{SS}
6	MASK	Output used to signal TBR (Flash)(see note 2)
7	COL1	Connections for 20 button single contact keypad
8	COL2	
9	COL5	
10	COL4	
11	COL3	
12	ROW1	
13	ROW2	
14	ROW3	
15	ROW4	
16	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
17	FILT OUT	
18	V_{DD}	Positive supply

1. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.
2. MASK may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.

Table 1 Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA535 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 217-224ms. This is so that short line breaks of less than 217ms, such as line reversals applied by the exchange, are ignored. In this case the $\overline{\text{MASK}}$ output will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted.This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 6.7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start up time if it was not already running).

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again. Keypad layout and connections are shown in Fig. 2.

	COL 1	COL 2	COL 3	COL 4	COL 5
ROW 1	1	2	3	A	LNR
ROW 2	4	5	6	B	TBR
ROW 3	7	8	9	C	
ROW 4	*	0	#	D	

Fig.2 Keypad layout and connections

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 21 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number.

The last number redial store has several features designed to assist the user.

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the LNR key. In this case, the remainder of the number will be dialled when the LNR key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

PIN confidentiality feature

DTMF signalling is often used for data transactions, where the characters A, B, C, D, * and #, which are not normally required in telephone numbers, are used.

To ensure confidentiality of PIN (Personal Identification Number) codes, if a call contains the digits A, B, C, D, * or #, only those digits dialled prior to the first press of either A, B, C, D, * or #, will be retained in the LNR store.

Timed Break & Earth Loop Recall (TBR) (Flash)

The MA535 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the LNR store is cleared. No further digits will be accepted during the current off-hook period.

A TBR (Flash) of 98ms[1] is generated when the TBR key is pressed. The MASK output goes low in order to produce the line break. The MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fig.3, or by use of a double contact switch.

[1]*Other TBR (Flash) periods are available as mask options (see page 1-20)*

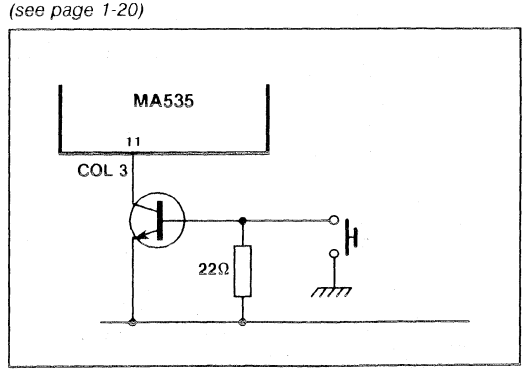


Fig.3 Earth loop recall

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC and V_{SS} to provide a timing reference for all chip functions. No other components are required or should be used.

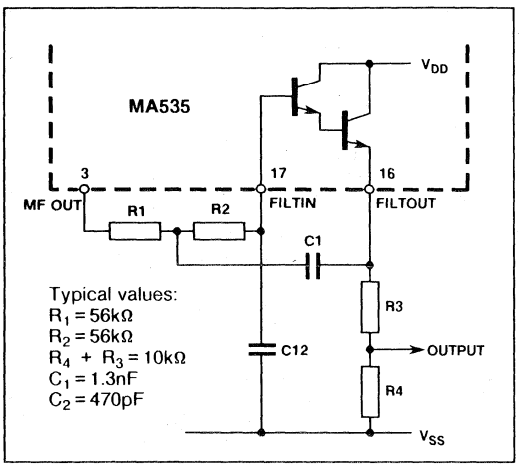


Fig.4 DTMF tone filtering

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 16 & 17) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The MF OUT output rises to its DC level of 0.9 V_{DD} at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 98ms on, followed by 98ms off[1]. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 98 ms, the tone output will continue until the key is released.

(1) *Tone on/off periods of 84/84 ms are available as mask options (see page 1-20).*

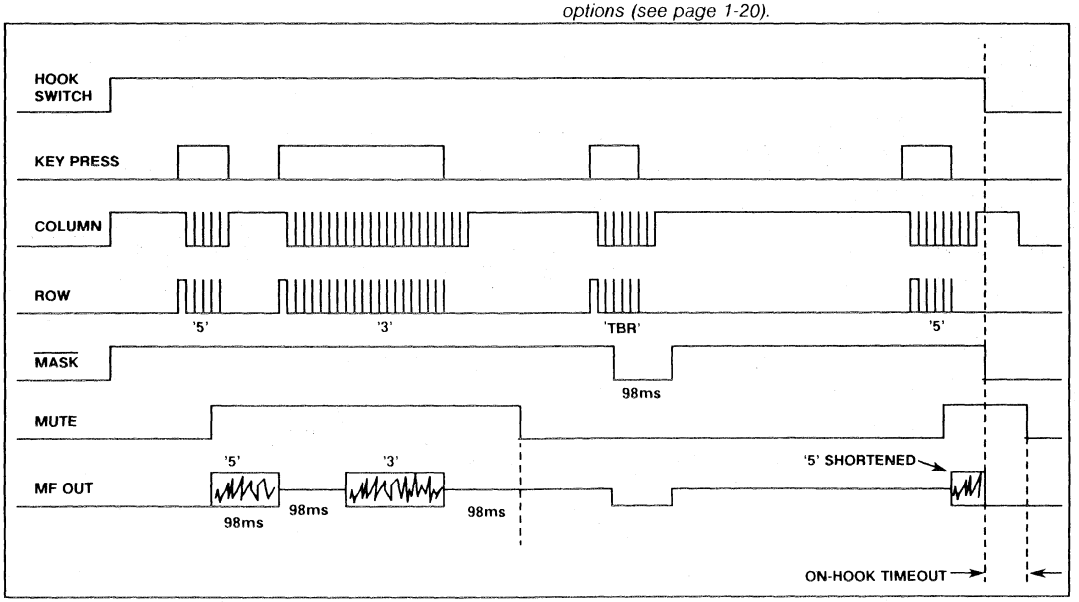


Fig.5 DTMF timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	- 0.07	- 0.10	+ 0.19	- 0.15	- 0.17	- 0.20	- 0.22	- 0.31

Table 2 Tone frequencies

MASK OPTIONS

The MA535 has been designed so that the TBR (Flash) period and DTMF tone on/off periods can be altered quickly and inexpensively at the final stage of manufacture. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit.

The options, listed in Table 3, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

TBR (Flash) period		DTMF tone on/off period	
Option	**Duration**	**Option**	**Duration**
a	***98 ms***	***a***	***98/98 ms***
b	105 ms	b	84/84 ms
c	196 ms		
d	210 ms		
e	294 ms		
f	315 ms		
g	392 ms		
h	420 ms		
i	490 ms		
j	525 ms		
k	588 ms		
l	630 ms		

Table 3 Mask options

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V, T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Supply Current: On-hook		< 1	5.0	μA	V_{DD} = 2.0V
Off-hook		1.5		μA	MF OUT low
MF tone sending			1.0	mA	
Output high voltage (MASK and MUTE outputs)	2.2			V	I = -1mA
Output low voltage (MASK and MUTE outputs)			0.3	V	I = +1mA
MF OUT DC level during tone sending		$0.9V_{DD}$		V	
MF OUT output resistance		3		kΩ	
'Key Pressed' resistance			2	kΩ	$2.5V < V_{DD} < 5.7V$
'Key Not Pressed' resistance	500			kΩ	$2.5V < V_{DD} < 5.7V$
Darlington pair current gain (see Fig. 4)	600	50,000			I_E = 100μA, V_{CE} = 2V

AC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Tone output: low group	57	64		mV rms	No load. See note 1.
high group		81	91	mV rms	No load. See note 1.
High-to-Low group amplitude ratio (pre-emphasis)	1.5	2	2.5	dB	See note 2.
Total harmonic distortion: 0-4 kHz		1.5		%	
0-10 kHz		2.5		%	
0-50 kHz		5.0		%	
0-200 kHz		6.5	10	%	
Oscillator start-up time		< 0.1	1	ms	

NOTES
1. DTMF tone output level is proportional to supply voltage (V_{DD}).
2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition	Min.	Typ.	Max.	Units	Notes
Supply Voltage: On-hook	2.0		5.7	V	
Off-hook	2.4		5.7	V	
Hookswitch Input: On-hook			$0.2V_{DD}$	V	
Off-hook	$0.8V_{DD}$			V	
Oscillating frequency		560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}–V_{SS}	– 0.3 to + 6.5V
Voltage on any pin (except HSW)	V_{SS} – 0.3V to V_{DD} + 0.3V
Voltage on HSW pin (See note 1)	V_{SS} – 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	± 1mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	–5 to 0mA
Storage temperature	–55°C to + 125°C
Operating temperature range	–10°C to + 55°C

NOTES
1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300μA max. no damage will occur. 2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

APPLICATIONS CIRCUITS

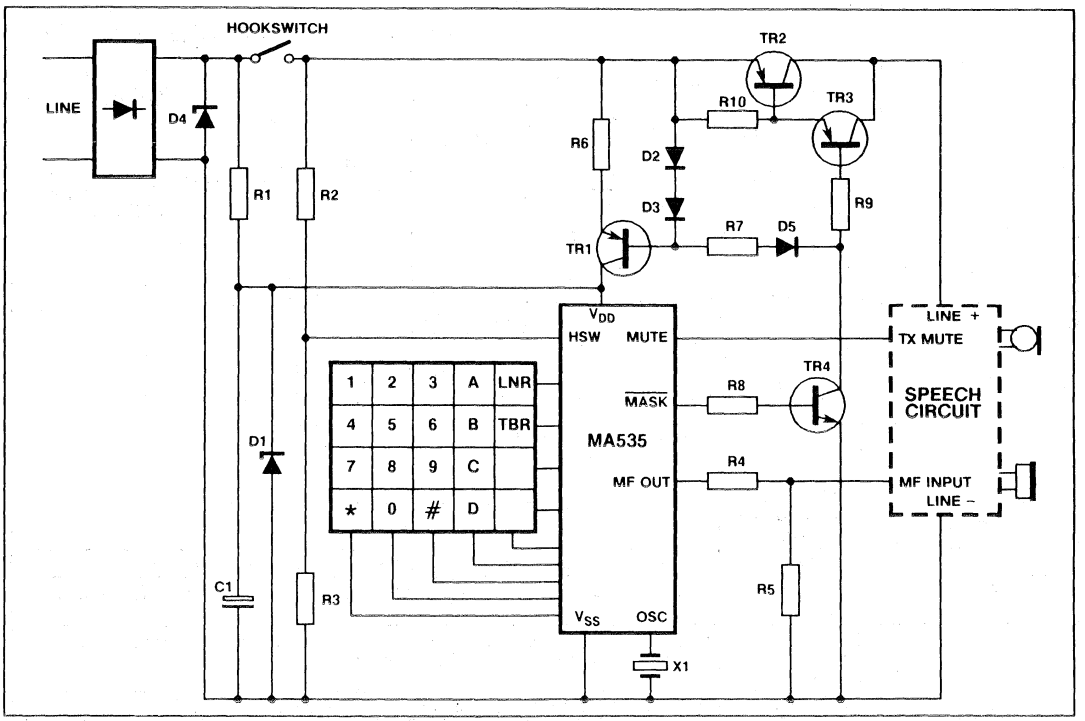


Fig.6 Application circuit 1 (with TBR)

Component	Nominal Value	Function
R1	2.2MΩ	R1 provides current to maintain redial memory whilst on-hook.
R2, R3	560kΩ	R2 & R3 present a logic '1' to the HSW input when the instrument is off-hook.
R4 R5	See function See function	R4 and R5 provide the correct level of tone. When the filter current is incorporated , the sum of R4 and R5 should be between 1kΩ and 10kΩ to allow sufficient bias for the filter amplifier.
TR1 D1 D2, R6 R7	BF423 or MPSA93 2.5V Zener GP Diodes 200Ω 56kΩ	These components provide a stable supply voltage for the MA535. The constant current source delivers a current defined by I×0.6/R6. The Zener diode (D1) defines the operating voltage and may comprise four BA314 diodes or a BZV462V0 and a BA314.
Speech circuit		The speech circuit of Fig. 6 is used to couple the DTMF tones to line.
C1	47μF	C1 provides current during line breaks.
X1	560kHz	X1 is a ceramic resonator which provides accurate timing for the chip.
D4	130V	D4 provides protection from line transients.
D5 R8 R9 R10 TR2, TR3, TR4	GP Diode 4.7kΩ 100 kΩ 6.2kΩ BF423	These components allow the TBR (Flash) signal generated on the $\overline{\text{MASK}}$ output of the MA535 to be coupled to line. During a TBR, the speech circuit is cut off as is the normal supply to the MA535 via TR1, in order to produce a clean line break. During a TBR capacitor C1 supplies the MA535.

Table 4 Application circuit 1 components

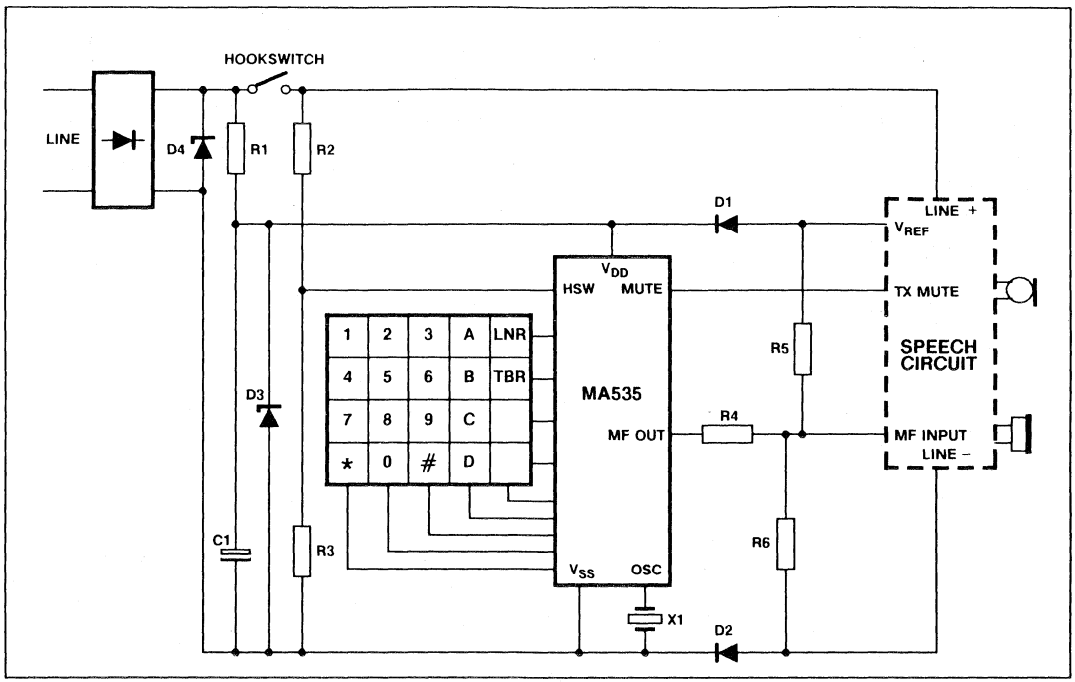


Fig.7 Application circuit 2 (without TBR)

Component	Nominal Value	Function
R1	2.2MΩ	R1 provides current to maintain redial memory whilst on-hook.
R2 R3	560kΩ 560kΩ	R2 & R3 present a logic '1' to the HSW input when the instrument is off-hook.
R4 R5 R6	See function See function See function	Resistors R4, R5, and R6 provide a potential divider network to set the tone levels and required DC bias for the speech circuit.
D1	GP diode	D1 prevents the speech circuit from taking current from C1 or R1.
D2	GP diode	D2 counteracts the voltage drop across D1.
D3	5.6V Zener	D3 is a protection diode.
Speech circuit	Integrated type	The speech circuit is an integrated type, supplying a stable reference voltage for the DTMF generator,and is also used to couple the DTMF tones to line.
C1	47μF	C1 provides current during line breaks.
X1	560kHz	X1 is a ceramic resonator which provides accurate timing for the chip.
D4	130V	D4 provides protection from line transients.

Table 5 Application circuit 2 components

DS3148-1.0
Supersedes CD10702FDS-2.1

MA541 FAMILY
LD/DTMF SWITCHABLE DIALLERS

The MA541 family are keypad switchable LD/DTMF dialler devices with a last number redial facility.

Two operating modes are available: LD mode, with the ability to temporarily switch to DTMF mode from the keypad during a call, and DTMF only mode. The former mode enables subscribers to access such services as home banking.

The MA541 devices are pin compatible with the GPS switchable dialler families MA526, MA527, MA545, MA547. MA585, MA587 and MA589 – providing a complete range of telephone features within a single PCB and circuit design.

Metal mask and pin selectable options are available to service specific requirements of particular countries and customers.

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- 32 Digit Last Number Redial
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Ceramic Resonator
- Low Power CMOS
- Mask Programmable Options to suit Application
- Timed Break Recall (Flash) and Earth Recall
- Reliable Power-on Reset

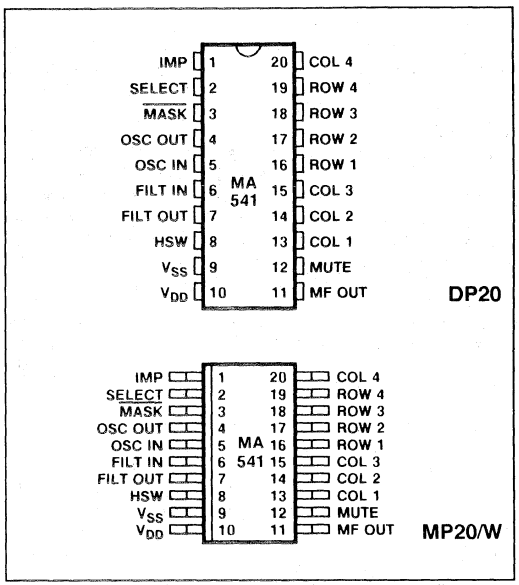


Fig.1 Pin connections - top view (not to scale)

PIN FUNCTIONS

Pin number	Pin name	Function
1	IMP	'Loop disconnect' dialling output
2	SELECT	LD/DTMF selection, IDP and B/M ratio programming
3	$\overline{\text{MASK}}$	Output to disable speech circuit during pulse dialling and recall (see note 1)
4	OSC OUT	Connections for 560kHz ceramic resonator
5	OSC IN	
6	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
7	FILT OUT	
8	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-Hook'
9	V_{SS}	Negative supply
10	V_{DD}	Positive supply
11	MF OUT	Unfiltered DTMF output
12	MUTE	Output active during keying and tone transmission (see note 2)
13	COL1	Connections for 16 button single contact keypad
14	COL2	
15	COL3	
16	ROW1	
17	ROW2	
18	ROW3	
19	ROW4	
20	COL4	

1. $\overline{\text{MASK}}$ may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1 Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA541 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied by the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted.This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start up time if it was not already running).

	COL 1	COL 2	COL 3	COL 4
ROW 1	1	2	3	TBR
ROW 2	4	5	6	LNR
ROW 3	7	8	9	SAVE (1)
ROW 4	*	0	#	TONE (1)

TBR: Timed Break Recall (Flash)
LNR: Last Number Redial
SAVE: Save last number dialled in 'SAVE Store'
TONE: Change dialling mode from LD to DTMF

(1) *These keys are only available as mask variants*

Fig.2 Keypad layout and connections

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

The dialling mode may be selected via the SELECT pin (pin 2) as detailed in Table 2. Four Loop-Disconnect options are available with different Interdigit pauses and Break/Make ratios, and one DTMF mode. If the DTMF mode is selected then dialling will remain fixed in the DTMF mode. However, if one of the LD modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing either the *, */# or TONE key (depending on mask variant – see Fig. 2 and page 1-28), provided that dialling is not in progress. If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

SELECT pin to	Dialling mode	IDP (ms)	B/Mratio
V_{SS}	LD	800	2:1
COL 1	LD	500	2:1
COL 2	LD	500	3:2
COL 3	LD	800	3:2
V_{DD}	DTMF	–	–

Table 2 Dialling mode selection

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 32 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the LNR key. In this case, the remainder of the number will be dialled when the LNR key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the */# or TONE key) to DTMF mode, only the digits dialled in LD mode will be retained. Providing that the number of digits dialled in LD mode does not exceed 32, they will be retained regardless of the number of DTMF digits entered subsequently.

DTMF Calls

A mask option is available (see page 1-28) to allow protection of PIN (Personal Identification Number) codes as follows: If a call contains the digits * or #, only those digits dialled prior to the first press of either * or # will be retained in the LNR store.

Store Operation (SAVE)

The SAVE store is available as a mask option (see page 1-28) in place of the LNR store and is 32 digits long. If the user attempts to save a number of more than 32 digits, the store is inhibited. The contents of the store are maintained until overwritten.

The SAVE key may be pressed at any time whilst off-hook. This action causes digits dialled since going off-hook to be retained and the previous contents of the store to be overwritten. Further digits may be dialled after depression of the SAVE key, but they will not be retained.

The number in the 'SAVE' store can be redialled by pressing the LNR key once, whilst in speech mode. However, if an LD to DTMF mode change was effected when the number was originally dialled, a marker(1) in the 'SAVE' store will cause the redialling to pause at this point and the speech circuit will be reactivated. If the LNR key is then pressed again, the remaining digits in the store will be redialled in DTMF.

The SAVE store offers the same 'Moving Cursor Facility' as the LNR store.

(1) *This marker requires one store location.*

Timed Break & Earth Loop Recall (Flash)

The MA541 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled after the ELR/TBR operation will be retained in the LNR store (2).

A TBR (Flash) of 100ms (3) is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fig. 3, or by use of a double contact switch.

(2) *A version where only the digits dialled before ELR/TBR are retained in the LNR store is available as a mask option (see page 1-28).*

(3) *Other TBR (Flash) periods are available as mask options (see page 1-28).*

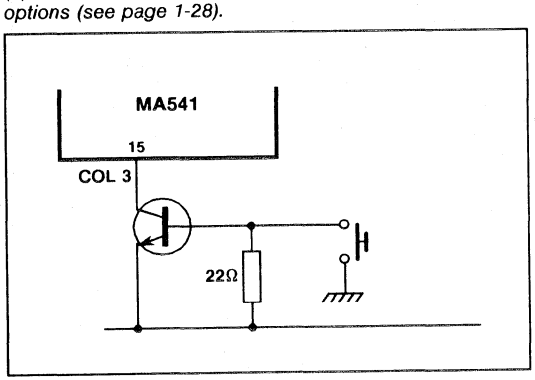


Fig.3 Earth loop recall

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally, the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 16 & 17) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

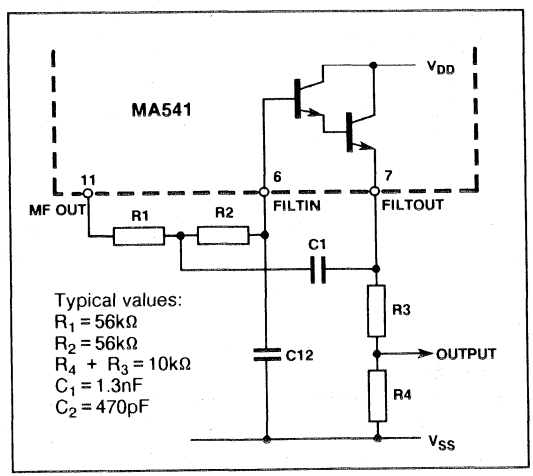


Fig.4 DTMF tone filtering

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The IMP output remains low during tone transmission. The MF OUT output rises to its DC level of 0.9 V_{DD} at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 100ms, the tone output will continue until the key is released.

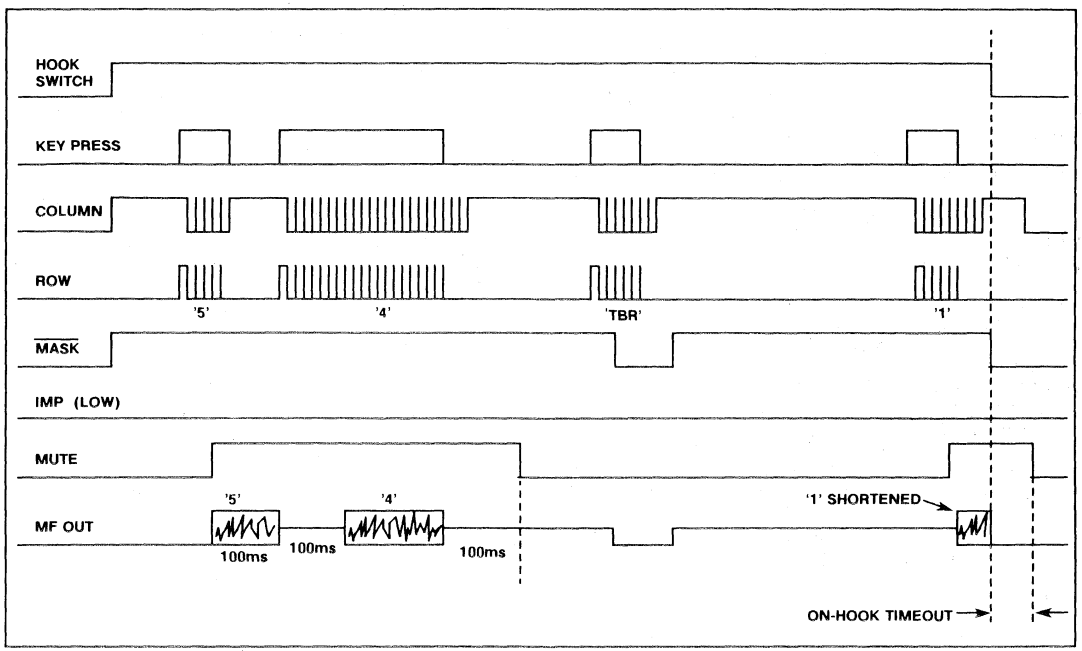


Fig.5 DTMF mode timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	- 0.07	- 0.10	+0.19	- 0.15	- 0.17	- 0.20	- 0.22	- 0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 3 Tone frequencies

LOOP-DISCONNECT DIALLING

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic '0' during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling. LD dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

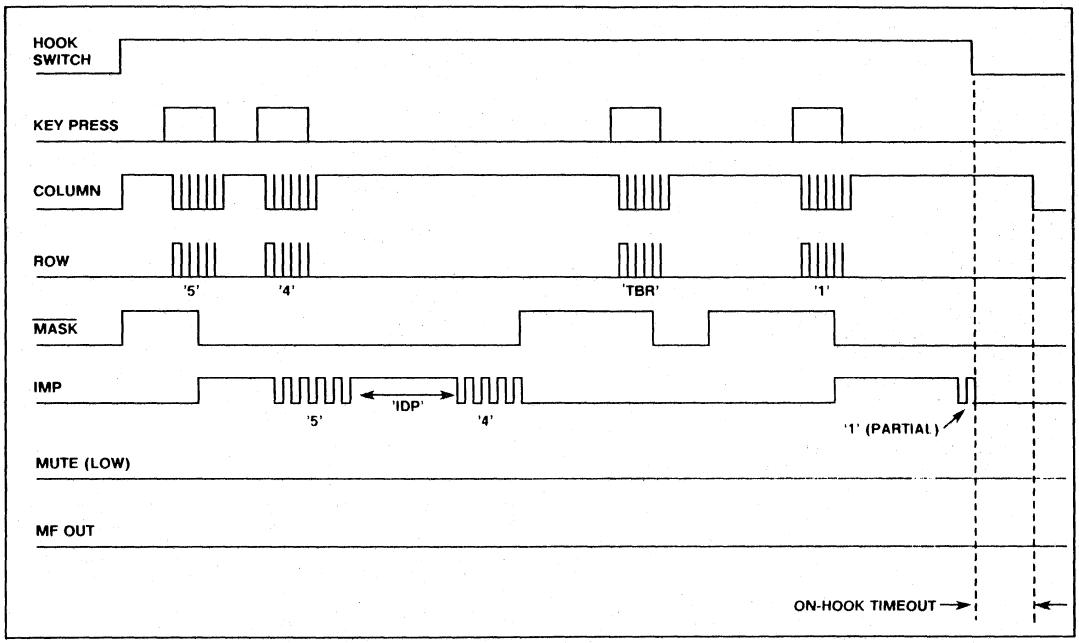


Fig.6 LD mode timing diagram

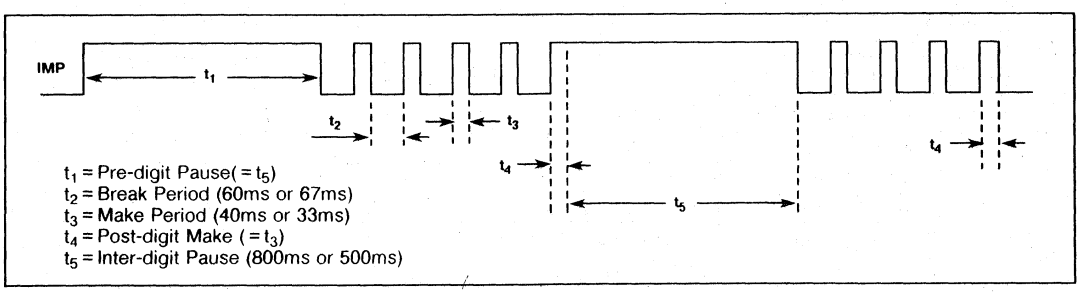


Fig.7 Timing data

MASK OPTIONS

The MA541 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufacture. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit.

The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

1. TBR (Flash) Period
- ***a. 100 ms***
- b. 200 ms
- c. 300 ms
- d. 400 ms
- e. 500 ms
- f. 600 ms

2. LD to DTMF Keypad Switching
- ***a. * and # keys***
- b. TONE key

3. Retention of Post-*/# Digits in LNR Store(DTMF mode)
- ***a. All digits retained***
- b. Digits before * or # retained

4. LNR or SAVE store
- ***a. LNR***
- b. SAVE

5. Recall (Flash) / LNR Protocol
- ***a. Digits dialled after recall retained***
- b. Digits dialled before recall retained

6. Pin 3
- ***a. $\overline{\text{MASK}}$***
- b. MASK

7. Pin 1
- ***a. IMP***
- b. $\overline{\text{IMP}}$
- c. [IMP + $\overline{\text{MASK}}$]
- d. $\overline{\text{[IMP + MASK]}}$

8. Pin 12
- ***a. $\overline{\text{MUTE}}$***
- b. $\overline{\text{MUTE}}$

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V, T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Supply Current: On-hook		<0.2	5.0	μA	V_{DD} = 2.0V. See note 1.
Off-hook		1.5		μA	MF OUT low
MF tone sending			1.0	mA	
LD impulsing			200	μA	
Output high voltage ($\overline{\text{MASK}}$, MUTE and IMP outputs)	2.2			V	I = -1mA
Output low voltage ($\overline{\text{MASK}}$, MUTE and IMP outputs)			0.3	V	I = +1mA
MF OUT DC level during tone sending		$0.9V_{DD}$		V	
MF OUT output resistance		3		kΩ	
'Key Pressed' resistance			2	kΩ	$2.5V < V_{DD} < 5.7V$
'Key Not Pressed' resistance	500			kΩ	$2.5V < V_{DD} < 5.7V$
Darlington pair current gain (see Fig. 4)	600	50,000			I_E = 100μA, V_{CE} = 2V

NOTE 1. Specially screened versions with lower on-hook supply current are available.

AC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Tone output: low group	57	64		mV rms	No load
high group		81	91	mV rms	No load
High-to-Low group amplitude ratio (pre-emphasis)	1.5	2	2.5	dB	See note 2.
Total harmonic distortion: 0-4 kHz		1.5		%	
0-10 kHz		2.5		%	
0-50 kHz		5.0		%	
0-200 kHz		6.5	10	%	
Oscillator start-up time		<0.1	1	ms	

NOTE 2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition	Min.	Typ.	Max.	Units	Notes
Supply Voltage: On-hook	1.8		5.7	V	For memory retention
Off-hook	2.4		5.7	V	
Hookswitch Input: On-hook			$0.2V_{DD}$	V	
Off-hook	$0.8V_{DD}$			V	
Oscillating frequency		560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}–V_{SS}	– 0.3 to + 6.5V
Voltage on any pin (except HSW)	V_{SS} – 0.3V to V_{DD} + 0.3V
Voltage on HSW pin (See note 1)	V_{SS} – 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	± 1mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	–5 to 0mA
Storage temperature	–55°C to + 125°C
Operating temperature range	–10°C to + 55°C

NOTES

1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300μA max. no damage will occur.
2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

APPLICATION CIRCUITS

The circuit in Fig. 8 uses a constant current supply to take current from the telephone line which is used to power the MA541. The 2.5V reference diode produces a stabilised supply voltage which determines the MF tone level of the MA541.

In Fig. 9, a stabilising voltage from the speech circuit is used to supply the MA541 during MF dialling to give accurate tone levels.

The MA541 is powered via the 150kΩ resistor during TBR operations and LD dialling breaks, and via TR1 during dialling makes. This configuration minimises the component count at the expense of allowing a leakage current of about 450μA during dialling breaks. The 47μF reservoir capacitor maintains and smooths the supply to the chip.

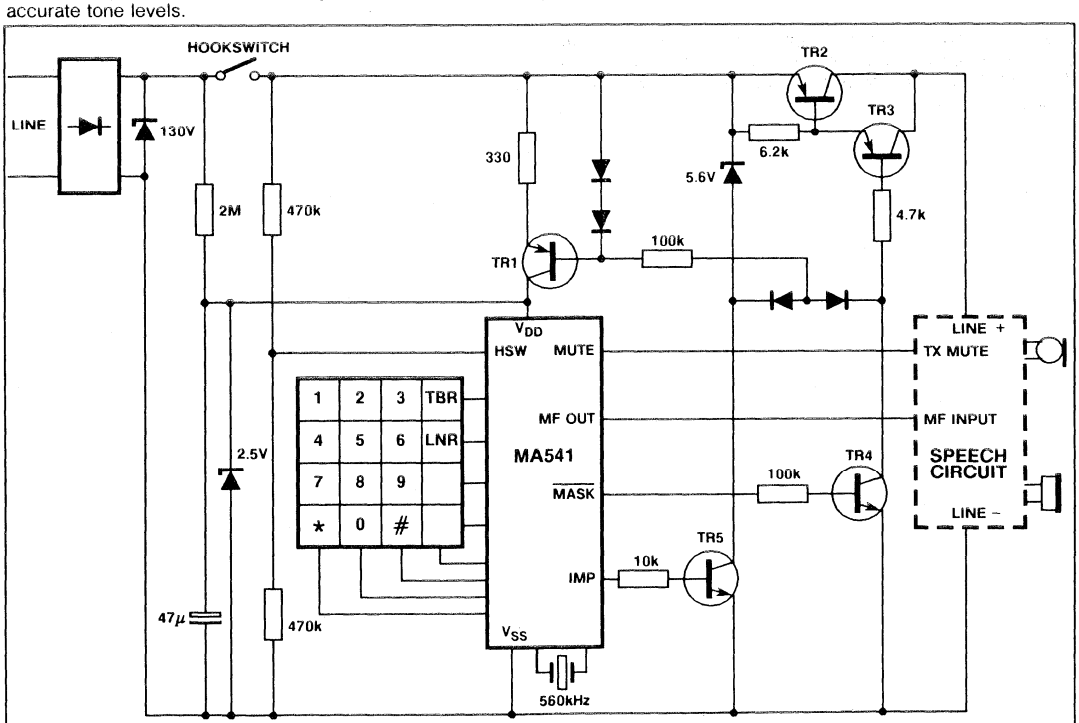


Fig.8 Application circuit 1

APPLICATION CIRCUITS (Continued)

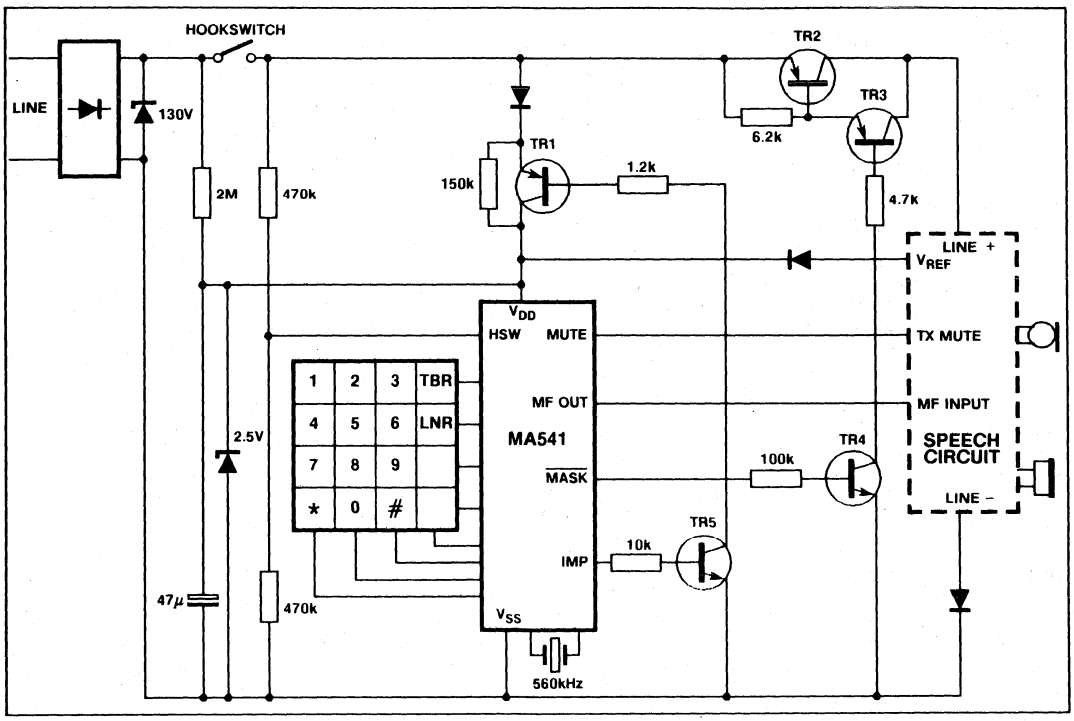


Fig.9 Application circuit 2

NOTE: Except for keypad functions and layout, the application circuits shown in Figs. 8 and 9 apply equally to the MA545, MA547, MA585, MA587 and MA589 dialler families.

DS3149-1.0
Supersedes CD10700FDS-1.1

MA545 FAMILY

LD/DTMF SWITCHABLE DIALLERS WITH 10 MEMORIES

The MA545 family are keypad switchable LD/DTMF dialler devices with a last number redial facility and ten 24-digit memories.

Two operating modes are available: LD mode, with the ability to temporarily switch to DTMF mode from the keypad during a call, and DTMF only mode. The former mode enables subscribers to access such services as home banking. Mixed LD and DTMF numbers can also be stored in memory.

The MA545 devices are pin compatible with the GPS switchable dialler families MA526, MA527, MA541, MA547. MA585, MA587 and MA589 – providing a complete range of telephone features within a single PCB and circuit design.

Metal mask and pin selectable options are available to service specific requirements of particular countries and customers.

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- 24 Digit Last Number Redial
- 10 × 24-Digit Memories
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Ceramic Resonator
- Battery-less operation - Low Power CMOS
- Mask Programmable Options to suit Application
- Timed Break Recall (Flash) and Earth Recall

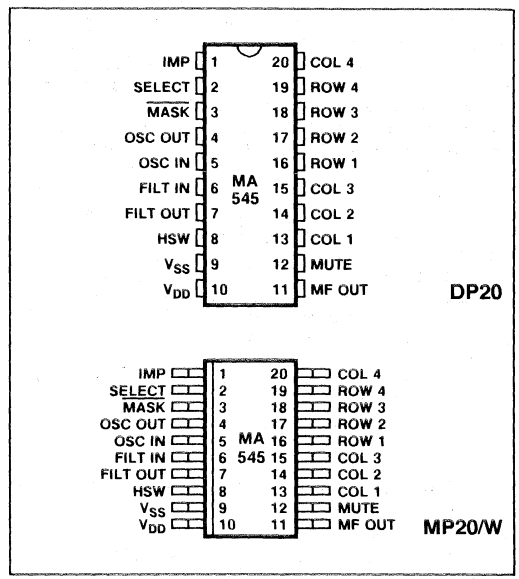


Fig.1 Pin connections - top view (not to scale)

PIN FUNCTIONS

Pin number	Pin name	Function
1	IMP	'Loop disconnect' dialling output
2	SELECT	LD/DTMF selection, IDP and B/M ratio programming
3	MASK	Output to disable speech circuit during pulse dialling and recall (see note 1)
4	OSC OUT	Connections for 560kHz ceramic resonator
5	OSC IN	
6	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
7	FILT OUT	
8	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-Hook'
9	V_{SS}	Negative supply
10	V_{DD}	Positive supply
11	MF OUT	Unfiltered DTMF output
12	MUTE	Output active during keying and tone transmission (see note 2)
13	COL1	Connections for 16 button single contact keypad
14	COL2	
15	COL3	
16	ROW1	
17	ROW2	
18	ROW3	
19	ROW4	
20	COL4	

1. MASK may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1 Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA545 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied by the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted.This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start-up time if it was not already running).

	COL 1	COL 2	COL 3	COL 4
ROW 1	1	2	3	TBR
ROW 2	4	5	6	REDIAL
ROW 3	7	8	9	STORE
ROW 4	*	0	#	PAUSE

TBR: Timed Break Recall (Flash). **REDIAL**: Last Number and Memory Redial. **STORE**: Memory Programming.
PAUSE: Insert pause in memory.
TONE (1):Change dialling mode from LD to DTMF
(1) *Only available as a mask option, replacing the PAUSE key. TONE can be used to insert pauses in memory but only during DTMF dialling.*

Fig.2 Keypad layout and connections

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

The dialling mode may be selected via the SELECT pin (pin 2) as detailed in Table 2. Four Loop-Disconnect options are available with different Interdigit pauses and Break/Make ratios, and one DTMF mode. If the DTMF mode is selected then dialling will remain fixed in the DTMF mode. However, if one of the LD modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing either the *, */# or TONE key (depending on the mask variant – see Fig. 2 and page 1-36), provided that dialling is not in progress. If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

SELECT pin to	Dialling mode	IDP (ms)	B/Mratio
V_{SS}	LD	800	2:1
COL 1	LD	500	2:1
COL 2	LD	500	3:2
COL 3	LD	800	3:2
V_{DD}	DTMF	–	–

Table 2 Dialling mode selection

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, the REDIAL key must be pressed twice.

The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the REDIAL key; the remainder of the number will be dialled when the REDIAL key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the *, */#, or TONE key) to DTMF mode, only the digits dialled in LD mode will be retained. This feature is provided to ensure security of PIN (Personal Identification Number) codes. Provided that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently.

Memory Dialling

The MA545 provides 10 memories, each of which has a capacity of 24 digits. The memories can store digits to be dialled in LD, DTMF or Mixed modes and also pauses.

Programming Memories

The MA545 must be 'off-hook' and idle:

1. Press the STORE key.
2. Press the number (0-9) of the memory to be programmed.
3. Enter digits to be stored (no digits will be dialled whilst programming)
4. To finish programming the memory either press the STORE key again or go 'on-hook'.
5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until re-programmed. If any non-valid keys are pressed during programming (e.g. REDIAL,TBR) they will be ignored.

Mixed mode numbers and pauses in memory

Mixed mode (i.e LD + DTMF) numbers are easily programmed into memory. The SELECT pin should be set to one of the LD modes (as it would be when dialling a mixed mode number), then the number entered using the same procedure as if dialling normally. The first press of *, */# or TONE (according to the mask variant) will be stored as a 'change to DTMF', and this will cause all subsequent digits to be sent in DTMF when redialling from memory.

Similarly, pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming.

When redialling from memory, both pauses and LD to DTMF changeovers will cause dialling to halt temporarily until the user presses either the REDIAL or PAUSE key. The exception to this rule is when an LD to DTMF changeover is stored in the first memory location: In this case DTMF dialling will occur immediately when memory dialling is invoked – this allows DTMF codes to be easily stored and sent even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location.

Dialling from memories

The MA545 must be 'off-hook' and idle:

1. Press the REDIAL key once.
2. Press the number (0-9) of the memory to be dialled. Dialling will now start.
3. If dialling halts due to a pause or an LD to DTMF changeover in the memory, further dialling can be resumed by pressing the REDIAL or the PAUSE key. Alternatively, the Column 4 pin can be pulled low (for a minimum of 14 ms) in order to achieve the same result, thus allowing an external timer circuit to be used.

All keypad positions are disabled whilst memory dialling is in progress.

Timed Break & Earth Loop Recall (Flash)

The MA545 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled after the ELR/TBR operation will be retained in the LNR store (1).

A TBR (Flash) of 100ms (2) is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fig. 3, or by use of a double contact switch.

(1) Other options are available, including an option for Danish requirements (see page 1-36). In Denmark, TBR (or ELR) is used to obtain an outside line in PABX use. Under these conditions the LNR store contents will be retained and can be redialled after a TBR or ELR. Digits manually entered after a TBR or ELR will become the new LNR store contents.

(2) Other TBR (Flash) periods are available as mask options (see page 1-36).

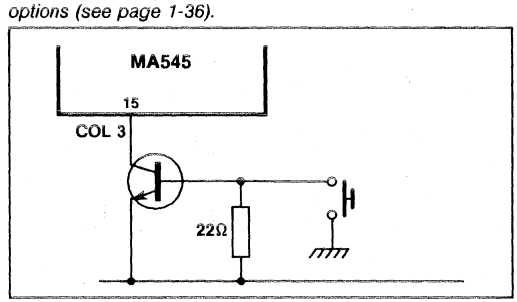


Fig.3 Earth loop recall

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally, the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 6 & 7) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

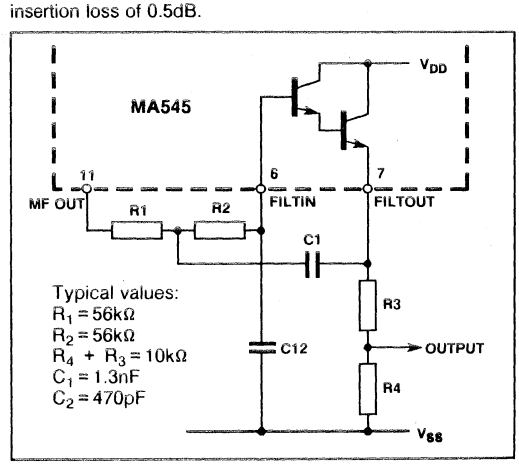


Fig.4 DTMF tone filtering

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The IMP output remains low during tone transmission. The MF OUT output rises to its DC level of 0.9 V_{DD} at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 100ms, the tone output will continue until the key is released.

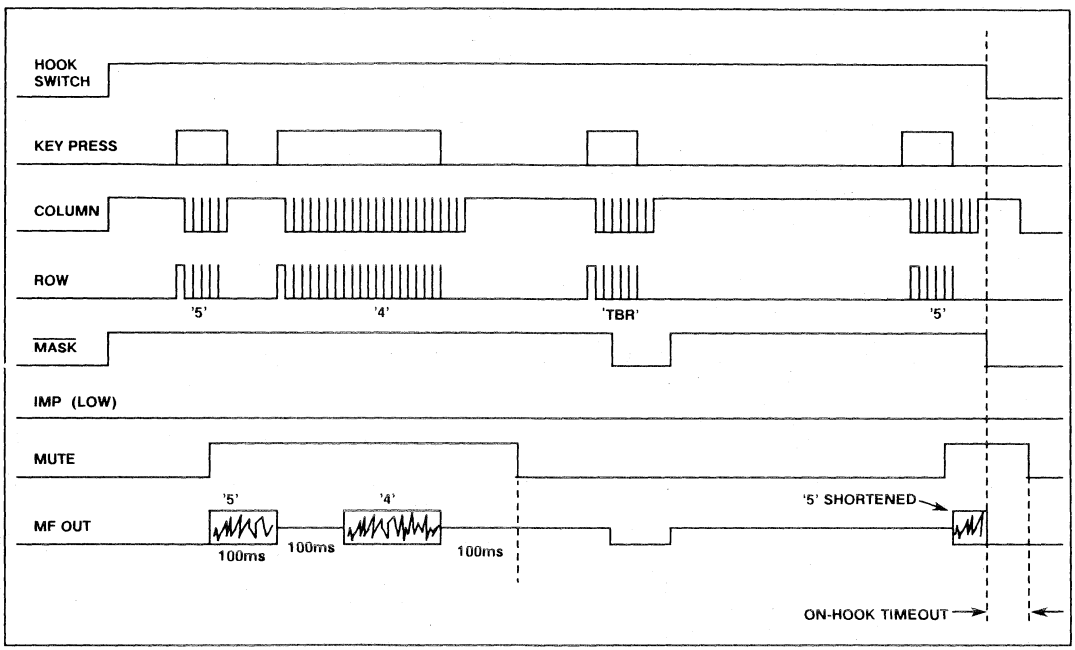


Fig.5 DTMF mode timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	- 0.07	- 0.10	+ 0.19	- 0.15	- 0.17	- 0.20	- 0.22	- 0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 3 Tone frequencies

LOOP-DISCONNECT DIALLING

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic '0' during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling. LD dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

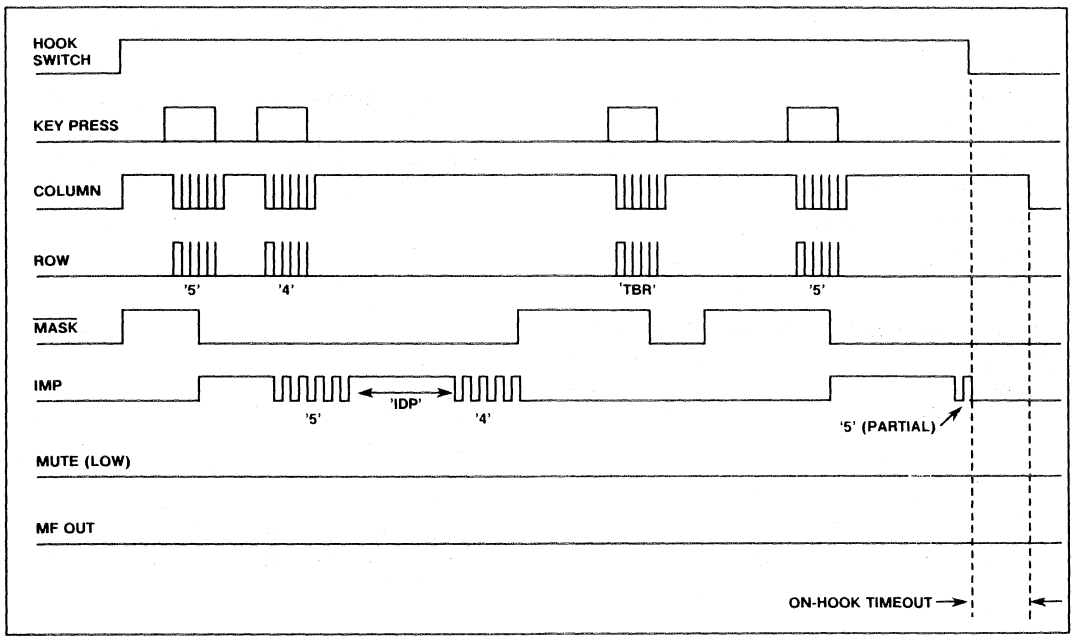


Fig.6 LD mode timing diagram

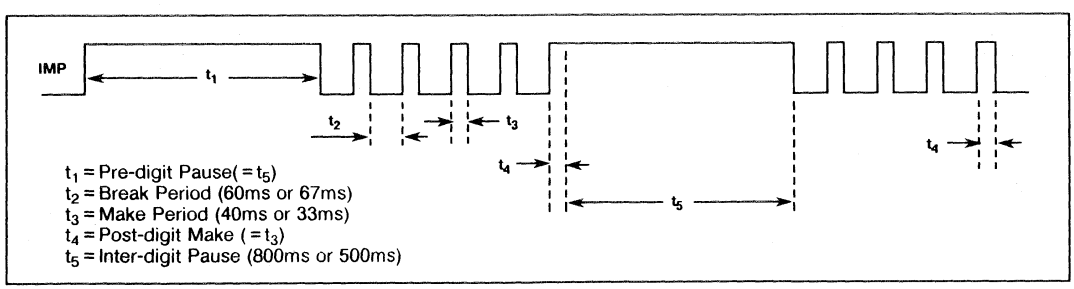


Fig.7 Timing data

MASK OPTIONS

The MA545 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufacture. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit.

The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

1. TBR (Flash) Period
- ***a. 100 ms***
- b. 200 ms
- c. 300 ms
- d. 400 ms
- e. 500 ms
- f. 600 ms

2. LD to DTMF Keypad Switching
- ***a. * and # keys***
- b. TONE key
- c. * key

3. Retention of Post-*/# Digits in LNR Store (DTMF Mode)
- ***a. All digits retained***
- b. Digits before * or # retained.
- c. Digits before * or # retained (except when * or # is first digit).

4. LD dialling options
- ***a. Standard (n = n pulses, except 0 = 10 pulses)***
- b. Swedish (n = (n + 1) pulses)
- c. Norwegian (n = (11-n) pulses)
- d. New Zealand (n = (10-n) pulses)

5. Recall (Flash)/LNR protocol
- ***a. Digits dialled after Recall retained.***
- b. Digits dialled before Recall retained
- c. Recall inhibits LNR
- d. For Danish PABX requirements

6. DTMF Minimum Timings
- ***a. 100ms on, 100ms off***
- b. 73ms on, 73ms off
- c. 73ms on, 147ms off

7. Keypad Options (Key Position COL4, ROW4)
- ***a. PAUSE key***
- b. TONE key (see option 2b)
- c. LNR key (single press, replaces double press of REDIAL)

8. Pin 3
- ***a. $\overline{MASK}$***
- b. MASK

9. Pin 1
- ***a. IMP***
- b. $\overline{IMP}$
- c. [IMP + $\overline{MASK}$]
- d. $\overline{[IMP + \overline{MASK}]}$

10. Pin 12
- ***a. MUTE***
- b. $\overline{MUTE}$

APPLICATION CIRCUITS

Refer to the MA541 data sheet, Figs. 8 and 9, on pages 1-29 and 1-30

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V, T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Supply Current: On-hook		<0.2	5.0	μA	V_{DD} = 2.0V. See note 1.
Off-hook		1.5		μA	MF OUT low
MF tone sending			1.0	mA	
LD impulsing			200	μA	
Output high voltage ($\overline{MASK}$. MUTE and IMP outputs)	2.2			V	I = -1mA
Output low voltage ($\overline{MASK}$, MUTE and IMP outputs)			0.3	V	I = +1mA
MF OUT DC level during tone sending		$0.9V_{DD}$		V	
MF OUT output resistance		3		kΩ	
'Key Pressed' resistance			2	kΩ	$2.5V < V_{DD} < 5.7V$
'Key Not Pressed' resistance	500			kΩ	$2.5V < V_{DD} < 5.7V$
Darlington pair current gain (see Fig. 4)	600	50,000			$I_E = 100\mu A$, $V_{CE} = 2V$

NOTE 1. Specially tested versions with guaranteed lower on-hook supply current are available.

AC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Tone output: low group	57	64		mV rms	No load
high group		81	91	mV rms	No load
High-to-Low group amplitude ratio (pre-emphasis)	1.5	2	2.5	dB	See note 2.
Total harmonic distortion: 0-4 kHz		1.5		%	
0-10 kHz		2.5		%	
0-50 kHz		5.0		%	
0-200 kHz		6.5	10	%	
Oscillator start-up time		<0.1	1	ms	

NOTE 2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition	Min.	Typ.	Max.	Units	Notes
Supply Voltage: On-hook	1.8		5.7	V	For memory retention
Off-hook	2.4		5.7	V	
Hookswitch Input: On-hook			$0.2V_{DD}$	V	
Off-hook	$0.8V_{DD}$			V	
Oscillating frequency		560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}–V_{SS}	-0.3 to +6.5V
Voltage on any pin (except HSW)	V_{SS} - 0.3V to V_{DD} + 0.3V
Voltage on HSW pin (See note 1)	V_{SS} - 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	±1mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	-5 to 0mA
Storage temperature	-55°C to +125°C
Operating temperature range	-10°C to +55°C

NOTES

1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300μA max. no damage will occur.
2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DS3150-1.1
Supersedes CD10701FDS-1.1

MA547 FAMILY

LD/DTMF SWITCHABLE DIALLERS WITH DEDICATED KEYS FOR 10 MEMORIES

The MA547 family are keypad switchable LD/DTMF dialler devices with a last number redial facility and ten 24-digit memories, each with its own dedicated dialling key.

Three operating modes are available: LD only mode, DTMF only mode and LD mode with the ability to switch temporarily to DTMF mode from the keypad during a call. This last mode enables subscribers to access such services as home banking. Mixed LD and DTMF numbers can also be stored in memory. The MA547 devices are pin compatible with the GPS switchable dialler families MA526, MA527, MA541, MA545. MA585, MA587 and MA589 – providing a complete range of telephone features within a single PCB and circuit design. Metal mask and pin selectable options are available to service specific requirements of particular countries and customers.

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- 10×24-Digit Memories, each with Dedicated Key
- 24 Digit Last Number Redial
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Ceramic Resonator
- Battery-less operation - Low Power CMOS
- Mask Programmable Options to suit Application
- Timed Break Recall (Flash) and Earth Recall

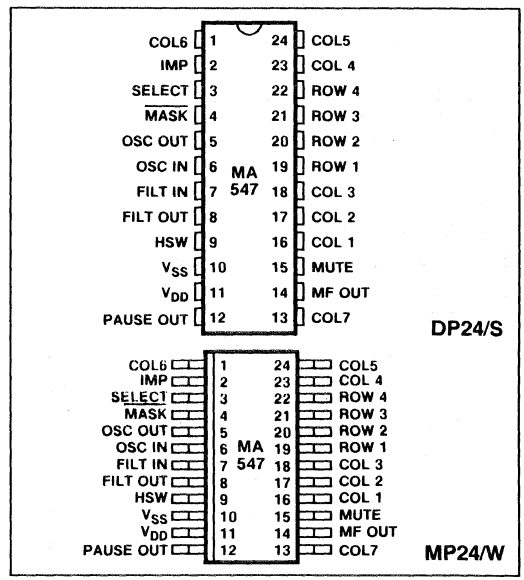


Fig.1 Pin connections - top view. DP24/S: 0.3in 'skinnydip' plastic DIL; MP24/W: wide-bodied Small Outline package.

PIN FUNCTIONS

Pin number	Pin name	Function
2	IMP	'Loop disconnect' dialling output
3	SELECT	LD/DTMF selection, IDP and B/M ratio programming
4	$\overline{\text{MASK}}$	Output to disable speech circuit during pulse dialling and recall (see note 1)
5	OSC OUT	Connections for 560kHz ceramic resonator
6	OSC IN	
7	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
8	FILT OUT	
9	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-Hook'
10	V_{SS}	Negative supply
11	V_{DD}	Positive supply
12	PAUSE OUT	Active high output indicating a pause when dialling from memory
14	MF OUT	Unfiltered DTMF output
15	MUTE	Output active during keying and tone transmission (see note 2)
16	COL1	Connections for 28 key single contact keypad
17	COL2	
18	COL3	
23	COL4	
24	COL5	
1	COL6	
13	COL7	
19	ROW1	
20	ROW2	
21	ROW3	
22	ROW4	

1. $\overline{\text{MASK}}$ may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1 Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA547 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied by the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted.This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start-up time if it was not already running).

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

The dialling mode may be selected via the SELECT pin (pin 3) as detailed in Table 2. Four 'Loop-Disconnect + DTMF options and four 'Loop-Disconnect only' options with different Interdigit pauses and Break/Make ratios are available and one DTMF mode. If one of the 'LD only' modes or the DTMF mode is selected then dialling will remain fixed in LD mode or DTMF mode respectively.

	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7
ROW 1	1	2	3	TBR	S1	S2	S3
ROW 2	4	5	6	LNR	S4	S5	S6
ROW 3	7	8	9	STORE	S7	S8	S9
ROW 4	*	0	#	PAUSE/ CONT	MUTE	S0	

Fig.2a Versions without TONE key

or/# are used to change from LD to DTMF dialling and are available as digits when in DTMF mode.

TBR: Timed Break Recall (Flash).
LNR: Last Number Redial.
STORE: Memory Programming.
PAUSE/CONT: Insert pause in memory/continue dialling.
MUTE: Activate MUTE output .
S0-S9: Dedicated memory dialling keys.
TONE: Change dialling mode from LD to DTMF

	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7
ROW 1	1	2	3	TBR	S1	S2	S3
ROW 2	4	5	6	LNR	S4	S5	S6
ROW 3	7	8	9	STORE	S7	S8	S9
ROW 4	*	0	#	TONE	MUTE	S0	PAUSE/ CONT

Fig.2b Versions with TONE key

Fig.2 Keypad layout and connections

SELECT pin to	Dialling mode	IDP (ms)	B/Mratio
V_{SS}	LD + DTMF	800	2:1
COL 1	LD + DTMF	500	2:1
COL 2	LD + DTMF	500	3:2
COL 3	LD + DTMF	800	3:2
COL 4	LD only	800	2:1
COL 5	LD only	500	2:1
COL 6	LD only	500	3:2
COL 7	LD only	800	3:2
V_{DD}	DTMF	-	-

Table 2 Dialling mode selection

However, if one of the 'LD + DTMF' modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing either the *, */# or TONE key (depending on the mask variant – see Fig. 2 and page 1-43), provided that dialling is not in progress. If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, the LNR key must be pressed once.

The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the LNR key; the remainder of the number will be dialled when the LNR key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the *, */#, or TONE key) to DTMF mode, only the digits dialled in LD mode will be retained. This feature is provided to ensure security of PIN (Personal Identification Number) codes. Provided that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently.

Memory Dialling

The MA547 provides 10 memories, each of which has a capacity of 24 digits and each of which has its own dedicated key. The memories can store digits to be dialled in LD, DTMF or mixed modes and also pauses.

Programming Memories

The MA547 must be 'off-hook' and idle:

1. Press the STORE key.
2. Press the key (S0-S9) of the memory to be programmed.
3. Enter digits to be stored (no digits will be dialled whilst programming)
4. To finish programming the memory either press the STORE key again or go 'on-hook'.
5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until re-programmed. If any non-valid keys are pressed during programming (e.g. LNR,TBR) they will be ignored.

Mixed mode numbers and pauses in memory

Mixed mode (i.e LD + DTMF) numbers are easily programmed into memory. The SELECT pin should be set to one of the 'LD + DTMF' modes (as it would be when dialling a mixed mode number), then the number entered using the same procedure as if dialling normally. The first press of *, */# or TONE (according to the mask variant) will be stored as a 'change to DTMF', and this will cause all subsequent digits to be sent in DTMF when redialling from memory.

Similarly, pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming.

When redialling from memory, both pauses and LD to DTMF changeovers will cause dialling to halt temporarily until the user presses the PAUSE/CONT key. The exception to this rule is when an LD to DTMF changeover is stored in the first memory location: in this case, DTMF dialling will occur immediately when memory dialling is invoked – this allows DTMF codes to be easily stored and sent even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location.

Dialling from memories

The MA547 must be 'off-hook' and idle:

1. Press the appropriate dedicated memory key (S0-S9). Dialling will now start.
2. If dialling halts due to a pause or an LD to DTMF changeover in the memory, the PAUSE OUT pin will go high (logic '1'). Further dialling can be resumed either by pressing the PAUSE/CONT key or, alternatively, the Column 4 pin can be pulled low (for a minimum of 14 ms) to achieve the same result, thus allowing an external timer circuit to be used. The PAUSE/OUT output is reset when dialling resumes.

All keypad positions are disabled whilst memory dialling is in progress.

Timed Break & Earth Loop Recall (Flash)

The MA547 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled after the ELR/TBR operation will be retained in the LNR store [1].

A TBR (Flash) of 100ms [2] is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fig. 3, or by use of a double contact switch.

(1) *Other options are available, including an option for Danish requirements (see page 1-43).. In Denmark, TBR (or ELR) is used to obtain an outside line in PABX use. Under these conditions the LNR store contents will be retained and can be redialled after a TBR or ELR. Digits manually entered after a TBR or ELR will become the new LNR store contents.*

(2) *Other TBR (Flash) periods are available as mask options (see page 1-43).*

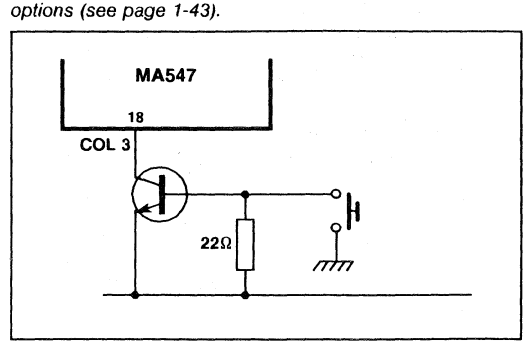


Fig.3 Earth loop recall

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally, the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

Mute Facility

A MUTE facility is provided to allow the user to mute the transmit path (ie. the microphone) while still being able to hear the receive path.

A keypad position is provided for this facility, whenever, and for as long as, the MUTE key is pressed, the MUTE output will be active (logic '1') in order to disable the transmit path of the speech circuit. This is the same action as during DTMF transmission.

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 7 & 8) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

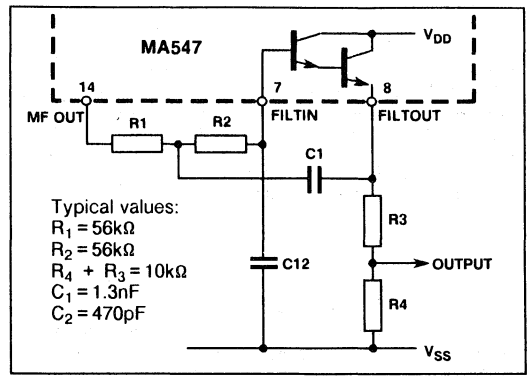


Fig.4 DTMF tone filtering

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission.

The IMP output remains low during tone transmission. The MF OUT output rises to its DC level of 0.9 V_{DD} at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 100ms, the tone output will continue until the key is released.

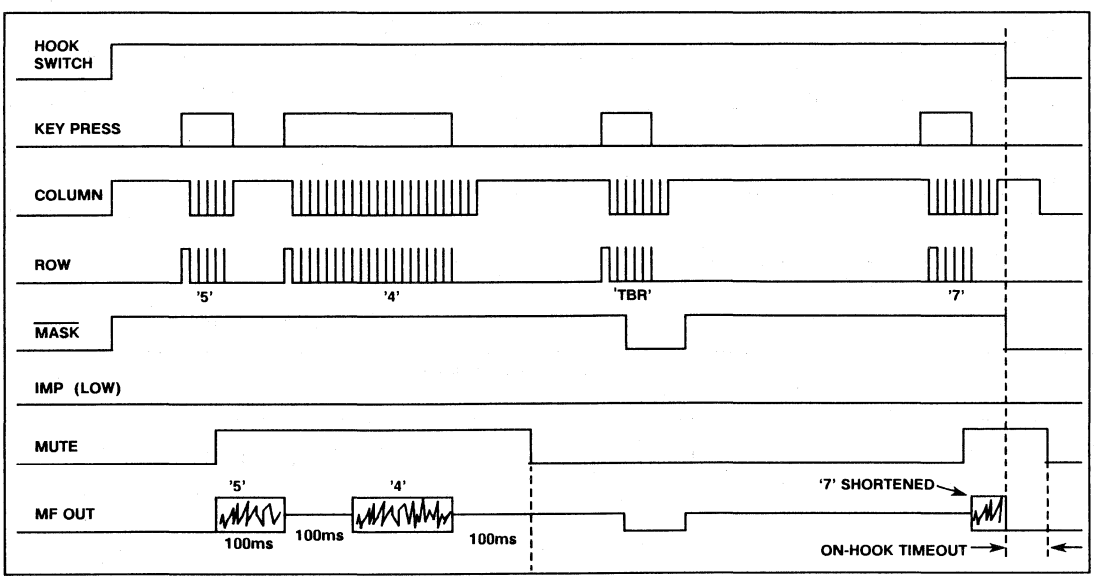


Fig.5 DTMF mode timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	- 0.07	- 0.10	+ 0.19	- 0.15	- 0.17	- 0.20	- 0.22	- 0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 3 Tone frequencies

LOOP-DISCONNECT DIALLING

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic '0' during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling. LD dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

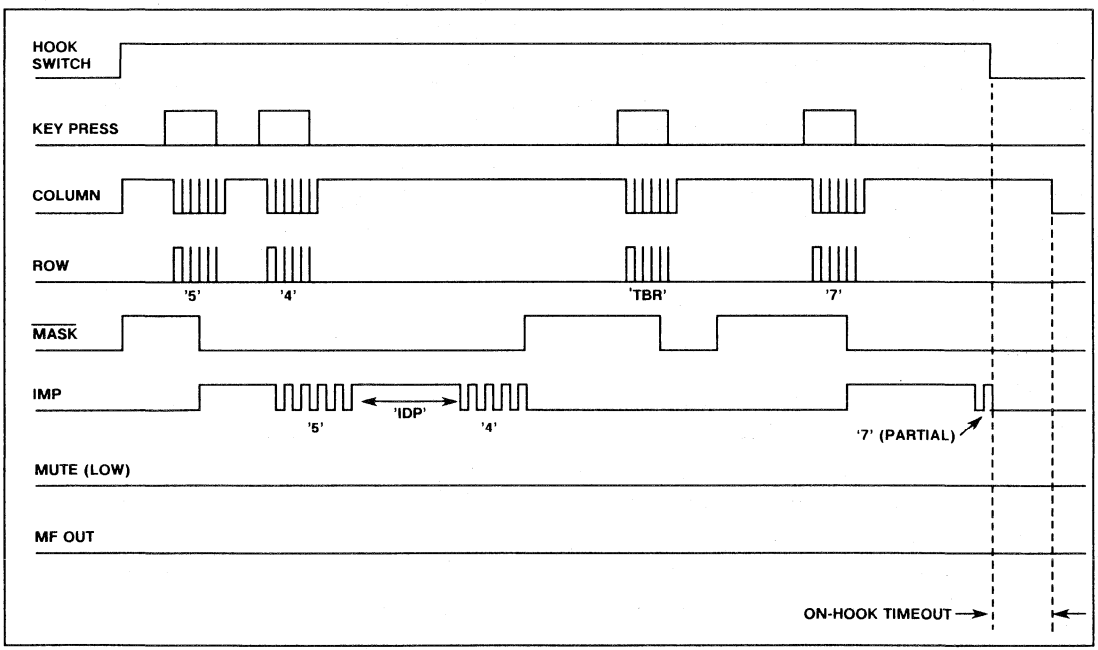


Fig.6 LD mode timing diagram

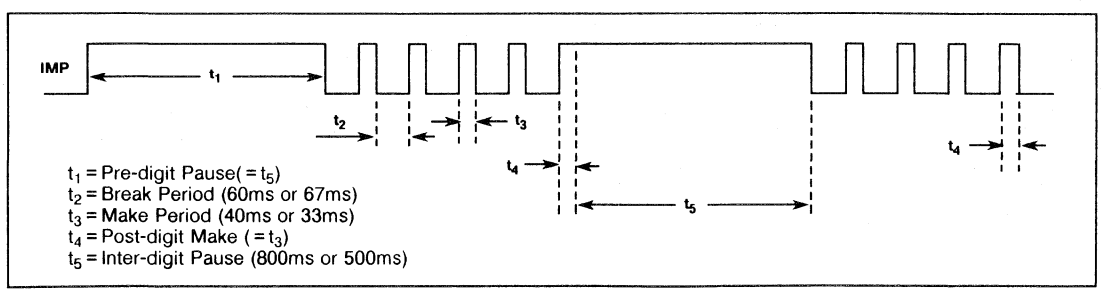


Fig.7 Timing data

MASK OPTIONS

The MA547 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufacture. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit.

The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

1. TBR (Flash) Period
- ***a. 100 ms***
- b. 200 ms
- c. 300 ms
- d. 400 ms
- e. 500 ms
- f. 600 ms

2. LD to DTMF Keypad Switching
- ***a. * and # keys***
- b. TONE key
- c. * key

3. Retention of Post-*/# Digits in LNR Store (DTMF Mode)
- ***a. All digits retained***
- b. Digits before * or # retained.
- c. Digits before * or # retained (except when * or # is first digit).

4. LD dialling options
- ***a. Standard (n = n pulses, except 0 = 10 pulses)***
- b. Swedish (n = (n + 1) pulses)
- c. Norwegian (n = (11-n) pulses)
- d. New Zealand (n = (10-n) pulses)

5. Recall (Flash)/LNR protocol
- ***a. Digits dialled after Recall retained.***
- b. Digits dialled before Recall retained
- c. Recall inhibits LNR
- d. For Danish PABX requirements

6. DTMF Minimum Timings
- ***a. 100ms on, 100ms off***
- b. 73ms on, 73ms off
- c. 73ms on, 147ms off

7. Pin 4
- ***a. $\overline{\text{MASK}}$***
- b. MASK

8. Pin 2
- ***a. IMP***
- b. $\overline{\text{IMP}}$
- c. [IMP + $\overline{\text{MASK}}$]
- d. $\overline{\text{[IMP + MASK]}}$

9. Pin 15
- ***a. MUTE***
- b. $\overline{\text{MUTE}}$

APPLICATION CIRCUITS

Refer to the MA541 data sheet, Figs. 8 and 9, on pages 1-29 and 1-30

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V, T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Supply Current: On-hook		<0.2	5.0	μA	V_{DD} = 2.0V. See note 1.
Off-hook		1.5		μA	MF OUT low
MF tone sending			1.0	mA	
LD impulsing			200	μA	
Output high voltage (MASK. MUTE and IMP outputs)	2.2			V	I = -1mA
Output low voltage (MASK, MUTE and IMP outputs)			0.3	V	I = +1mA
MF OUT DC level during tone sending		$0.9V_{DD}$		V	
MF OUT output resistance		3		kΩ	
'Key Pressed' resistance			2	kΩ	$2.5V < V_{DD} < 5.7V$
'Key Not Pressed' resistance	500			kΩ	$2.5V < V_{DD} < 5.7V$
Darlington pair current gain (see Fig. 4)	600	50,000			$I_E = 100\mu A$, $V_{CE} = 2V$

NOTE 1. Specially tested versions with guaranteed lower on-hook supply current are available.

AC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Tone output: low group	57	64		mV rms	No load
high group		81	91	mV rms	No load
High-to-Low group amplitude ratio (pre-emphasis)	1.5	2	2.5	dB	See note 2.
Total harmonic distortion: 0-4 kHz		1.5		%	
0-10 kHz		2.5		%	
0-50 kHz		5.0		%	
0-200 kHz		6.5	10	%	
Oscillator start-up time		<0.1	1	ms	

NOTE 2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition	Min.	Typ.	Max.	Units	Notes
Supply Voltage: On-hook	1.8		5.7	V	For memory retention
Off-hook	2.4		5.7	V	
Hookswitch Input: On-hook			$0.2V_{DD}$	V	
Off-hook	$0.8V_{DD}$			V	
Oscillating frequency		560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}–V_{SS}	−0.3 to +6.5V
Voltage on any pin (except HSW)	V_{SS} − 0.3V to V_{DD} + 0.3V
Voltage on HSW pin (See note 1)	V_{SS} − 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	±1mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	−5 to 0mA
Storage temperature	−55°C to +125°C
Operating temperature range	−10°C to +55°C

NOTES

1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300μA max. no damage will occur.
2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DS3151-1.0
Supersedes CD10703FDS-1.1

MA585 FAMILY

LD/DTMF SWITCHABLE DIALLERS WITH 20 MEMORIES

The MA585 family are keypad switchable LD/DTMF dialler devices with a last number redial facility and twenty 24-digit memories.

Two operating modes are available: LD mode, with the ability to temporarily switch to DTMF mode from the keypad during a call, and DTMF only mode. The former mode enables subscribers to access such services as home banking. Mixed LD and DTMF numbers can also be stored in memory.

The MA585 devices are pin compatible with the GPS switchable dialler families MA526, MA527, MA541, MA545, MA547. MA587 and MA589 – providing a complete range of telephone features within a single PCB and circuit design.

Metal mask and pin selectable options are available to service specific requirements of particular countries and customers.

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- 24 Digit Last Number Redial
- 20 x 24-Digit Memories
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Ceramic Resonator
- Battery-less operation - Low Power CMOS
- Mask Programmable Options to suit Application
- Timed Break Recall (Flash) and Earth Recall

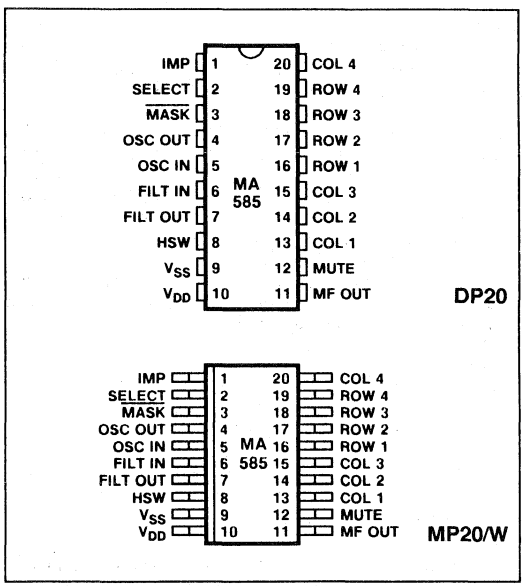


Fig.1 Pin connections - top view (not to scale)

PIN FUNCTIONS

Pin number	Pin name	Function
1	IMP	'Loop disconnect' dialling output
2	SELECT	LD/DTMF selection, IDP and B/M ratio programming
3	$\overline{\text{MASK}}$	Output to disable speech circuit during pulse dialling and recall (see note 1)
4	OSC OUT	Connections for 560kHz ceramic resonator
5	OSC IN	
6	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
7	FILT OUT	
8	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-Hook'
9	V_{SS}	Negative supply
10	V_{DD}	Positive supply
11	MF OUT	Unfiltered DTMF output
12	MUTE	Output active during keying and tone transmission (see note 2)
13	COL1	Connections for 16 button single contact keypad
14	COL2	
15	COL3	
16	ROW1	
17	ROW2	
18	ROW3	
19	ROW4	
20	COL4	

1. $\overline{\text{MASK}}$ may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1 Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA585 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied by the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted. This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start-up time if it was not already running).

	COL 1	COL 2	COL 3	COL 4
ROW 1	1	2	3	TBR
ROW 2	4	5	6	REDIAL
ROW 3	7	8	9	STORE
ROW 4	*	0	#	PAUSE

TBR: Timed Break Recall (Flash). **REDIAL**: Last Number and Memory Redial. **STORE**: Memory Programming.
PAUSE: Insert pause in memory.
TONE (1):Change dialling mode from LD to DTMF
(1) *Only available as a mask option, replacing the PAUSE key. TONE can be used to insert pauses in memory but only during DTMF dialling.*

Fig.2 Keypad layout and connections

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

The dialling mode may be selected via the SELECT pin (pin 2) as detailed in Table 2. Four Loop-Disconnect options are available with different Interdigit pauses and Break/Make ratios, and one DTMF mode. If the DTMF mode is selected then dialling will remain fixed in the DTMF mode. However, if one of the LD modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing either the *, */# or TONE key (depending on the mask variant – see Fig. 2 and page 1-50), provided that dialling is not in progress. If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

SELECT pin to	Dialling mode	IDP (ms)	B/Mratio
V_{SS}	LD	800	2:1
COL 1	LD	500	2:1
COL 2	LD	500	3:2
COL 3	LD	800	3:2
V_{DD}	DTMF	–	–

Table 2 Dialling mode selection

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, the REDIAL key must be pressed twice.

The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the REDIAL key; the remainder of the number will be dialled when the REDIAL key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the *, */#, or TONE key) to DTMF mode, only the digits dialled in LD mode will be retained. This feature is provided to ensure security of PIN (Personal Identification Number) codes. Provided that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently.

Memory Dialling

The MA585 provides 20 memories, each of which has a capacity of 24 digits. The memories can store digits to be dialled in LD, DTMF or Mixed modes and also pauses.

Programming Memories

The MA585 must be 'off-hook' and idle:

1. Press the STORE key.
2. Press two digits (00-19) indicating the number of the memory to be programmed.
3. Enter digits to be stored (no digits will be dialled whilst programming)
4. To finish programming the memory either press the STORE key again or go 'on-hook'.
5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until re-programmed. If any non-valid keys are pressed during programming (e.g. REDIAL,TBR) they will be ignored.

Mixed mode numbers and pauses in memory

Mixed mode (i.e LD + DTMF) numbers are easily programmed into memory. The SELECT pin should be set to one of the LD modes (as it would be when dialling a mixed mode number), then the number entered using the same procedure as if dialling normally. The first press of *, */# or TONE (according to the mask variant) will be stored as a 'change to DTMF', and this will cause all subsequent digits to be sent in DTMF when redialling from memory.

Similarly, pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming.

When redialling from memory, both pauses and LD to DTMF changeovers will cause dialling to halt temporarily until the user presses either the REDIAL or PAUSE key. The exception to this rule is when an LD to DTMF changeover is stored in the first memory location: In this case DTMF dialling will occur immediately when memory dialling is invoked – this allows DTMF codes to be easily stored and sent even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location.

Dialling from memories

The MA585 must be 'off-hook' and idle:

1. Press the REDIAL key once.
2. Press two digits (00-19) indicating the number of the memory to be dialled. Dialling will now start.
3. If dialling halts due to a pause or an LD to DTMF changeover in the memory, further dialling can be resumed by pressing the REDIAL or the PAUSE key. Alternatively, the Column 4 pin can be pulled low (for a minimum of 14 ms) in order to achieve the same result, thus allowing an external timer circuit to be used.

All keypad positions are disabled whilst memory dialling is in progress.

Timed Break & Earth Loop Recall (Flash)

The MA585 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled after the ELR/TBR operation will be retained in the LNR store (1).

A TBR (Flash) of 100ms (2) is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fig. 3, or by use of a double contact switch.

(1) Other options are available, including an option for Danish requirements (see page 1-50). In Denmark, TBR (or ELR) is used to obtain an outside line in PABX use. Under these conditions the LNR store contents will be retained and can be redialled after a TBR or ELR. Digits manually entered after a TBR or ELR will become the new LNR store contents.

(2) Other TBR (Flash) periods are available as mask options (see page 1-50).

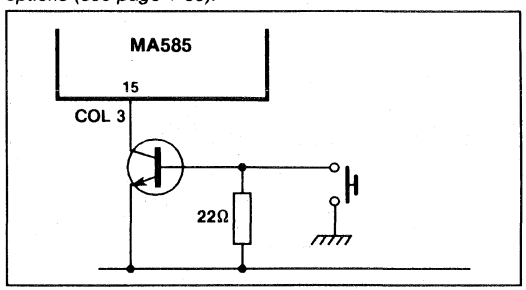


Fig.3 Earth loop recall

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally, the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 6 & 7) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

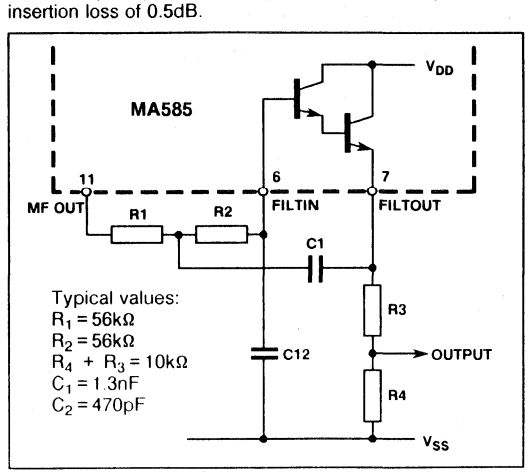


Fig.4 DTMF tone filtering

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The IMP output remains low during tone transmission. The MF OUT output rises to its DC level of 0.9 V_{DD} at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 100ms, the tone output will continue until the key is released.

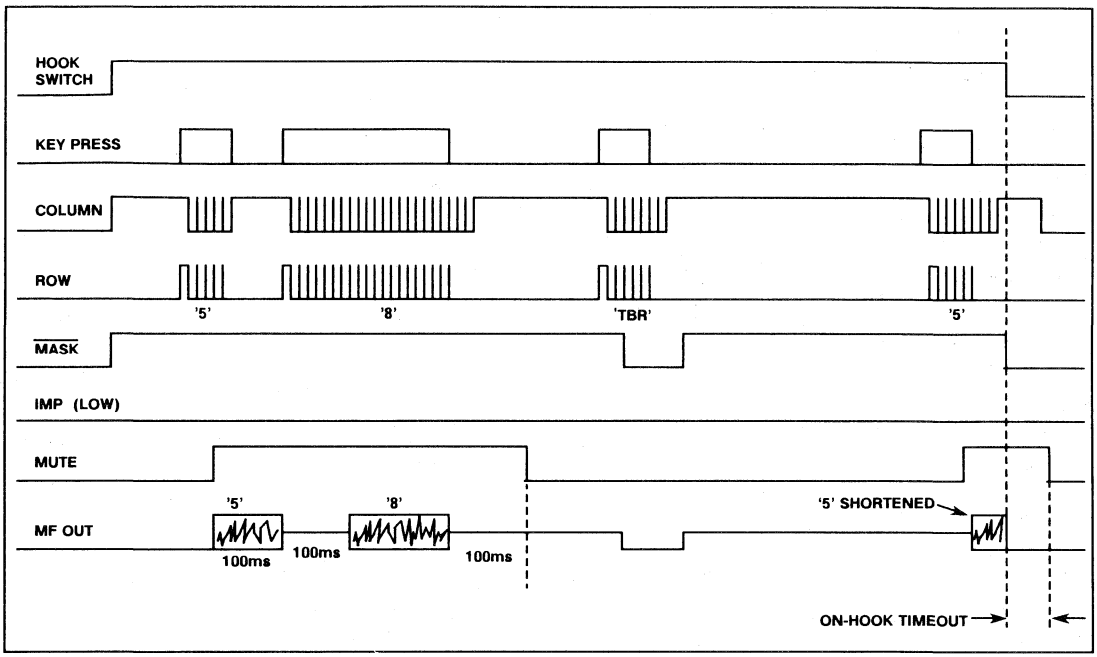


Fig.5 DTMF mode timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	- 0.07	- 0.10	+ 0.19	- 0.15	- 0.17	- 0.20	- 0.22	- 0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 3 Tone frequencies

LOOP-DISCONNECT DIALLING

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic '0' during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling. LD dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

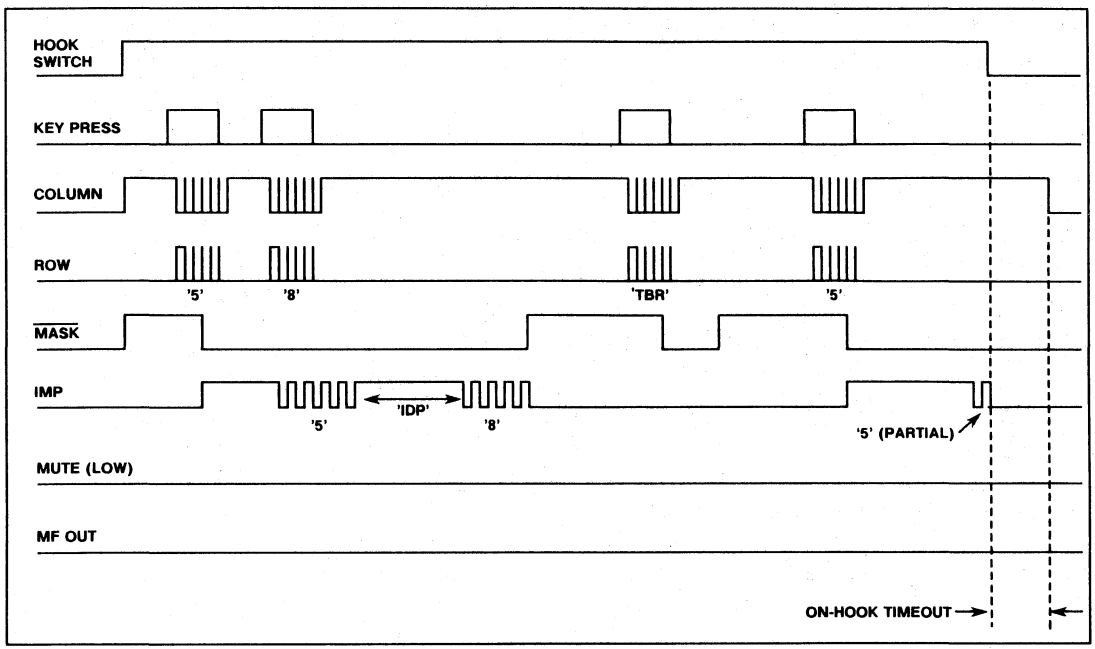


Fig.6 LD mode timing diagram

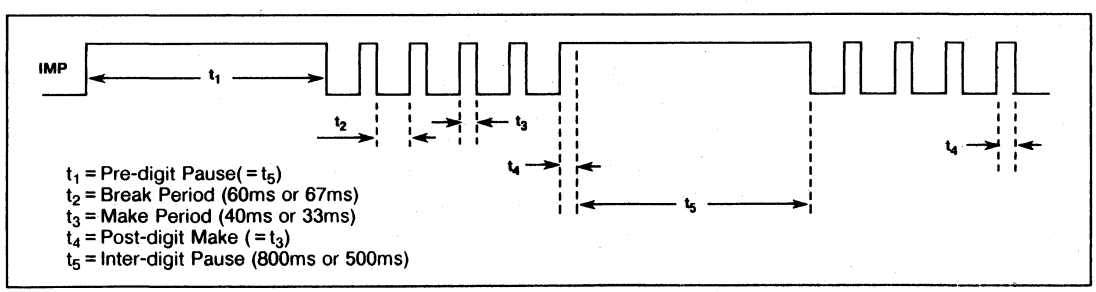


Fig.7 Timing data

MASK OPTIONS

The MA585 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufacture. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit.

The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

1. TBR (Flash) Period
- ***a. 100 ms***
- b. 200 ms
- c. 300 ms
- d. 400 ms
- e. 500 ms
- f. 600 ms

2. LD to DTMF Keypad Switching
- ***a. * and # keys***
- b. TONE key
- c. * key

3. Retention of Post-*/# Digits in LNR Store (DTMF Mode)
- ***a. All digits retained***
- b. Digits before * or # retained.
- c. Digits before * or # retained (except when * or # is first digit).

4. LD dialling options
- ***a. Standard (n = n pulses, except 0 = 10 pulses)***
- b. Swedish (n = (n + 1) pulses)
- c. Norwegian (n = (11-n) pulses)
- d. New Zealand (n = (10-n) pulses)

5. Recall (Flash)/LNR protocol
- ***a. Digits dialled after Recall retained.***
- b. Digits dialled before Recall retained
- c. Recall inhibits LNR
- d. For Danish PABX requirements

6. DTMF Minimum Timings
- ***a. 100ms on, 100ms off***
- b. 73ms on, 73ms off
- c. 73ms on, 147ms off

7. Keypad Options (Key Position COL4, ROW4)
- ***a. PAUSE key***
- b. TONE key (see option 2b)
- c. LNR key (single press, replaces double press of REDIAL)

8. Pin 3
- ***a. $\overline{\text{MASK}}$***
- b. MASK

9. Pin 1
- ***a. IMP***
- b. $\overline{\text{IMP}}$
- c. [IMP + $\overline{\text{MASK}}$]
- d. $\overline{\text{[IMP + MASK]}}$

10. Pin 12
- ***a. $\overline{\text{MUTE}}$***
- b. $\overline{\text{MUTE}}$

APPLICATION CIRCUITS

Refer to the MA541 data sheet, Figs. 8 and 9, on pages 1-29 and 1-30

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V, T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Supply Current: On-hook		<0.2	5.0	μA	V_{DD} = 2.0V. See note 1.
Off-hook		1.5		μA	MF OUT low
MF tone sending			1.0	mA	
LD impulsing			200	μA	
Output high voltage ($\overline{\text{MASK}}$, MUTE and IMP outputs)	2.2			V	I = -1mA
Output low voltage ($\overline{\text{MASK}}$, MUTE and IMP outputs)			0.3	V	I = +1mA
MF OUT DC level during tone sending		$0.9V_{DD}$		V	
MF OUT output resistance		3		kΩ	
'Key Pressed' resistance			2	kΩ	$2.5V < V_{DD} < 5.7V$
'Key Not Pressed' resistance	500			kΩ	$2.5V < V_{DD} < 5.7V$
Darlington pair current gain (see Fig. 4)	600	50,000			$I_E = 100\mu A$, $V_{CE} = 2V$

NOTE 1. Specially tested versions with guaranteed lower on-hook supply current are available.

AC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Tone output: low group	57	64		mV rms	No load
high group		81	91	mV rms	No load
High-to-Low group amplitude ratio (pre-emphasis)	1.5	2	2.5	dB	See note 2.
Total harmonic distortion: 0-4 kHz		1.5		%	
0-10 kHz		2.5		%	
0-50 kHz		5.0		%	
0-200 kHz		6.5	10	%	
Oscillator start-up time		<0.1	1	ms	

NOTE 2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition	Min.	Typ.	Max.	Units	Notes
Supply Voltage: On-hook	1.8		5.7	V	For memory retention
Off-hook	2.4		5.7	V	
Hookswitch Input: On-hook			$0.2V_{DD}$	V	
Off-hook	$0.8V_{DD}$			V	
Oscillating frequency		560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}–V_{SS}	−0.3 to +6.5V
Voltage on any pin (except HSW)	V_{SS} − 0.3V to V_{DD} + 0.3V
Voltage on HSW pin (See note 1)	V_{SS} − 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	±1mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	−5 to 0mA
Storage temperature	−55°C to +125°C
Operating temperature range	−10°C to +55°C

NOTES

1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300μA max. no damage will occur.
2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DS3152-1.1
Supersedes CD10704FDS-1.1

MA587 FAMILY

LD/DTMF SWITCHABLE DIALLERS WITH 20 MEMORIES (10 DEDICATED MEMORY KEYS)

The MA587 family are keypad switchable LD/DTMF dialler devices with a last number redial facility and twenty 24-digit memories, accessible via 10 dedicated dialling keys. Three operating modes are available: LD only mode, DTMF only mode and LD mode with the ability to switch temporarily to DTMF mode from the keypad during a call. This last mode enables subscribers to access such services as home banking. Mixed LD and DTMF numbers can also be stored in memory. The MA587 devices are pin compatible with the GPS switchable dialler families MA526, MA527, MA541, MA545. MA547, MA585 and MA589 – providing a complete range of telephone features within a single PCB and circuit design. Metal mask and pin selectable options are available to service specific requirements of particular countries and customers.

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- 20 x 24-Digit Memories, (10 Dedicated Keys)
- 24 Digit Last Number Redial
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Ceramic Resonator
- Battery-less operation - Low Power CMOS
- Mask Programmable Options to suit Application
- Timed Break Recall (Flash) and Earth Recall

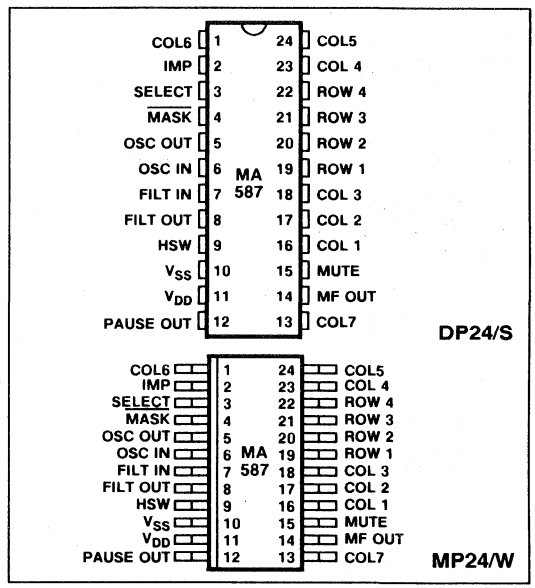


Fig.1 Pin connections - top view. DP24/S: 0.3in 'skinnydip' plastic DIL; MP24/W: wide-bodied Small Outline package.

PIN FUNCTIONS

Pin number	Pin name	Function
2	IMP	'Loop disconnect' dialling output
3	SELECT	LD/DTMF selection, IDP and B/M ratio programming
4	MASK	Output to disable speech circuit during pulse dialling and recall (see note 1)
5	OSC OUT	Connections for 560kHz ceramic resonator
6	OSC IN	
7	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
8	FILT OUT	
9	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-Hook'
10	V_{SS}	Negative supply
11	V_{DD}	Positive supply
12	PAUSE OUT	Active high output indicating a pause when dialling from memory
14	MF OUT	Unfiltered DTMF output
15	MUTE	Output active during keying and tone transmission (see note 2)
16	COL1	Connections for 28 key single contact keypad
17	COL2	
18	COL3	
23	COL4	
24	COL5	
1	COL6	
13	COL7	
19	ROW1	
20	ROW2	
21	ROW3	
22	ROW4	

1. MASK may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1 Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA587 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied by the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted.This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start-up time if it was not already running).

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

The dialling mode may be selected via the SELECT pin (pin 3) as detailed in Table 2. Four 'Loop-Disconnect + DTMF options and four 'Loop-Disconnect only' options with different Interdigit pauses and Break/Make ratios are available and one DTMF mode. If one of the 'LD only' modes or the DTMF mode is selected then dialling will remain fixed in LD mode or DTMF mode respectively.

	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7
ROW 1	1	2	3	TBR	S1	S2	S3
ROW 2	4	5	6	LNR	S4	S5	S6
ROW 3	7	8	9	STORE	S7	S8	S9
ROW 4	*	0	#	PAUSE/ CONT	SHIFT	S0	

Fig.2a Versions without TONE key

or/# are used to change from LD to DTMF dialling and are available as digits when in DTMF mode.

TBR: Timed Break Recall (Flash).
LNR: Last Number Redial.
STORE: Memory Programming.
PAUSE/CONT: Insert pause in memory/continue dialling.
SHIFT: Used in conjunction with the 10 dedicated memory keys, allows all 20 memories to be addressed.
S0-S9: Dedicated memory dialling keys.
TONE: Change dialling mode from LD to DTMF

	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7
ROW 1	1	2	3	TBR	S1	S2	S3
ROW 2	4	5	6	LNR	S4	S5	S6
ROW 3	7	8	9	STORE	S7	S8	S9
ROW 4	*	0	#	TONE	SHIFT	S0	PAUSE/ CONT

Fig.2b Versions with TONE key

Fig.2 Keypad layout and connections

SELECT pin to	Dialling mode	IDP (ms)	B/Mratio
V_{SS}	LD + DTMF	800	2:1
COL 1	LD + DTMF	500	2:1
COL 2	LD + DTMF	500	3:2
COL 3	LD + DTMF	800	3:2
COL 4	LD only	800	2:1
COL 5	LD only	500	2:1
COL 6	LD only	500	3:2
COL 7	LD only	800	3:2
V_{DD}	DTMF	–	–

Table 2 Dialling mode selection

However, if one of the 'LD + DTMF' modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing either the *, */# or TONE key (depending on the mask variant – see Fig. 2 and page 1-57), provided that dialling is not in progress. If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, the LNR key must be pressed once.

The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the LNR key; the remainder of the number will be dialled when the LNR key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the *, */#, or TONE key) to DTMF mode, only the digits dialled in LD mode will be retained. This feature is provided to ensure security of PIN (Personal Identification Number) codes. Provided that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently.

Memory Dialling

The MA587 provides 20 memories, each of which has a capacity of 24 digits. There are 10 dedicated memory keys and a SHIFT key which allows all 20 memories to be addressed by the 10 memory keys. The memories can store digits to be dialled in LD, DTMF or mixed modes and also pauses.

Programming Memories

The MA587 must be 'off-hook' and idle:

1. Press the STORE key.
2. Press key S0-S9 or SHIFT + S0-S9 indicating the memory to be programmed.
3. Enter digits to be stored (no digits will be dialled whilst programming)
4. To finish programming the memory either press the STORE key again or go 'on-hook'.
5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until re-programmed. If any non-valid keys are pressed during programming (e.g. LNR,TBR) they will be ignored.

Mixed mode numbers and pauses in memory

Mixed mode (i.e LD + DTMF) numbers are easily programmed into memory. The SELECT pin should be set to one of the 'LD + DTMF' modes (as it would be when dialling a mixed mode number), then the number entered using the same procedure as if dialling normally. The first press of *, */# or TONE (according to the mask variant) will be stored as a 'change to DTMF', and this will cause all subsequent digits to be sent in DTMF when redialling from memory.

Similarly, pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming.

When redialling from memory, both pauses and LD to DTMF changeovers will cause dialling to halt temporarily until the user presses the PAUSE/CONT key. The exception to this rule is when an LD to DTMF changeover is stored in the first memory location: in this case, DTMF dialling will occur immediately when memory dialling is invoked – this allows DTMF codes to be easily stored and sent even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location.

Dialling from memories

The MA587 must be 'off-hook' and idle:

1. Press the appropriate memory key S0-S9 or SHIFT + S0-S9. Dialling will now start.
2. If dialling halts due to a pause or an LD to DTMF changeover in the memory, the PAUSE OUT pin will go high (logic '1'). Further dialling can be resumed either by pressing the PAUSE/CONT key or, alternatively, the Column 4 pin can be pulled low (for a minimum of 14 ms) to achieve the same result, thus allowing an external timer circuit to be used. The PAUSE/OUT output is reset when dialling resumes.

All keypad positions are disabled whilst memory dialling is in progress.

Timed Break & Earth Loop Recall (Flash)

The MA587 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled after the ELR/TBR operation will be retained in the LNR store (1).

A TBR (Flash) of 100ms (2) is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fig. 3, or by use of a double contact switch.

(1) *Other options are available, including an option for Danish requirements (see page 1-57).. In Denmark, TBR (or ELR) is used to obtain an outside line in PABX use. Under these conditions the LNR store contents will be retained and can be redialled after a TBR or ELR. Digits manually entered after a TBR or ELR will become the new LNR store contents.*

(2) *Other TBR (Flash) periods are available as mask options (see page 1-57).*

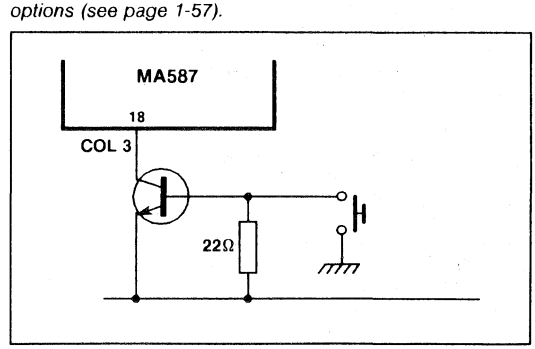


Fig.3 Earth loop recall

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally, the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 7 & 8) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

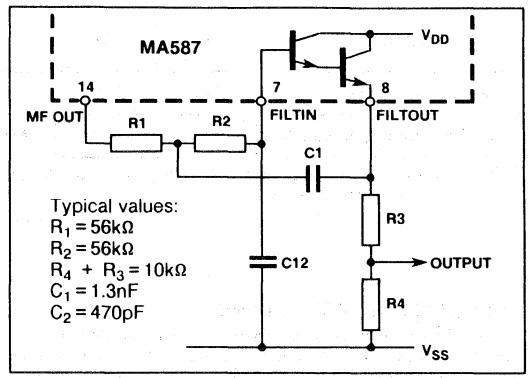


Fig.4 DTMF tone filtering

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission.

The IMP output remains low during tone transmission. The MF OUT output rises to its DC level of 0.9 V_{DD} at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 100ms, the tone output will continue until the key is released.

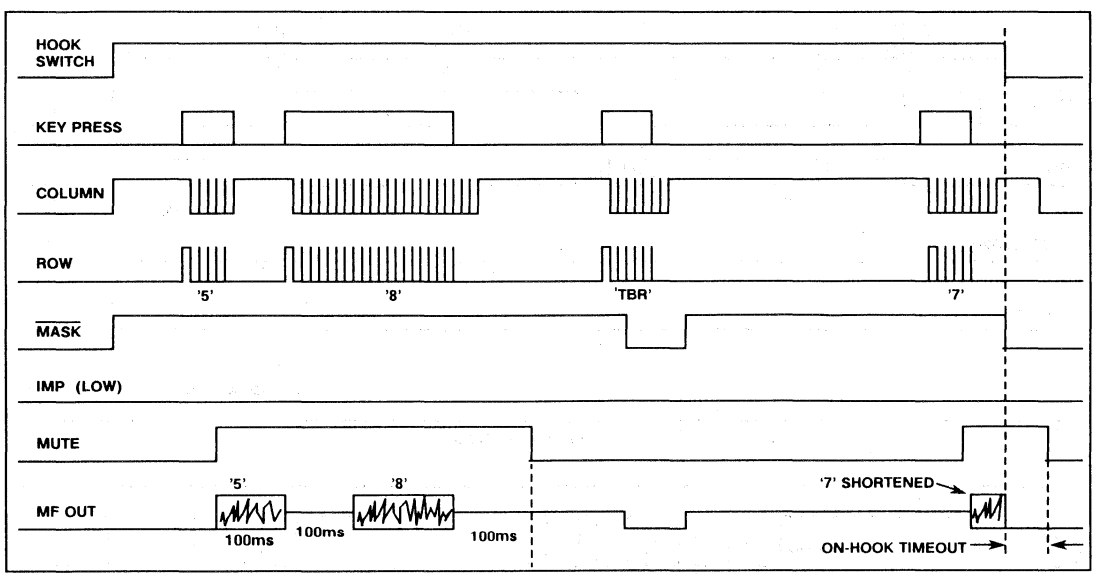


Fig.5 DTMF mode timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	- 0.07	- 0.10	+ 0.19	- 0.15	- 0.17	- 0.20	- 0.22	- 0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 3 Tone frequencies

LOOP-DISCONNECT DIALLING

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic '0' during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling. LD dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

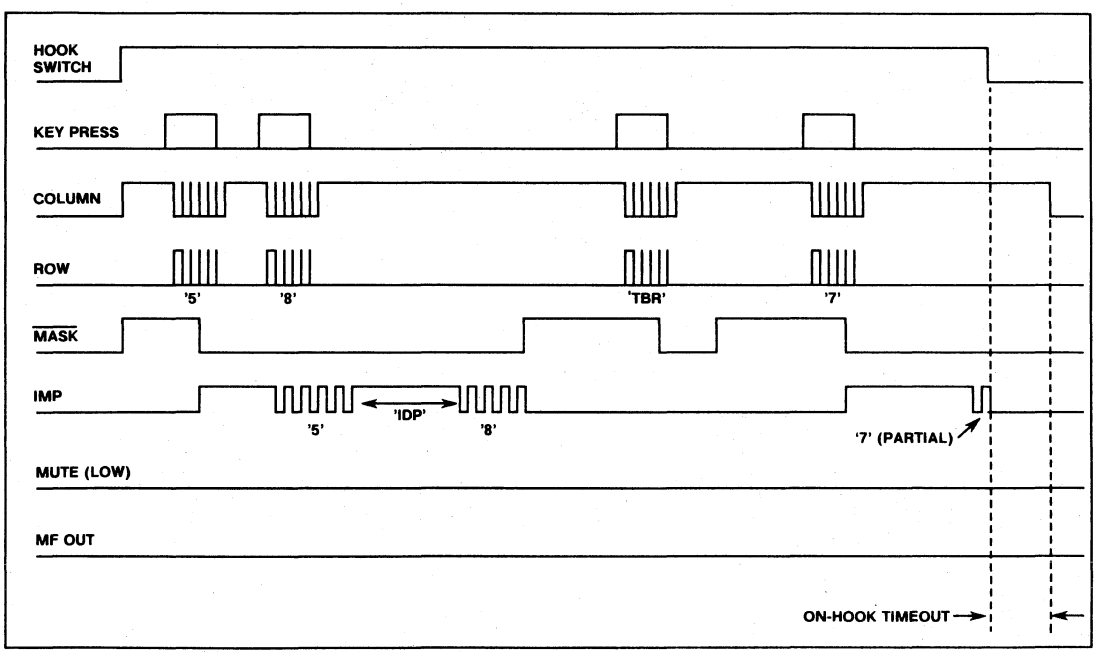


Fig.6 LD mode timing diagram

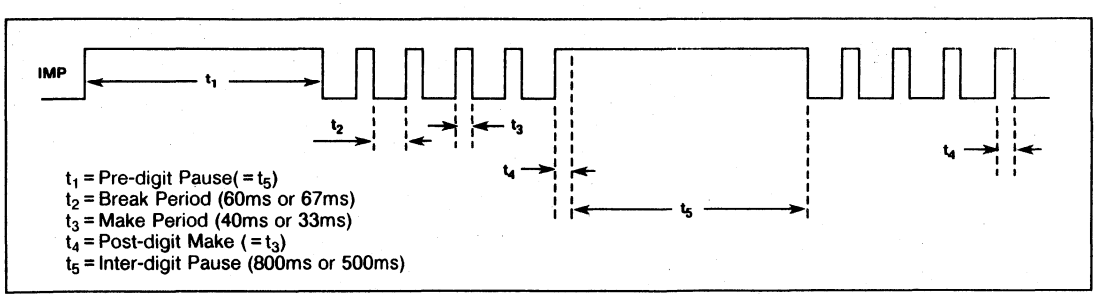


Fig.7 Timing data

MASK OPTIONS

The MA587 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufacture. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit.

The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

1. TBR (Flash) Period
- ***a. 100 ms***
- b. 200 ms
- c. 300 ms
- d. 400 ms
- e. 500 ms
- f. 600 ms

2. LD to DTMF Keypad Switching
- ***a. * and # keys***
- b. TONE key
- c. * key

3. Retention of Post-*/# Digits in LNR Store (DTMF Mode)
- ***a. All digits retained***
- b. Digits before * or # retained.
- c. Digits before * or # retained (except when * or # is first digit).

4. LD dialling options
- ***a. Standard (n = n pulses, except 0 = 10 pulses)***
- b. Swedish (n = (n + 1) pulses)
- c. Norwegian (n = (11-n) pulses)
- d. New Zealand (n = (10-n) pulses)

5. Recall (Flash)/LNR protocol
- ***a. Digits dialled after Recall retained.***
- b. Digits dialled before Recall retained
- c. Recall inhibits LNR
- d. For Danish PABX requirements

6. DTMF Minimum Timings
- ***a. 100ms on, 100ms off***
- b. 73ms on, 73ms off
- c. 73ms on, 147ms off

7. Pin 4
- ***a. $\overline{\text{MASK}}$***
- b. MASK

8. Pin 2
- ***a. IMP***
- b. $\overline{\text{IMP}}$
- c. [IMP + $\overline{\text{MASK}}$]
- d. $\overline{\text{[IMP + MASK]}}$

9. Pin 15
- ***a. MUTE***
- b. $\overline{\text{MUTE}}$

APPLICATION CIRCUITS

Refer to the MA541 data sheet, Figs. 8 and 9, on pages 1-29 and 1-30

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V, T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Supply Current: On-hook		<0.2	5.0	μA	V_{DD} = 2.0V. See note 1.
Off-hook		1.5		μA	MF OUT low
MF tone sending			1.0	mA	
LD impulsing			200	μA	
Output high voltage ($\overline{MASK}$. MUTE and IMP outputs)	2.2			V	I = -1mA
Output low voltage ($\overline{MASK}$, MUTE and IMP outputs)			0.3	V	I = +1mA
MF OUT DC level during tone sending		$0.9V_{DD}$		V	
MF OUT output resistance		3		kΩ	
'Key Pressed' resistance			2	kΩ	$2.5V < V_{DD} < 5.7V$
'Key Not Pressed' resistance	500			kΩ	$2.5V < V_{DD} < 5.7V$
Darlington pair current gain (see Fig. 4)	600	50,000			$I_E = 100\mu A$, $V_{CE} = 2V$

NOTE 1. Specially tested versions with guaranteed lower on-hook supply current are available.

AC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Tone output: low group	57	64		mV rms	No load
high group		81	91	mV rms	No load
High-to-Low group amplitude ratio (pre-emphasis)	1.5	2	2.5	dB	See note 2.
Total harmonic distortion: 0-4 kHz		1.5		%	
0-10 kHz		2.5		%	
0-50 kHz		5.0		%	
0-200 kHz		6.5	10	%	
Oscillator start-up time		<0.1	1	ms	

NOTE 2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition	Min.	Typ.	Max.	Units	Notes
Supply Voltage: On-hook	1.8		5.7	V	For memory retention
Off-hook	2.4		5.7	V	
Hookswitch Input: On-hook			$0.2V_{DD}$	V	
Off-hook	$0.8V_{DD}$			V	
Oscillating frequency		560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}–V_{SS}	-0.3 to +6.5V
Voltage on any pin (except HSW)	V_{SS} - 0.3V to V_{DD} + 0.3V
Voltage on HSW pin (See note 1)	V_{SS} - 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	±1mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	-5 to 0mA
Storage temperature	-55°C to +125°C
Operating temperature range	-10°C to +55°C

NOTES

1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300μA max. no damage will occur.
2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DS3153-1.1
Supersedes CD10705FDS-1.1

MA589 FAMILY

LD/DTMF SWITCHABLE DIALLERS WITH DEDICATED KEYS FOR 20 MEMORIES

The MA589 family are keypad switchable LD/DTMF dialler devices with a last number redial facility and twenty 24-digit memories, each with its own dedicated dialling key.

Three operating modes are available: LD only mode, DTMF only mode and LD mode with the ability to switch temporarily to DTMF mode from the keypad during a call. This last mode enables subscribers to access such services as home banking. Mixed LD and DTMF numbers can also be stored in memory.

The MA589 devices are pin compatible with the GPS switchable dialler families MA526, MA527, MA541, MA545. MA547, MA585 and MA587 – providing a complete range of telephone features within a single PCB and circuit design. Metal mask and pin selectable options are available to service specific requirements of particular countries and customers.

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- 20 × 24-Digit Memories, each with Dedicated Key
- 24 Digit Last Number Redial
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Ceramic Resonator
- Battery-less operation - Low Power CMOS
- Mask Programmable Options to suit Application
- Timed Break Recall (Flash) and Earth Recall

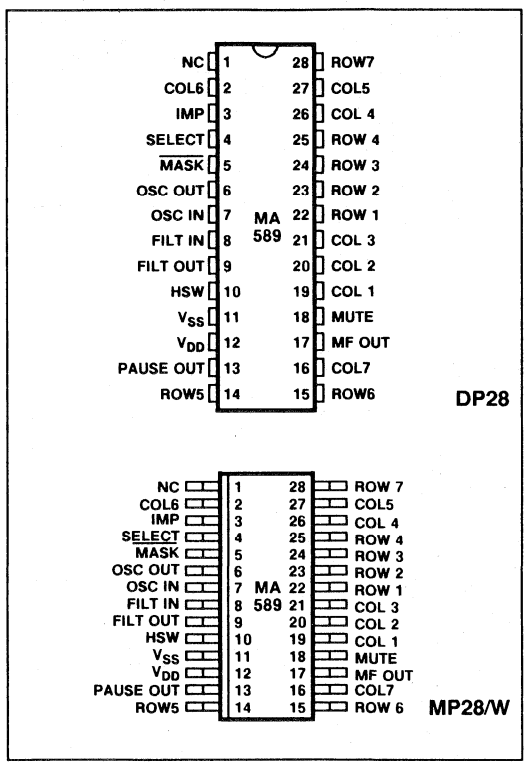


Fig.1 Pin connections - top view (not to scale)

PIN FUNCTIONS

Pin number	Pin name	Function
1	NC	Not connected
3	IMP	'Loop disconnect' dialling output
4	SELECT	LD/DTMF selection, IDP and B/M ratio programming
5	$\overline{\text{MASK}}$	Output to disable speech circuit during pulse dialling and recall (see note 1)
6	OSC OUT	Connections for 560kHz ceramic resonator
7	OSC IN	
8	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
9	FILT OUT	
10	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-Hook'
11	V_{SS}	Negative supply
12	V_{DD}	Positive supply
13	PAUSE OUT	Active high output indicating a pause when dialling from memory
17	MF OUT	Unfiltered DTMF output
18	MUTE	Output active during keying and tone transmission (see note 2)
19	COL1	Connections for 38 key single contact keypad
20	COL2	
21	COL3	
26	COL4	
27	COL5	
2	COL6	
16	COL7	
22	ROW1	
23	ROW2	
24	ROW3	
25	ROW4	
14	ROW5	
15	ROW6	
28	ROW7	

1. $\overline{\text{MASK}}$ may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1 Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA589 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied by the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted. This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start-up time if it was not already running).

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

The dialling mode may be selected via the SELECT pin (pin 4) as detailed in Table 2. Four 'Loop-Disconnect + DTMF options and four 'Loop-Disconnect only' options with different Interdigit pauses and Break/Make ratios are available and one DTMF mode. If one of the 'LD only' modes or the DTMF mode is selected then dialling will remain fixed in LD mode or DTMF mode respectively.

	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7
ROW 1	1	2	3	TBR	S01	S02	S03
ROW 2	4	5	6	REDIAL	S04	S05	S06
ROW 3	7	8	9	STORE	S07	S08	S09
ROW 4	*	0	#	PAUSE/ CONT	SHIFT	S00	LNR
ROW 5					S11	S12	S13
ROW 6				S10	S14	S15	S16
ROW 7					S17	S18	S19

Fig.2a Versions without TONE key

or/# are used to change from LD to DTMF dialling and are available as digits when in DTMF mode.

TBR: Timed Break Recall (Flash).
STORE: Memory Programming key. Use in conjunction with dedicated memory keys or a two-digit code representing the number of the memory to be programmed.
S00-S19: 'Single touch' dedicated memory dialling keys.
LNR: Last Number Redial.
REDIAL and **SHIFT:** These keys are clearly unnecessary where keypad positions are provided for all the dedicated memory keys but may be useful to access memories in applications where the telephone provides insufficient keys for all these functions. For a description of the function of the REDIAL and SHIFT keys, see the MA585 and MA587 data sheets, respectively. Do not fit keys in these positions if not required.
PAUSE/CONT: Insert pause in memory/continue dialling.
TONE: Change dialling mode from LD to DTMF

	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7
ROW 1	1	2	3	TBR	S01	S02	S03
ROW 2	4	5	6	REDIAL	S04	S05	S06
ROW 3	7	8	9	STORE	S07	S08	S09
ROW 4	*	0	#	TONE	SHIFT	S00	LNR
ROW 5					S11	S12	S13
ROW 6				S10	S14	S15	S16
ROW 7					S17	S18	S19

Fig.2b Versions with TONE key

Fig.2 Keypad layout and connections

However, if one of the 'LD + DTMF' modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing either the *, */# or TONE key (depending on the mask variant – see Fig. 2 and page 1-65), provided that dialling is not in progress. If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

SELECT pin to	Dialling mode	IDP (ms)	B/Mratio
V_{SS}	LD + DTMF	800	2:1
COL 1	LD + DTMF	500	2:1
COL 2	LD + DTMF	500	3:2
COL 3	LD + DTMF	800	3:2
COL 4	LD only	800	2:1
COL 5	LD only	500	2:1
COL 6	LD only	500	3:2
COL 7	LD only	800	3:2
V_{DD}	DTMF	–	–

Table 2 Dialling mode selection

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, the LNR key must be pressed once.

The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the LNR key; the remainder of the number will be dialled when the LNR key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the *, */#, or TONE key) to DTMF mode, only the digits dialled in LD mode will be retained. This feature is provided to ensure security of PIN (Personal Identification Number) codes. Provided that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently.

Memory Dialling

The MA589 provides 20 memories, each of which has a capacity of 24 digits and each of which has its own dedicated key. The memories can store digits to be dialled in LD, DTMF or mixed modes and also pauses.

Programming Memories

The MA589 must be 'off-hook' and idle:

1. Press the STORE key.
2. Press the key (S00-S19) of the memory to be programmed.
3. Enter digits to be stored (no digits will be dialled whilst programming)
4. To finish programming the memory either press the STORE key again or go 'on-hook'.
5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until re-programmed. If any non-valid keys are pressed during programming (e.g. LNR,TBR) they will be ignored.

Mixed mode numbers and pauses in memory

Mixed mode (i.e LD + DTMF) numbers are easily programmed into memory. The SELECT pin should be set to one of the 'LD + DTMF' modes (as it would be when dialling a mixed mode number), then the number entered using the same procedure as if dialling normally. The first press of *, */# or TONE (according to the mask variant) will be stored as a 'change to DTMF', and this will cause all subsequent digits to be sent in DTMF when redialling from memory.

Similarly, pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming.

When redialling from memory, both pauses and LD to DTMF changeovers will cause dialling to halt temporarily until the user presses the PAUSE/CONT key. The exception to this rule is when an LD to DTMF changeover is stored in the first memory location: in this case, DTMF dialling will occur immediately when memory dialling is invoked – this allows DTMF codes to be easily stored and sent even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location.

Dialling from memories

The MA589 must be 'off-hook' and idle:

1. Press the appropriate dedicated memory key (S00-S19). Dialling will now start.
2. If dialling halts due to a pause or an LD to DTMF changeover in the memory, the PAUSE OUT pin will go high (logic '1').

   Further dialling can be resumed either by pressing the PAUSE/CONT key or, alternatively, the Column 4 pin can be pulled low (for a minimum of 14 ms) to achieve the same result, thus allowing an external timer circuit to be used. The PAUSE/OUT output is reset when dialling resumes.

All keypad positions are disabled whilst memory dialling is in progress.

Timed Break & Earth Loop Recall (Flash)

The MA589 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled after the ELR/TBR operation will be retained in the LNR store [1].

A TBR (Flash) of 100ms [2] is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fig. 3, or by use of a double contact switch.

(1) *Other options are available, including an option for Danish requirements (see page 1-65). In Denmark, TBR (or ELR) is used to obtain an outside line in PABX use. Under these conditions the LNR store contents will be retained and can be redialled after a TBR or ELR. Digits manually entered after a TBR or ELR will become the new LNR store contents.*

(2) *Other TBR (Flash) periods are available as mask options (see page 1-65).*

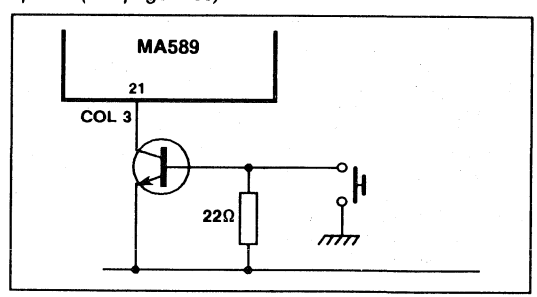


Fig.3 Earth loop recall

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally, the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 7 & 8) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

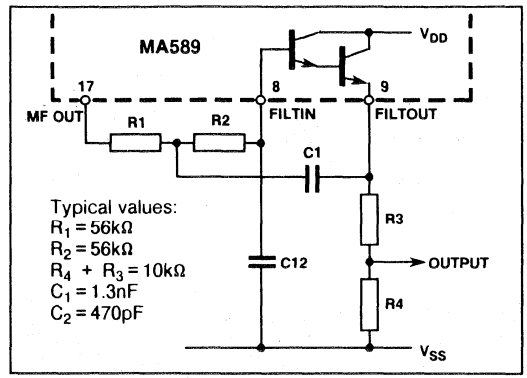


Fig.4 DTMF tone filtering

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission.

The IMP output remains low during tone transmission. The MF OUT output rises to its DC level of 0.9 V_{DD} at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 100ms, the tone output will continue until the key is released.

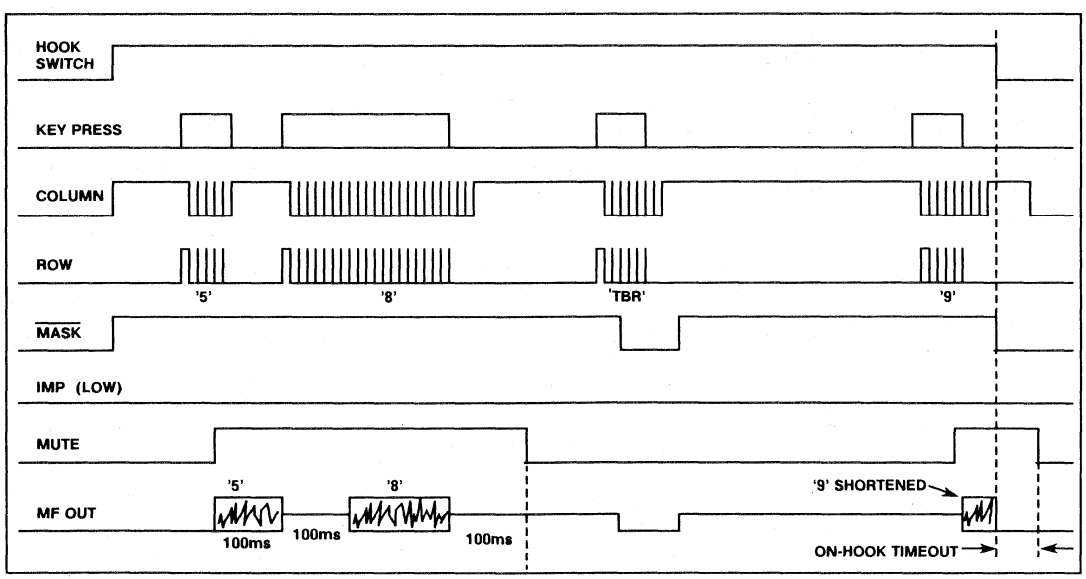


Fig.5 DTMF mode timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	- 0.07	- 0.10	+ 0.19	- 0.15	- 0.17	- 0.20	- 0.22	- 0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 3 Tone frequencies

LOOP-DISCONNECT DIALLING

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic '0' during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling. LD dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

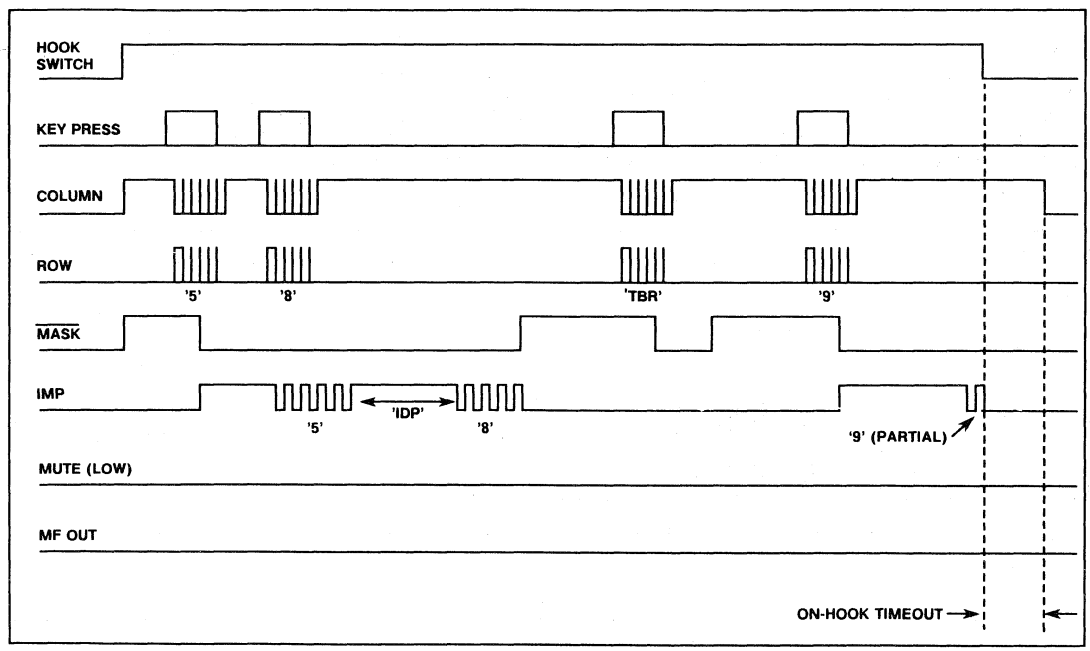


Fig.6 LD mode timing diagram

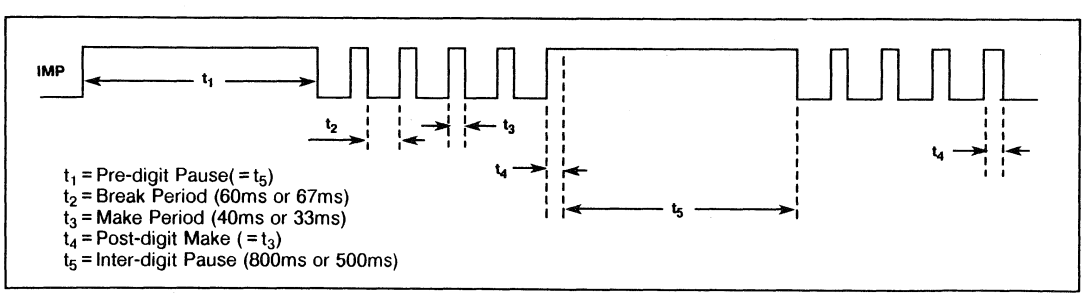


Fig.7 Timing data

MASK OPTIONS

The MA589 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufacture. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit.

The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

1. TBR (Flash) Period
- ***a. 100 ms***
- b. 200 ms
- c. 300 ms
- d. 400 ms
- e. 500 ms
- f. 600 ms

2. LD to DTMF Keypad Switching
- ***a. * and # keys***
- b. TONE key
- c. * key

3. Retention of Post-*/# Digits in LNR Store (DTMF Mode)
- ***a. All digits retained***
- b. Digits before * or # retained.
- c. Digits before * or # retained (except when * or # is first digit).

4. LD dialling options
- ***a. Standard (n = n pulses, except 0 = 10 pulses)***
- b. Swedish (n = (n + 1) pulses)
- c. Norwegian (n = (11-n) pulses)
- d. New Zealand (n = (10-n) pulses)

5. Recall (Flash)/LNR protocol
- ***a. Digits dialled after Recall retained.***
- b. Digits dialled before Recall retained
- c. Recall inhibits LNR
- d. For Danish PABX requirements

6. DTMF Minimum Timings
- ***a. 100ms on, 100ms off***
- b. 73ms on, 73ms off
- c. 73ms on, 147ms off

7. Pin 5
- ***a. $\overline{MASK}$***
- b. MASK

8. Pin 3
- ***a. IMP***
- b. $\overline{IMP}$
- c. [IMP + $\overline{MASK}$]
- d. $\overline{[IMP + \overline{MASK}]}$

9. Pin 18
- ***a. MUTE***
- b. $\overline{MUTE}$

APPLICATION CIRCUITS

Refer to the MA541 data sheet, Figs. 8 and 9, on pages 1-29 and 1-30

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V, T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Supply Current: On-hook		<0.2	5.0	μA	V_{DD} = 2.0V. See note 1.
Off-hook		1.5		μA	MF OUT low
MF tone sending			1.0	mA	
LD impulsing			200	μA	
Output high voltage (MASK, MUTE and IMP outputs)	2.2			V	I = -1mA
Output low voltage (MASK, MUTE and IMP outputs)			0.3	V	I = +1mA
MF OUT DC level during tone sending		$0.9V_{DD}$		V	
MF OUT output resistance		3		kΩ	
'Key Pressed' resistance			2	kΩ	$2.5V < V_{DD} < 5.7V$
'Key Not Pressed' resistance	500			kΩ	$2.5V < V_{DD} < 5.7V$
Darlington pair current gain (see Fig. 4)	600	50,000			$I_E = 100\mu A$, $V_{CE} = 2V$

NOTE 1. Specially tested versions with guaranteed lower on-hook supply current are available.

AC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Tone output: low group	57	64		mV rms	No load
high group		81	91	mV rms	No load
High-to-Low group amplitude ratio (pre-emphasis)	1.5	2	2.5	dB	See note 2.
Total harmonic distortion: 0-4 kHz		1.5		%	
0-10 kHz		2.5		%	
0-50 kHz		5.0		%	
0-200 kHz		6.5	10	%	
Oscillator start-up time		<0.1	1	ms	

NOTE 2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition	Min.	Typ.	Max.	Units	Notes
Supply Voltage: On-hook	1.8		5.7	V	For memory retention
Off-hook	2.4		5.7	V	
Hookswitch Input: On-hook			$0.2V_{DD}$	V	
Off-hook	$0.8V_{DD}$			V	
Oscillating frequency		560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}–V_{SS}	−0.3 to +6.5V
Voltage on any pin (except HSW)	V_{SS} − 0.3V to V_{DD} + 0.3V
Voltage on HSW pin (See note 1)	V_{SS} − 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	±1mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	−5 to 0mA
Storage temperature	−55°C to +125°C
Operating temperature range	−10°C to +55°C

NOTES

1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300μA max. no damage will occur.
2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DS3154-1.0
Supersedes C800D 1.1

MA552

BILINGUAL (LOOP-DISCONNECT AND DTMF) DIALLER WITH REDIAL

The MA552 is a CMOS Bilingual (ie Loop Disconnect and Multi-frequency) dialler chip with a 21 digit Last Number Redial facility. The chip can be operated in either LD mode, MF mode or a third mode in which dialling can be switched from LD to DTMF from the keypad during a call. This third mode is intended for users connected to an exchange accepting only LD signalling but may require access to facilities such as home banking and databases accepting DTMF signalling.

Low power CMOS design allows the LNR store contents to be maintained by a minimal current whilst the telephone is on-hook. A selectable facility allows access pauses to be recognised during manual dialling and to regenerate these pauses automatically when using the LNR facility.

In order to cater for the telephone specifications of many countries and different circuit configurations, the MA552 offers a variety of pin selectable and metal mask programmable options.

Other features include a temperature compensated voltage reference for accurate DTMF levels independent of supply voltage and a 'single pin' oscillator circuit requiring only an inexpensive external 560kHz ceramic resonator. Both Timed Break Recall (Flash) and Earth Loop Recall are supported and offer identical operating protocols.

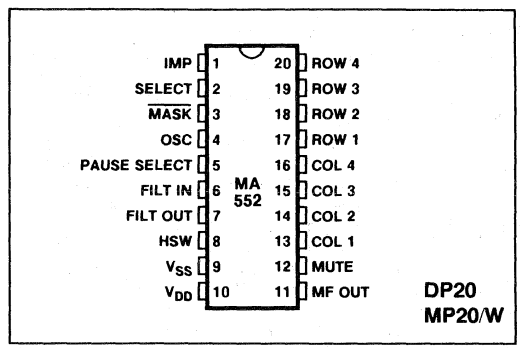


Fig.1 Pin connections - top view (not to scale)

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- DTMF output Levels Independent of Temperature and Voltage
- 21 Digit Last Number Redial
- Automatic Pause Detection for LNR
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Ceramic Resonator
- Battery-less Operation – Low Power CMOS
- Mask Programmable Options to suit Application
- PIN (Personal Identification Number) Confidentiality
- Timed Break Recall (Flash) and Earth Recall

PIN FUNCTIONS

Pin number	Pin name	Function
17 18 19 20 13 14 15 16	ROW1 ROW1 ROW1 ROW1 COL1 COL1 COL1 COL1	Connections for 16-key, single contact keyboard
10	V_{DD}	Positive supply
9	V_{SS}	Negative supply
2	MODE SELECT	LD/MF selection, and B/M ratio programming
5	PAUSE SELECT	Pause and Pause Duration Selection
4	OSC	Oscillator connection. Connect 560kHz resonator from this pin to V_{SS}.
8	HSW	Hookswitch. A logic '1' voltage at this pin is used to indicate 'off-hook'
3	$\overline{\text{MASK}}$	Output to disable speech circuit during LD dialling and Recall (Flash): Note 1
1	IMP	'Loop-Disconnect' dialling output
11	MF OUT	Unfiltered, dual tone output
7	FILT OUT	Unity gain amplifier output for 2-pole filter
6	FILT IN	Unity gain amplifier input for 2-pole filter
12	MUTE	Output active during keying and tone transmission: Note 2

1. $\overline{\text{MASK}}$ may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1 Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA552 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied by the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted.This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start-up time if it was not already running).

	COL 1	COL 2	COL 3	COL 4
ROW 1	1	2	3	TONE *
ROW 2	4	5	6	TBR
ROW 3	7	8	9	
ROW 4	*	0	#	LNR

TONE :Change dialling mode from LD to DTMF
** This key is only available as a mask variant.*
TBR: Timed Break Recall (Flash).
LNR: Last Number Redial.

Fig.2 Keypad layout and connections

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Two key rollover

If one key is pressed and verified and then a second key pressed whilst the first is still held down, the second key will be accepted only when both keys are released or the second key pressed again.

Dialling Mode Selection

The dialling mode may be selected via the MODE SELECT pin (pin 2) as detailed in Table 2. If one of the 'LD only' modes or 'DTMF only' mode is selected then dialling will remain fixed in the mode selected. However, if one of the 'LD + DTMF' modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing either the *, */# or TONE key (dependent on the mask variant – see page 1-72), provided that dialling is not in progress. If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

MODE SELECT pin to	Dialling mode	Keypad switchable	B/Mratio
V_{SS}	LD	NO	2:1
COL 1	LD	YES	2:1
COL 2	LD	NO	3:2
COL 3	LD	YES	3:2
V_{DD}	DTMF	–	–

Table 2 Dialling mode selection

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, the REDIAL key must be pressed twice.

The last number redial store has several features designed to assist the user:

Automatic pause feature

PAUSE SELECT pin to	Pause option
V_{SS}	No pause
COL 1	3s pause
COL 2	6s pause
V_{DD}	Manual pause

Table 3 Pause option selection

This feature may be selected as detailed in Table 3. When selected, the MA552 will detect up to two pauses during dialling and insert these into the LNR store.

A pause is defined as follows:

1. In LD mode - if the user waits until the digit(s) already entered have been dialled before entering further digits

2. In DTMF mode - if the user waits for 1 second[1] after the 1st, 2nd or 3rd digit(s)[2] have been dialled before entering further digits.

On redialling, a pause of either 3s, 6s or until the user presses the LNR key again (as selected) will occur whenever a pause was recognised. A timed pause may also be interrupted by pressing the LNR key again.

Notes: (1) Mask options for 2 & 3 seconds are available.

(2) A Mask option is available to allow up to 2 pauses to be detected at any time in DTMF mode.

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the REDIAL key; the remainder of the number will be dialled when the REDIAL key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the *, */#, or TONE key) to DTMF mode, only the digits dialled in LD mode will be retained. Providing that the number of digits dialled in LD mode does not exceed 21, they will be retained regardless of the number of DTMF digits entered subsequently. This feature is provided to ensure security of PIN (Personal Identification Number) codes.

DTMF calls

If a call contains the digits * or # only those digits dialled prior to the first press of either * or # will be retained in the LNR store.This feature also ensures security for PIN codes.

The exception to this is if * or # is the first digit dialled whilst in the off-hook state. In this case the * or # and all subsequent digits (including further * or #) will be retained.

Timed Break & Earth Loop Recall (Flash)

The MA552 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the dialling mode selected via the MODE SELECT pin will be restored. Also, only the digits dialled after the ELR/TBR operation will be retained in the LNR store.

A TBR (Flash) of 100ms is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin (pin 16). If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fig. 3, or by use of a double contact switch.

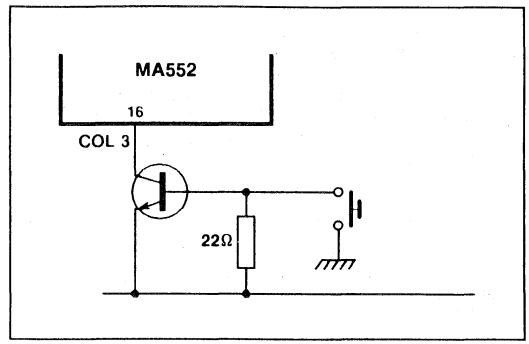


Fig.3 Earth loop recall

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC and V_{SS} to provide a timing reference for all chip functions. No other components are required or should be used.

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 6 & 7) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

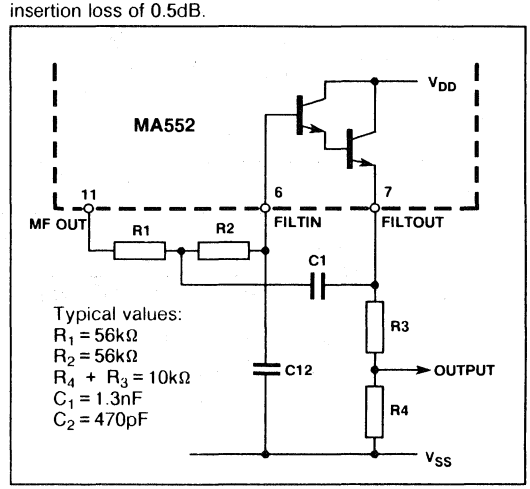


Fig.4 DTMF tone filtering

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The IMP output remains low during tone transmission. The MF OUT output rises to its DC level of V_{DD} – 0.3V at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 100ms, the tone output will continue until the key is released.

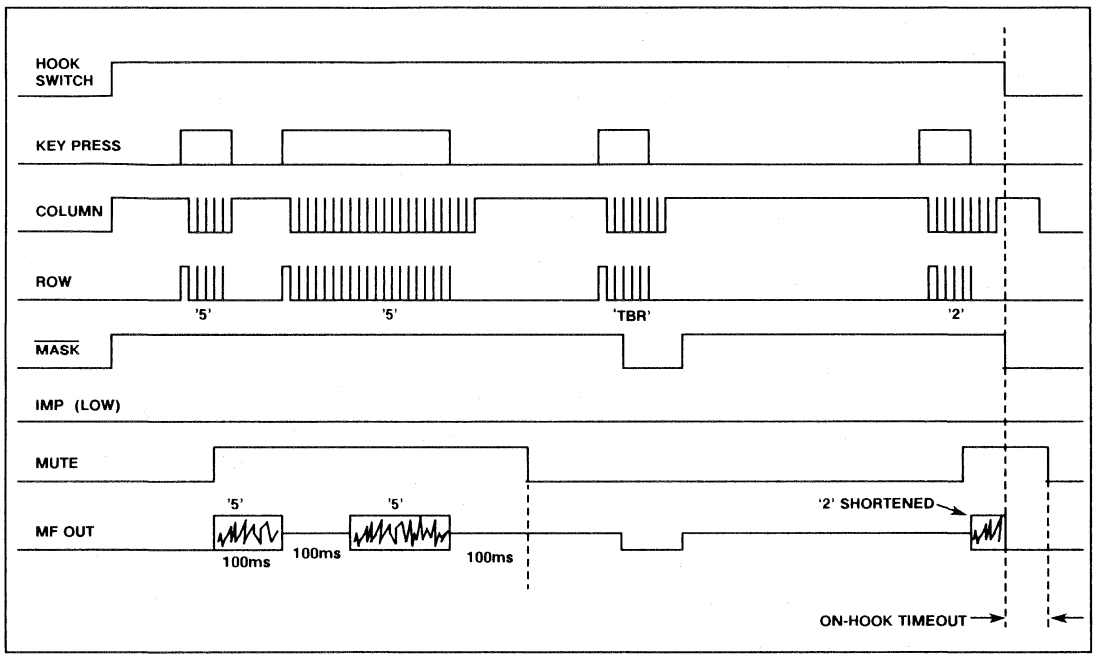


Fig.5 DTMF mode timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477
Deviation from nominal (%)	– 0.07	– 0.10	+ 0.19	– 0.15	– 0.17	– 0.20	– 0.22

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 4 Tone frequencies

LOOP-DISCONNECT DIALLING

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic '0' during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling. LD dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

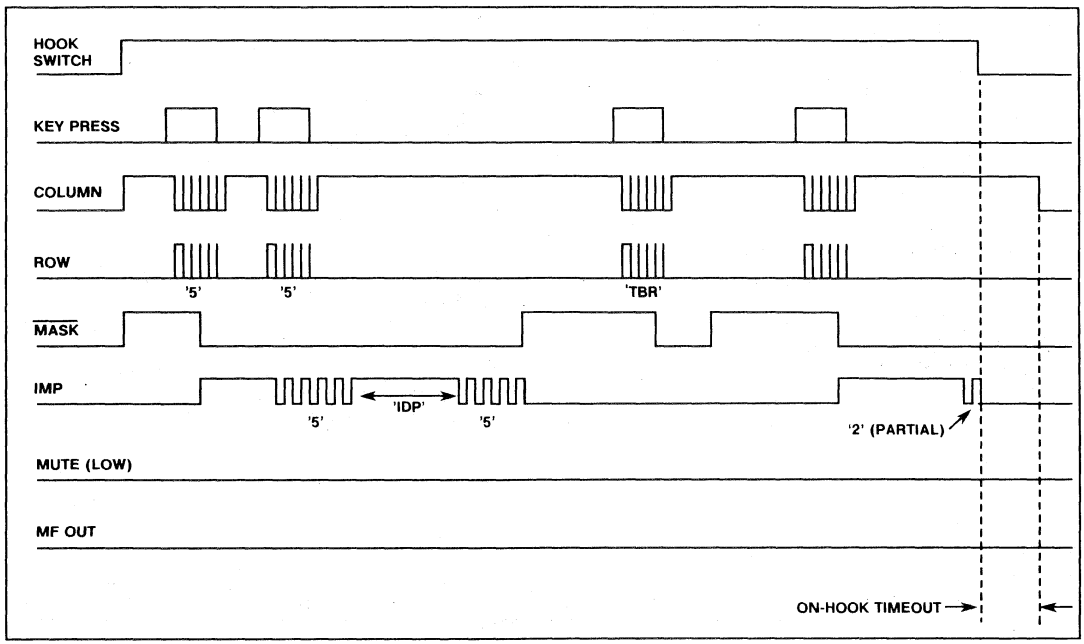


Fig.6 LD mode timing diagram

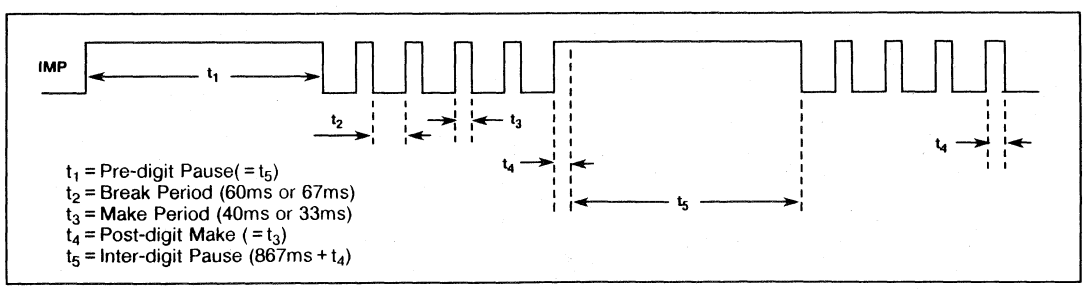


Fig.7 Timing data

MASK OPTIONS

The MA552 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufacture. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit.

The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

1. TBR (Flash) Period
- ***a. 100 ms***
- b. 200 ms
- c. 300 ms
- d. 400 ms
- e. 500 ms
- f. 600 ms

2. LD to DTMF Keypad Switching
- ***a. * key***
- b. * and # keys
- c. TONE key

3. Inter-Digit Pause Options
- ***a. 867ms (not incluning PDM)***
- b.520ms (not including PDM)

4. LD dialling
- ***a. Standard (n = (n + 1 pulses, except 0 = 10)***
- b. Swedish (n = (n + 1) pulses)
- c. Norwegian (n = (11-n) pulses)
- d. New Zealand (n = (10-n) pulses)

5. Pin 3
- ***a. $\overline{MASK}$***
- b. MASK

6. Pin 1
- ***a. IMP***
- b. $\overline{IMP}$
- c. [IMP + $\overline{MASK}$]
- d. $\overline{[IMP + \overline{MASK}]}$

7. Pin 12
- ***a. MUTE***
- b. $\overline{MUTE}$

8. Pause Recognition Period (in DTMF Mode)
- ***a. 1 second***
- b. 2 seconds
- c. 3 seconds

9. Pause Recognition Position (in DTMF Mode)
- ***a. After 1st, 2nd and 3rd digits only***
- b. At any time during number

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V, T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Supply Current: On-hook		<1	2	µA	V_{DD} = 2.0V
Off-hook		1.5		µA	MF OUT low
MF tone sending			1.0	mA	
LD impulsing			200	µA	
Output high voltage ($\overline{MASK}$, MUTE and IMP outputs)	2.2			V	I = -1mA
Output low voltage ($\overline{MASK}$, MUTE and IMP outputs)			0.3	V	I = +1mA
MF OUT DC level during tone sending		V_{DD}-0.3		V	
MF OUT output resistance		5		kΩ	
'Key Pressed' resistance			2	kΩ	2.5V < V_{DD} < 5.7V
'Key Not Pressed' resistance	500			kΩ	2.5V < V_{DD} < 5.7V
Darlington pair current gain (see Fig. 4)	600	50,000			I_E = 100µA, V_{CE} = 2V

AC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Tone output: low group	68	77		mV rms	No load
high group		97	109	mV rms	No load
High-to-Low group amplitude ratio (pre-emphasis)	1.5	2	2.5	dB	See note 1.
Total harmonic distortion: 0-4 kHz		1.5		%	
0-10 kHz		2.5		%	
0-50 kHz		5.0		%	
0-200 kHz		6.5	10	%	
Oscillator start-up time		<0.1	1	ms	

NOTE 1. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition	Min.	Typ.	Max.	Units	Notes
Supply Voltage: On-hook Off-hook	1.8 2.4		5.7 5.7	V V	For memory retntion
Hookswitch Input: On-hook Off-hook	 $0.8V_{DD}$		$0.2V_{DD}$	V V	
Oscillating frequency		560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}–V_{SS}	– 0.3 to + 6.5V
Voltage on any pin (except HSW)	V_{SS} – 0.3V to V_{DD} + 0.3V
Voltage on HSW pin (See note 1)	V_{SS} – 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	± 1mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	–5 to 0mA
Storage temperature	–55°C to + 125°C
Operating temperature range	–25°C to + 70°C

NOTES

1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300μA max. no damage will occur.
2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS

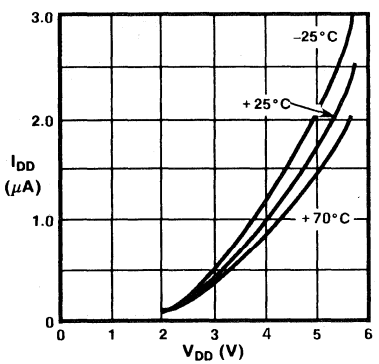


Fig.8 On-hook supply current as a function of supply voltage

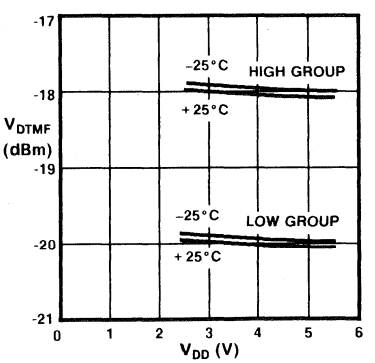


Fig.9 DTMF output voltage levels as a function of supply voltage

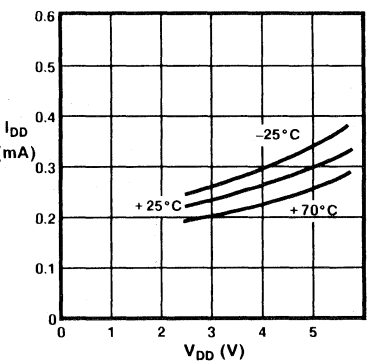


Fig.10 Operating supply current (DTMF output active) as a function of supply voltage

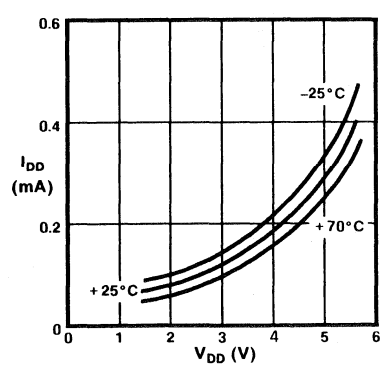


Fig.11 Operating supply current (LD outpulsing) as a function of supply voltage

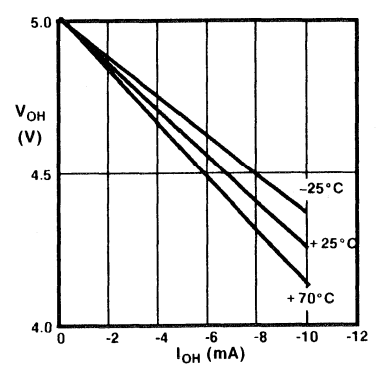


Fig.12 DC Output High levels as a function of output source current (V_{DD} = 5V)

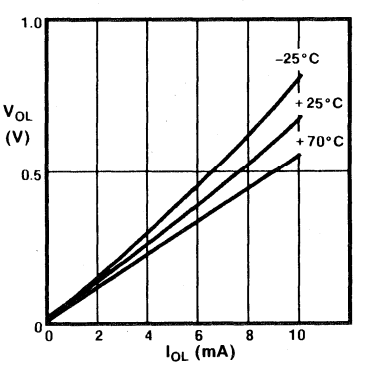


Fig.13 DC Output Low levels as function of output sink current (V_{DD} = 5V)

APPLICATION CIRCUITS

Figs. 14 and 15 are simplified examples of how the MA552 may be used in a telephone circuit suitable for Loop-Disconnect and DTMF signalling. For clarity, none of the components required for DTMF tone filtering are shown.

In Fig.14, a 4MΩ resistor is used to leak current from the line when the telephone is on-hook in order to maintain the contents of the LNR Store.

Fig. 15 demonstrates how a large, low leakage capacitor can be used to maintain the contents of the LNR store for a finite period in applications where complete line isolation is required whilst on-hook.

In both circuits a 47μF capacitor is used to maintain and smooth the supply to the chip and the 130V Zener diode protects the chip from overvoltage.

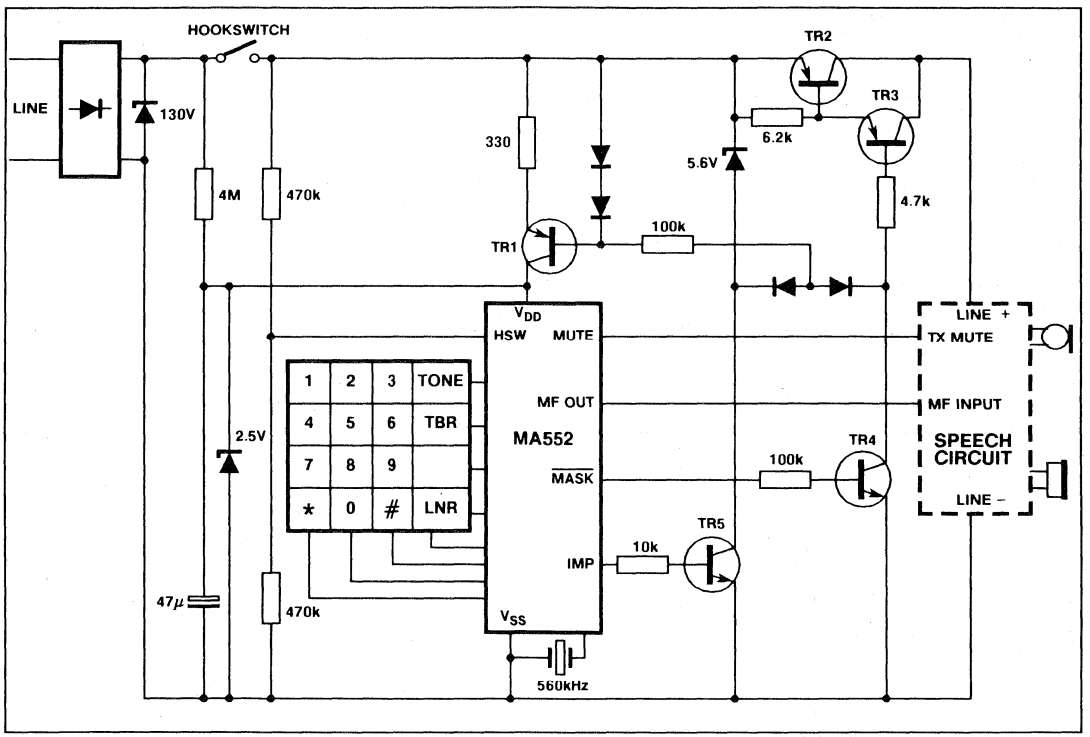


Fig.14

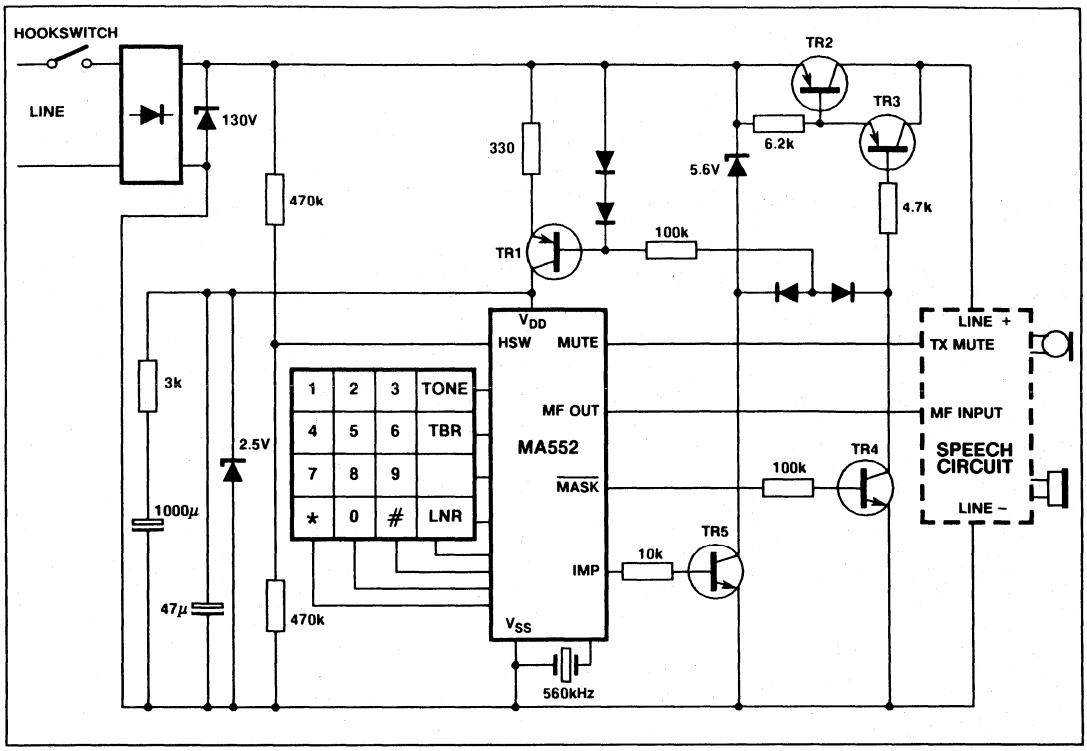

HOOKSWITCH
LINE
130V
470k
330
TR2
TR3
6.2k
5.6V
4.7k
TR1
100k
3k
2.5V
1000µ
47µ
470k
1 2 3 TONE
4 5 6 TBR
7 8 9
* 0 # LNR
VDD
HSW
MUTE
MF OUT
MA552
MASK
IMP
VSS
560kHz
10k
TR5
100k
TR4
LINE +
TX MUTE
MF INPUT
SPEECH CIRCUIT
LINE –

Fig.15

DS3146-1.0
Supersedes Version 2.1

MA525

MICROPROCESSOR CONTROLLED LD/DTMF DIALLER

The MA525 is a microprocessor controlled Loop-Disconnect (LD) and Dual Tone Multi-Frequency (DTMF) dialler device with a last number redial facility.

The MA525 is directly controlled via a MOTEL™ interface which automatically adapts to either Motorola or Intel format, thereby allowing interfacing to most common microprocessors and microcontrollers. The bus design allows both 4 and 8-bit bus systems to be used and the device is designed to allow the bus to be shared with other peripheral devices.

All dialling conditions and timings are programmable via on-chip registers in order to allow the device to meet the specifications of virtually any telephone network with one standard product. Blocks of up to 21 digits at a time (including TBR and Pause) can be loaded for dialling. The device will retain the last number dialled for redialling if required.

Dialling and associated control signals are generated by the device in both LD and DTMF modes using a low-cost 560kHz ceramic resonator as an accurate timing reference.The A,B,C,D tone pairs are available in DTMF mode. In addition, a 'single tone' output is provided.

The MA525 can be operated in either 'Phone' or 'Modem' mode, generating appropriate control signals for the application.

The polarity of all output signals may be inverted, making the MA525 suitable for use with virtually any line interfacing technique.

A chip select ($\overline{CS}$) input is also provided, allowing the MA525 to share a common microprocessor bus with other microprocessor peripherals.

APPLICATIONS

- Feature Telephones
- Auto-Dialling Modems
- Auto-Dialling Telephones
- Pay Phones
- Security Products
- Cordless Telephone Base Stations
- Banking Facilities

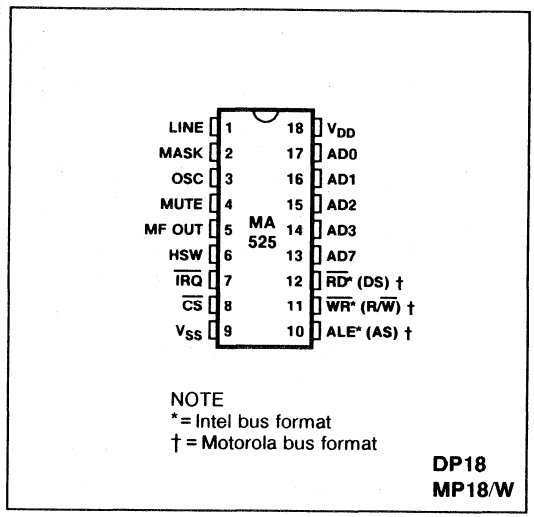


Fig.1 Pin connections - top view

FEATURES

- MOTEL™ Microprocessor Interface for Direct Connection to Motorola or Intel Derived Buses
- Loop-Disconnect and DTMF dialling.
- Modem and Phone Modes.
- Last Number Redial Facility.
- All Timing Parameters Programmable to meet International Signalling Requirements
- Reloadable 21-digit Store Including Access Pause and Timed Break Recall (Flash).
- Reliable Power-on Reset.
- Uses a Low-cost 560kHz Ceramic Resonator

PIN FUNCTIONS

Pin no.	Name	Type	Function
1	LINE	O	Dialling pulse output and modem line control.
2	MASK	O	Output to disable speech circuit during LD dialling and TBR.
3	OSC	I/O	Connection for 560kHz ceramic resonator.
4	MUTE	O	Output to inhibit microphone during DTMF dialling. In Modem mode it can be used to switch DTMF tones or the modem to the line.
5	MF OUT	O	DTMF tone output.
6	HSW	I	Hookswitch sense input. '1' = Off-hook. No direct control for modem use but status still available.
7	$\overline{IRQ}$	O	Interrupt request. N-channel open-drain output.
8	$\overline{CS}$	I	Chip select input. Used to activate MOTEL interface.
9	V_{SS}	SUPPLY	Negative supply
10	AS ALE	I	Motorola Mode: Address Strobe Intel Mode: Address Latch Enable
11	R/$\overline{W}$ $\overline{WR}$	I	Motorola Mode: Read/Write Intel Mode: Write Strobe
12	DS $\overline{RD}$	I	Motorola Mode: Data Strobe Intel Mode: Read Strobe
13	AD7	I/O	Available for servicing interrupt request
14	AD3	I/O	Multiplexed address/data bi-directional bus. MSB.
15	AD2	I/O	Multiplexed address/data bi-directional bus.
16	AD1	I/O	Multiplexed address/data bi-directional bus.
17	AD0	I/O	Multiplexed address/data bi-directional bus. LSB.
18	V_{DD}	SUPPLY	Positive supply.

Table 1 Pin functions

MICROPROCESSOR INTERFACE

The MA525 interfaces to the controlling microprocessor by means of a multiplexed bus of the MOTEL format. This interface bus has the ability to adapt itself automatically to the format and timing of both MOTorola and IntEL interface busses (hence MOTEL). Internally, the detection circuitry latches the status of the DS/$\overline{RD}$ line when AS/ALE goes high. If the result is high, then the Intel mode is used; if the result is low then the Motorola mode is used. This procedure is carried out each time that AS/ALE goes high. Note that the MA525 defaults to Intel mode on power up and is reconfigured to the relevant mode after the first DS/ALE positive going edge.

In practice the MOTEL interface is transparent to the user. For bus connection and timing information simply refer to the description relevant to the particular microprocessor/ microcontroller used.

Industry standard microprocessors such as the 8085,8088 etc. and microcontrollers such as the 8051 or 6805 are all compatible with the interface on the MA525. It is also possible to drive the microprocessor interface pins on the MA525 directly using port pins .

It should be noted that all bus timings are derived from the microprocessor and are independent of the MA525 clock input.

Registers 0 to 9 are write only whereas Register 10 is a read-only Status Register. An interrupt pin is provided ($\overline{IRQ}$) to speed microprocessor interfacing. This may be disabled at any point if necessary. In addition, an Interrupt Request Flag in Register 10 operates in exactly the same way as the $\overline{IRQ}$ pin (but is active high).

BUS TIMINGS

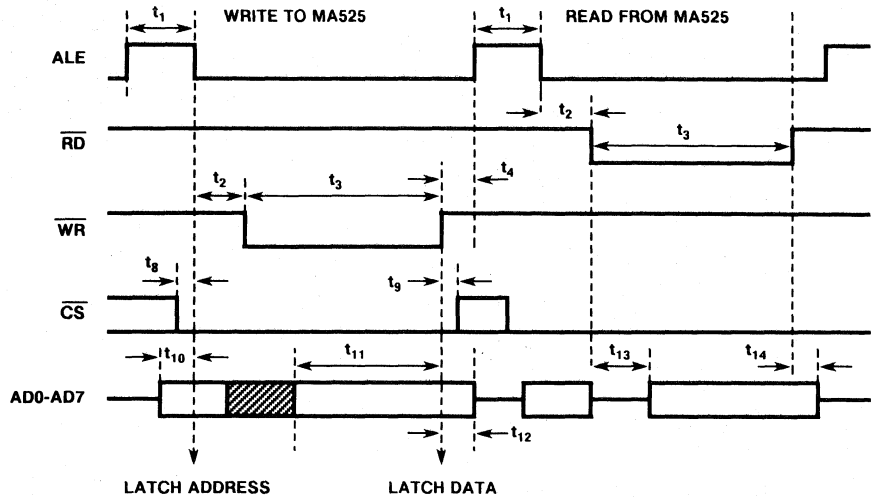


Fig.2 Intel bus timing diagram

Parameter	Symbol	Min	Typ	Max	Units
ALE high period	t_1	70			ns
Delay time , ALE to $\overline{WR}$	t_2	40			ns
$\overline{WR}$ low period	t_3	50		50μs	ns
Delay time, $\overline{WR}$ high to ALE high	t_4	10			ns
$\overline{CS}$ setup time	t_8	40			ns
$\overline{CS}$ hold time	t_9	0			ns
Address setup time	t_{10}	30			ns
Address hold time	t_{15}	10			ns
Data setup time	t_{11}	50			ns
Data hold time	t_{12}	0			ns
Output data response time	t_{13}		60	85	ns
Output data removal time	t_{14}		30	50	ns

The address is latched by the falling edge of ALE. Data is written from the bus into the MA525 on the rising edge of $\overline{WR}$. Data can be read from the MA525 on the rising edge of $\overline{RD}$ providing that this follows the falling edge of $\overline{RD}$ by the minimum period, t_3. All bus timings are quoted with 30pF capacitance to V_{SS}.

Table 2 Intel bus timings at V_{DD} = 5V, T_{AMB} = +25°C

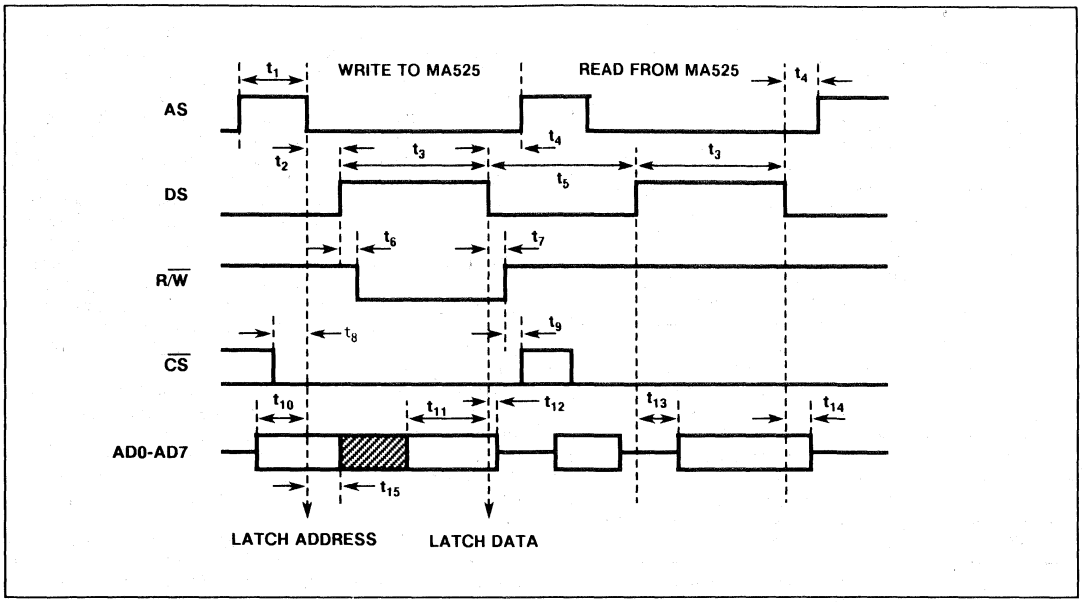


Fig.3 Motorola bus timing diagram

Parameter	Symbol	Min	Typ	Max	Units
AS high period	t_1	50			ns
Delay time , AS low to DS high	t_2	40			ns
DS high period	t_3	40		50μs	ns
Delay time, DS low to AS high	t_4	10			ns
DS low period	t_5	165			ns
DS high to R/$\overline{W}$ low setup time	t_6	15			ns
R/$\overline{W}$ hold time	t_7	10			ns
$\overline{CS}$ setup time	t_8	40			ns
$\overline{CS}$ hold time	t_9	0			ns
Address setup time	t_{10}	30			ns
Address hold time	t_{15}	10			ns
Write data setup time	t_{11}	50			ns
Write data hold time	t_{12}	0			ns
Output data response time	t_{13}		55	80	ns
Output data removal time	t_{14}		35	50	ns

The address is latched on the falling edge of the AS line. Data is written from the bus into the MA525 when R/$\overline{W}$ is low on the falling edge of DS (providing $\overline{CS}$ is low). Data can be read from the MA525 when R/$\overline{W}$ is high on the falling edge of DS. All bus timings are quoted with 30pF capacitance to V_{SS}.

Table 3 Motorola bus timings at V_{DD} = 5V, T_{AMB} = +25°C

REGISTER ADDRESSING

AD_3 - AD_0	Register	Type	Function
0000	R0	Write only	Digit buffer
0001	R1	Write only	Dial conditions
0010	R2	Write only	Control
0011	R3	Write only	Output configuration
0100	R4	Write only	Access pause time
0101	R5	Write only	DTMF timing
0110	R6	Write only	HSW response time
0111	R7	Write only	TBR (Flash) time
1000	R8	Write only	IDP time
1001	R9	Write only	Single tone O/P
1010	R10	Read only	Status

Table 4 MA525 register addressing

Default register conditions are automatically set in all programmable registers on power-up and remain valid until a register is reprogrammed. In addition the dial store is cleared.

Read commands to a 'write only' register and write commands to a 'read only' register will be ignored.

Note that register 11 is provided for in-house test purposes and should not be used during normal device operation. If a register number greater than 11 is addressed, the command will be ignored and the ERROR bit raised.

REGISTER FUNCTIONS

(A summary showing register functions and calculations is given on page 1-85).

It is recommended that parameters set in Registers 1, 3, 4, 5, 7 and 8 should not be changed while dialling is in progress. However, parameters can be changed during the same call provided that dialling is not active (i.e. if the BUSY bit in the status register is at '0') at the time -there is no need to go on-hook or to set the DISCON bit before changing parameters.

If parameters in registers 1, 3, 4, 5, 7 or 8 are changed during dialling, misdialling may occur but the device will operate normally when the dial sequence is complete. The ERROR flag will not be raised in this case.

Register 0 - Digit Buffer

Digits to be sent to the dial store should be loaded into Register 0. To load a TBR or a Pause into the dial store the appropriate bits should be set in register 2. Digits will be sent to the dial store in the order in which they are loaded into registers 0 and 2.

Digits may be loaded into the dial store in blocks of up to 22 digits. If more than 22 digits are loaded in total, it is important not to perform a last number redial to ensure correct operation.

Digits can be loaded into Register 0 either before or after the DIAL Bit is set in Register 2. Digits loaded after the DIAL bit is set will be concatenated with any digits yet to be dialled. However, if digits are loaded whilst a Last Number Redial is being dialled the digits will be ignored.

Each digit can be loaded into the dial store using a handshaking routine. As each digit is loaded into register 0 (or bits 2 and 3 in register 2) the BUF bit is set in the status register (Register 10). When the digit has been accepted into the dial store from Register 0, the BUF bit is cleared, indicating that the next digit can be loaded into register 0. Alternatively digits can be loaded directly without monitoring the BUF bit providing that the timing requirements are met (see a.c. conditions). In either case the ERROR bit in the Status Register will be set if an attempt is made to load a digit while the BUF bit is set to 1 and the digit will not be accepted.

Up to 21 undialled digits can be held in the dial store at a time. Once the dial store is full the BUF bit will be set to 1 and no further digits can be loaded until it is reset to 0 either because space becomes available (due to digits having been dialled out) or until the device is sent on-hook (in Phone mode) or DISCON is set to 1 (Modem mode).

Codes *,A,B,C,D and # are illegal in LD mode and will not be accepted into Register 0 while the device is set to LD mode. If an attempt is made to do this, the ERROR bit will be set in the Status Register.

Bits 3210	Code	Digit	Comment
0000	0	0	0 = 10 pulses in LD mode
0001	1	1	
0010	2	2	
0011	3	3	
0100	4	4	
0101	5	5	
0110	6	6	
0111	7	7	
1000	8	8	
1001	9	9	
1010	10	*	Not allowed in LD mode
1011	11	A	Not allowed in LD mode
1100	12	B	Not allowed in LD mode
1101	13	C	Not allowed in LD mode
1110	14	D	Not allowed in LD mode
1111	15	#	Not allowed in LD mode

Table 5 Register 0 - digit buffer

Register 1 - Dial Conditions Register

Bit	Name	Default	Function
0	USE	0	Phone or Modem use 0 = Phone 1 = Modem
1	B/M	0	Break/Make ratio 0 = 2:1 1 = 3:2
2	DS	0	Dialling Speed (LD) 0 = Normal 1 = Double
3	MODE	0	LD/DTMF dialling 0 = LD 1 = DTMF

Table 6 Register 1

If the USE bit is cleared whilst the LINE output is at a '1' state, the LINE output will not be cleared. Normal Phone Mode operation will resume after the DISCON bit is next set.

Bit 2 of register 1 defines the dialling speed in LD only. If this bit is cleared the dialling speed will be set to 10 impulses per second and all other timings will be as per the relevant registers. If the DS bit is set however, the dialling speed will be 20 impulses per second and all other timings will also be halved.

Register 2 - Control Register

Bit	Name	Default	Function
0	DIAL	0	Start dial sequence 1 = Start
1	DISCON	1	Disconnect 0 = Seize line, 1 = Disconnect line
2	ACCESS	0	Load access pause = 1
3	TBR	0	Load TBR (Flash) = 1

Table 7 Register 2

When the DIAL bit is set to 1, dialling will start, assuming DISCON is set to 0. If dialling is terminated either by the HSW being timed out (in Phone mode) or by setting the DISCON bit to 1 (in both modes), the dial bit is automatically reset to 0. Note that forcing the DIAL bit low using the microprocessor interface does *not* terminate dialling.

In Phone mode, setting the DISCON bit simply terminates dialling immediately. The device outputs then revert to their normal 'off-hook and idle' states. If, when programming Register 2 in Phone mode an attempt is made to set both the DIAL and DISCON bits to '0', the command will be ignored.

In Modem mode, setting the dial bit causes LINE to make a low to high transition after 6.6ms. After dialling is completed, the LINE output will remain high, thereby holding the line for subsequent speech/data interchange. DISCON may be used at any time to relinquish the line - thus ending the call. Further digits may be loaded and dialled at any time whilst LINE is high.

If, when programming register 2, an attempt is made to set both the DIAL and DISCON bits to '1', DIAL will be set to '0' and DISCON to '1', i.e. DISCON takes priority. The DIAL /DISCON protocol is shown in State Diagram form in Figs. 4 and 5. If PAUSE and TBR bits are set simultaneously , the write operation will be ignored and the ERROR flag raised.

If an LNR is required after setting DISCON, simply set the DIAL bit. In order to prevent the device redialling the previous number, it is necessary to clear the DISCON bit first.

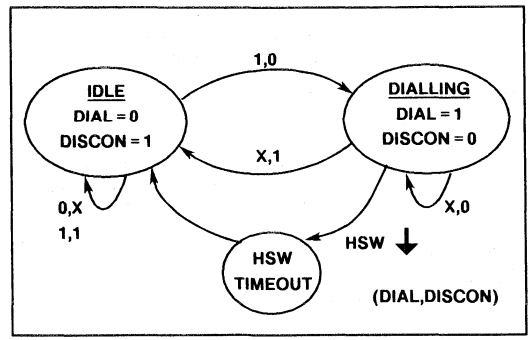


Fig.4 Finite state diagram – Phone mode

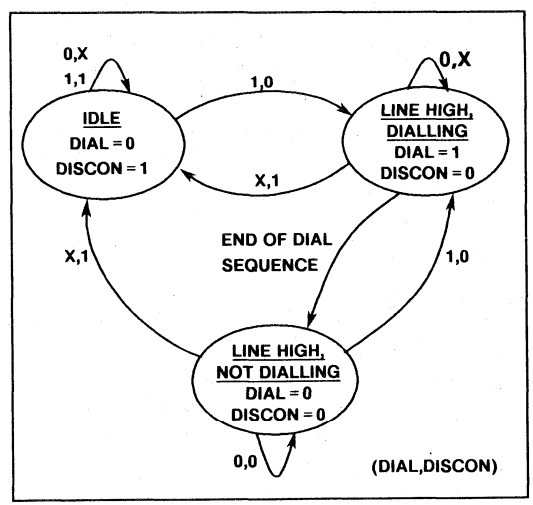


Fig.5 Finite state diagram – Modem mode

Note that since TBR and Pause are treated as normal digits, the device places a Pre-Digit Pause before, and an Inter-Digit Pause after the TBR/Pause whilst in LD mode. In DTMF mode, a tone pause period (as defined by register 5) is placed both before and after the TBR/Pause.

On power up, if the DIAL bit is set without first loading any digits in LD mode, the device defaults to dialling an access digit (9).

WARNING: No response will be obtained if Access Pause or TBR is entered as the first digit in a string with non-default values in either Pause Duration register or TBR Duration register whilst in DTMF mode. If this condition is inadvertantly invoked, it may be cleared by setting the DISCON bit (in both Phone and Modem modes), toggling the HSW input (in Phone mode only) or by powering down the MA525.

Register 3 - Output Configuration Register

Bit	Name	Default	Function
0	IE	0	Interrupt Enable 0 = Disable 1 = Enable
1	LS	0	LINE output polarity 0 = Normal 1 = Invert
2	MS	0	MUTE output polarity 0 = Normal 1 = Invert
3	KS	0	MASK output polarity 0 = Normal 1 = Invert

Table 8 Register 3

Disabling the Interrupt Enable simply disables both the $\overline{IRQ}$ output (i.e. high-impedance open-drain) and the IRQF bit in the Status Register.

Register 4 - Access Pause Duration

Code	Default	Function
1 - 15	1 (i.e. 500ms)	Set length of Access pause. Duration = Code × 500ms.

Table 9 Register 4

If code 0 is loaded, the Access Pause duration will be set to the default value and the ERROR bit will be set in the status register.

If pauses longer than 7.5 seconds are required, Pauses may be programmed more than once in succession. This will give a longer 'seamless' pause with no transitions on any device outputs.

Register 5 - DTMF Duration

Bit	Name	Default	Function
0-3	Duration	15 (100ms)	Set tone on/off period. Period = (Code × 6.67) ms

Table 10 Register 5

Register 5 sets both the active tone period and the pause time between tones. Note that if code 0 is loaded, the DTMF duration is set to the default value and the ERROR bit will be raised in the Status Register.

Register 6 - Hookswitch Response Time

Code	Default	Function
0 - 15	2 (i.e. 200ms)	Set Hookswitch timeout period Duration = Code × 100ms.

Table 11 Register 6

The hookswitch timeout period is the time taken between the hookswitch going low and the on-hook condition being recognised by the MA525. It is used to differentiate between short line breaks due to electrical noise (or line polarity reversal) and the user placing the handset on-hook. If the HSW input returns high before the timeout period has elapsed then the on-hook condition is not recognised. The status of the HS bit in the status register reflects the immediate status of the HSW input rather than whether the device recognises the on-hook or off-hook condition. It should be noted that the actual hookswitch response time will vary between the nominal duration set and up to 100ms greater than this (eg. if 200ms is set, the response time is 200-300ms).

Parameters set in Register 6 should not be changed when a hookswitch timeout is occuring, as this may give an unpredictable timeout period. If this occurs, however, the device will behave as normal after the timeout is complete.

Register 7 - Timed Break Recall (Flash) Period

Code	Default	Function
0 - 15	1 (i.e. 100ms)	Set TBR (Flash) period Duration = Code × 100ms.

Table 12 Register 7

If code 0 is loaded, the TBR (Flash) Period will be set to the default value and the ERROR bit will be set in the status register.

Register 8 - Inter-Digit Pause Duration

Code	Default	Function
0 - 15	8 (i.e. 800ms)	Set IDP duration (LD dialling) Duration = Code × 100ms.

Table 13 Register 8

The IDP duration applies only to LD dialling. If code 0 is loaded, the IDP duration will be set to the default value and the ERROR bit will be set in the status register.

Register 9 - Single Tone Output

Code	Default	Function
0-7	Disable	Disable single tone output
8		Enable 697 Hz output
9		Enable 770 Hz output
10		Enable 852 Hz output
11		Enable 941 Hz output
12		Enable 1209 Hz output
13		Enable 1336 Hz output
14		Enable 1477 Hz output
15		Enable 1663 Hz output

Table 14 Register 9

When selected, the single tone output is generated from the DTMF output. The output level is therefore dependent upon whether the particular tone is in the high or low frequency group (see AC characteristics). Once selected, the single tone output is continuous until it is either disabled or until another single tone is selected. Single tones cannot be selected in LD mode.
Single tone outputs are active whether the device is on or off-hook.

During single tone outputs the BUSY bit is not set. In addition, the device outputs (MUTE,MASK and LINE) will remain inactive.

If the DIAL bit is set whilst a single tone is active, the device will behave as if it is dialling (i.e. BUSY bit set, MUTE active et cetera) although the single tone will take priority on the TONE pin. It is therefore important to disable single tones before a DTMF dialling sequence.

Register 10 - Status Register (Read Only)

Bit	Name	Function
0	BUSY	Indicates dialling in progress: 1 = Busy
1	ERROR	Indicates programming error: 1 = Error
2	HS	Indicates hookswitch status: 1 = off-hook 0 = on-hook
3	BUF	Indicates digit buffer status: 0 = available 1 = in use
7	IRQF	Interrupt request set flag: 0 = clear 1 = set

Table 15 Register 10

Bit 0: BUSY
The BUSY bit is active (i.e. set to '1') during dialling of digits, TBR and Pauses in either LD or DTMF modes.

The BUSY bit is automatically reset to '0' when:
1. A dialling sequence is complete.
2. A dialling sequence is terminated by setting the DISCON bit (Reg 2) to 1.
3. A dialling sequence is terminated by an on-hook timeout.

Bit 1: ERROR
In general, the ERROR bit is raised when an illegal operation is performed. Some operations, such as changing certain registers whilst dialling, are not fundamentally illegal but are nevertheless not recommended. Such errors do *not* raise the ERROR flag.

The ERROR bit is always reset by reading the Status Register.

The ERROR bit is set to 1 under the following conditions:

1. When an attempt is made to load illegal digits into the digit buffer (Reg0) while the device is set to LD mode (i.e. A,B,C,D,★or #).
2. When an attempt is made to dial an illegal digit in LD mode (i.e. A,B,C,D,★or #) loaded whilst the device is in DTMF mode .
3. If an attempt is made to load a digit into the dial store while the BUF bit is set to 1.
4. If an attempt is made to load code 0 into registers 4, 7 or 8.
5. When a register addressing error is made (i.e. if a register number greater than 11 is addressed).

Bit 2: HS
The HS bit is set to 1 immediately the HSW input goes high. HS remains high until the HSW input goes low, when it will be reset to 0. The status of the HSW input has no relevance to device operation when in Modem mode, but the HS bit remains operational. If DISCON is invoked during a hookswitch timeout the device will assume the on-hook condition instantly, i.e. DISCON takes priority over the hookswitch timeout.

Bit 3: BUF
When the BUF bit is set to 0, this indicates that a digit (or a TBR or Pause) can be loaded into the dial store via Register 0, the digit buffer (or via Register 2).

When the BUF bit is set to 1 this indicates that the temporary digit buffer is not available for use and that digits should therefore not be loaded. If a digit is loaded while BUF = 1, it will not be accepted and the ERROR bit and IRQF will be set.

The BUF bit is set to 1 under the following conditions:

1. While the MA525 is accepting a digit from the temporary digit buffer to the dial store. A handshaking procedure, as shown in Fig. 6, can be used to load digits from the digit buffer to the dial store. Such handshaking will ensure correct loading of the digits whether or not the MA525 oscillator is running at the time of first loading. Providing that the oscillator is running (see Oscillator Circuit section) handshaking need not be used so long as the buffer timing constraints are observed.
2. When the dial store is full and therefore unable to receive any further digits. As soon as a dial store location becomes available the BUF bit will be reset to 0 and the digit previously held in the buffer will be transferred to the dial store.

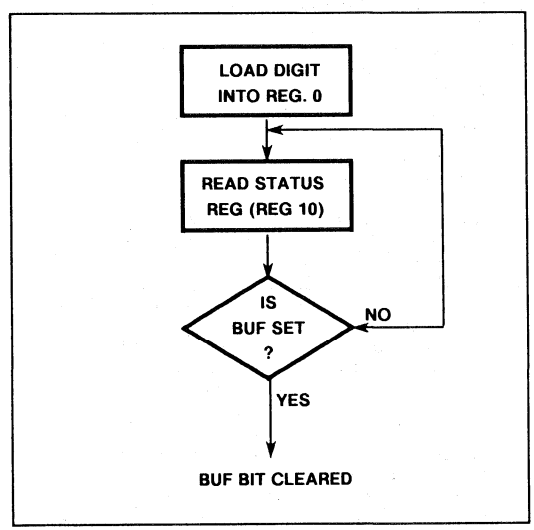


Fig. 6 Digit loading handshaking procedure.

Bit 7: IRQF
The IRQF bit simply reflects the status of the $\overline{IRQ}$ output. The IRQF bit is set to 1 ($\overline{IRQ}$ = 0) under the following conditions:

1. Whenever the ERROR bit is set to 1.
2. Whenever a dialling sequence is completed (but not if DISCON is asserted or the hookswitch is taken low before the sequence is complete).

The IRQF bit and $\overline{IRQ}$ are returned to their inactive states by reading the status register.

Note that if IRQF goes high and is subsequently cleared as a consequence of a good sequence, the Status Register will hold the data relating to the latter (correct) operation and not the former (incorrect) operation.

LAST NUMBER REDIAL FACILITY

The MA525 will dial the previous contents of the dial store if :
(i) No digits are loaded between HSW being timing out (or DISCON being set) and DIAL being set in Phone Mode.(See Fig. 7).
(ii) No digits are loaded between DISCON being set and DIAL being set in Modem Mode.(See Fig. 8).
Note:
(i) Digits cannot be appended to an LNR.
(ii) The presence of a Timed Break Recall (TBR) or Access Pause does not affect the LNR – they are simply treated as another digit.

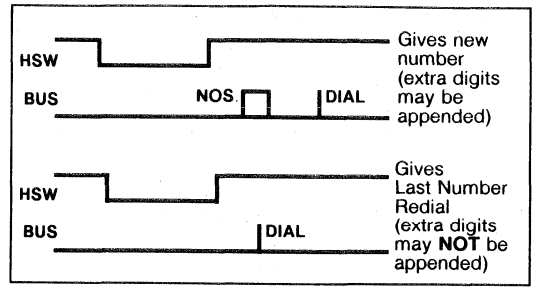


Fig.7 LNR protocol - Phone Mode

OSCILLATOR CIRCUIT

The oscillator circuit requires an external 560kHz ceramic resonator between OSC and V_{SS}. No other components should be used. Please see your resonator supplier who will recommend a suitable resonator type. The OSC pin may also be driven by an external logic signal if required.

Under normal MA525 operation, the oscillator will be started during dialling or digit loading sequences and shut-down afterwards in order to conserve power and reduce possible crosstalk to speech or other sensitive circuits.

Thus the oscillator will be started by:

1. The presence of a digit in the digit buffer. (whilst off-hook or in Modem mode).
2. DIAL bit being set (whilst off-hook or in Modem mode).
3. Whilst performing a hookswitch timeout (whilst in Phone mode only).
4. Beginning a Single Tone output.

The oscillator will be shut-down following:

1. A hookswitch timeout (in Phone mode only).
2. DISCON bit being set.
3. Completion of a dialling sequence.
4. BUF being cleared. Note that if a 23rd digit is loaded, it will reside in the buffer until a space becomes available for it in the dial store. In the meantime, BUF will be set and the oscillator will run continuously. To ensure minimum crosstalk with any speech circuitry, it is advisable to avoid this situation.
5. Ending a Single Tone output.

Note that reading the Status Register will not restart the oscillator. Hence data held in this Register will not be updated after the oscillator has been shut-down.

Since the oscillator is stopped whilst the hookswitch is down in Phone mode it is not possible to load digits into the dial store. A single digit can be held in the buffer, however, until the device is next taken off-hook. Digits may, however, be loaded at any time whilst in Modem mode irrespective of hookswitch and DISCON status.

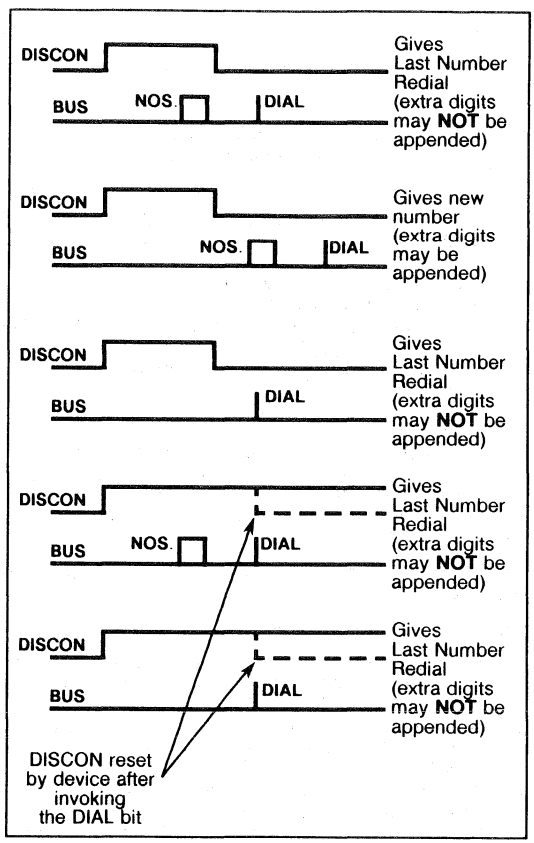


Fig.8 LNR protocol - Modem Mode

REGISTER SUMMARY

Reg no.	Name	Bit 3 (MSB)	Bit 2	Bit 1	Bit 0 (LSB)
1	DIAL CONDITIONS	**MODE** 0 PULSE 1 DTMF	**DIAL SPEED** 0 NORM 1 DOUBLE	**B/M RATIO** 0 = 2:1 1 = 3:2	**USE** 0 PHONE 1 MODEM
2	CONTROL REGISTER	**TBR**	**ACCESS PAUSE**	**DISCON**	**DIAL**
3	OUTPUT CONFIGURATION	**MASK POLARITY** 0 NORM 1 INV	**MUTE POLARITY** 0 NORM 1 INV	**LINE POLARITY** 0 NORM 1 INV	**IE** 0 DISABLE 1 ENABLE
10	STATUS REGISTER	**BUF** 0 AVAIL 1 IN USE	**HS** 0 OFFHK 1 ONHK	**DIGIT ERROR**	**BUSY BIT**

Table 16 Summary of registers 1, 2. 3 and 10 functions

Reg. no.	Function	Coding
4	ACCESS PAUSE DURATION	CODE × 500ms
5	DTMF DURATION	CODE × 6.67ms
6	HOOKSWITCH RESPONSE TIME	CODE × 100ms
7	TBR (FLASH) DURATION	CODE × 100ms
8	INTER-DIGIT PAUSE DURATION	CODE × 100ms

Table 17 Summary of registers 4, 5, 6, 7 and 8 functions

Code	Register 9 - Single Tone Output
0-7	Disable single tone output
8	Enable 697 Hz output
9	Enable 770 Hz output
10	Enable 852 Hz output
11	Enable 941 Hz output
12	Enable 1209 Hz output
13	Enable 1336 Hz output
14	Enable 1477 Hz output
15	Enable 1663 Hz output

Table 18 Register 9 summary

PULSE DIALLING IN PHONE MODE

The MASK output is provided in order to disable the speech circuit during LD (Pulse) dialling. Consequently, the MASK output is normally at logic '0' in the off-hook condition, but changes to logic '1' during LD dialling. MASK also changes to logic '1' in order to signal a Timed Break Recall (Flash) to the line.

LD dialling is signalled on the LINE output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the LINE output sits at logic '0'.

Both MUTE and TONE outputs remain low during LD dialling. LINE, MUTE and MASK outputs may be inverted independently if desired.

If the HSW input goes low whilst dialling, the LINE and MASK outputs continue as normal until the hookswitch timeout occurs. If the hookswitch goes high again before the timeout, LINE and MASK will continue uninterrupted. The BUSY bit (Reg 10) will remain high until either the dialling sequence finishes internally or until a hookswitch timeout occurs (whichever comes first).

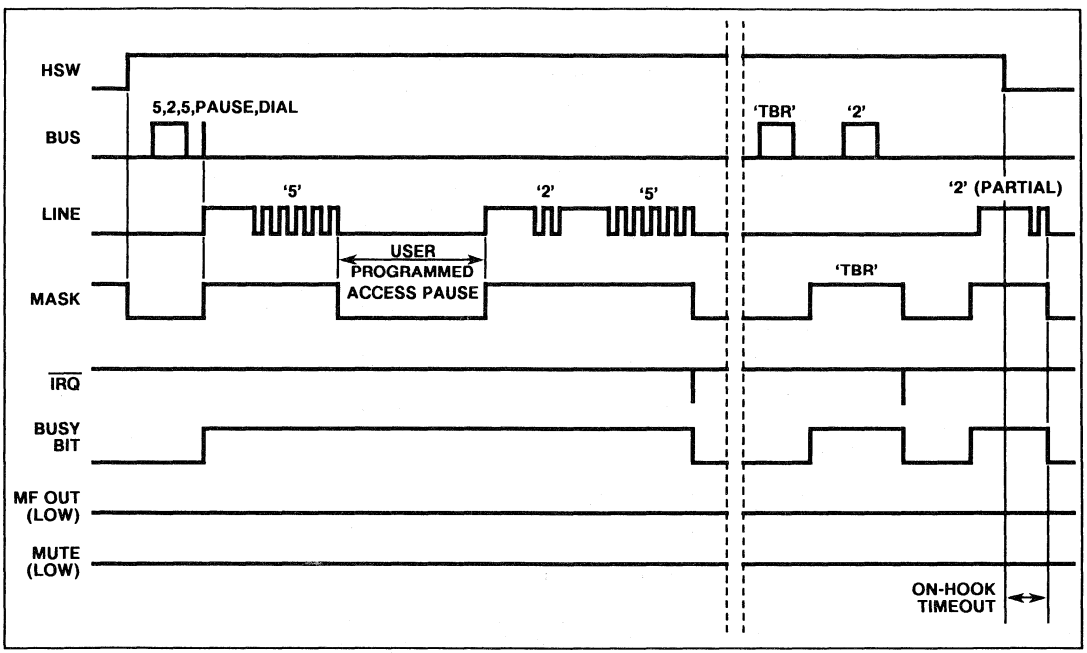
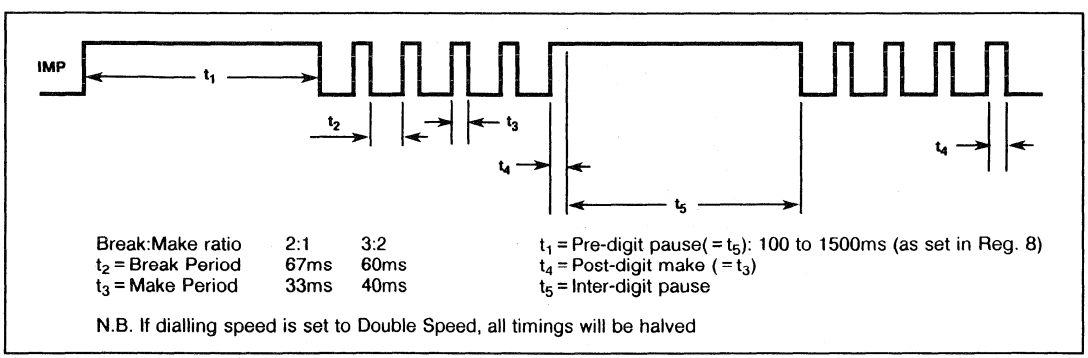


Fig.9 LD/phone mode timing diagram



Break:Make ratio	2:1	3:2
t_2 = Break Period	67ms	60ms
t_3 = Make Period	33ms	40ms

t_1 = Pre-digit pause(= t_5): 100 to 1500ms (as set in Reg. 8)
t_4 = Post-digit make (= t_3)
t_5 = Inter-digit pause

N.B. If dialling speed is set to Double Speed, all timings will be halved

Fig.10 Timing data

PULSE DIALLING IN MODEM MODE

The MASK output is provided in order to disable the speech circuit during LD dialling. Consequently, the MASK output is normally at logic '0' in the off-hook condition, but changes to logic '1' during LD dialling. MASK also changes to logic '1' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and TONE remain low during LD dialling. LINE, MUTE and MASK may be inverted independently if desired.

The status of the HSW input is irrelevant in Modem mode. However, HSW status can still be read from register 10.

The LINE output is used to control the on/off-hook status *and* for LD dialling. The line will be seized when dialling starts. A break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. After dialling finishes the LINE output will remain high until the line is disconnected by setting the DISCON bit to '1'.

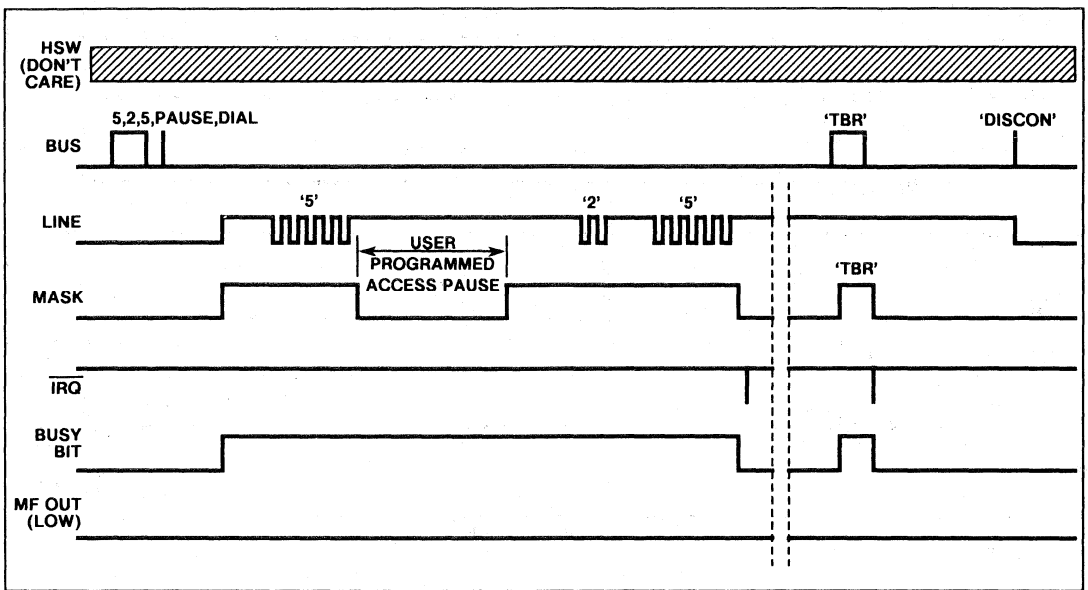


Fig.11 LD/modem mode timing diagram

DTMF DIALLING IN PHONE MODE

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The LINE output remains low during tone transmission.

The MF OUT output rises to its DC level as soon as the MODE bit in register 1 is set and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

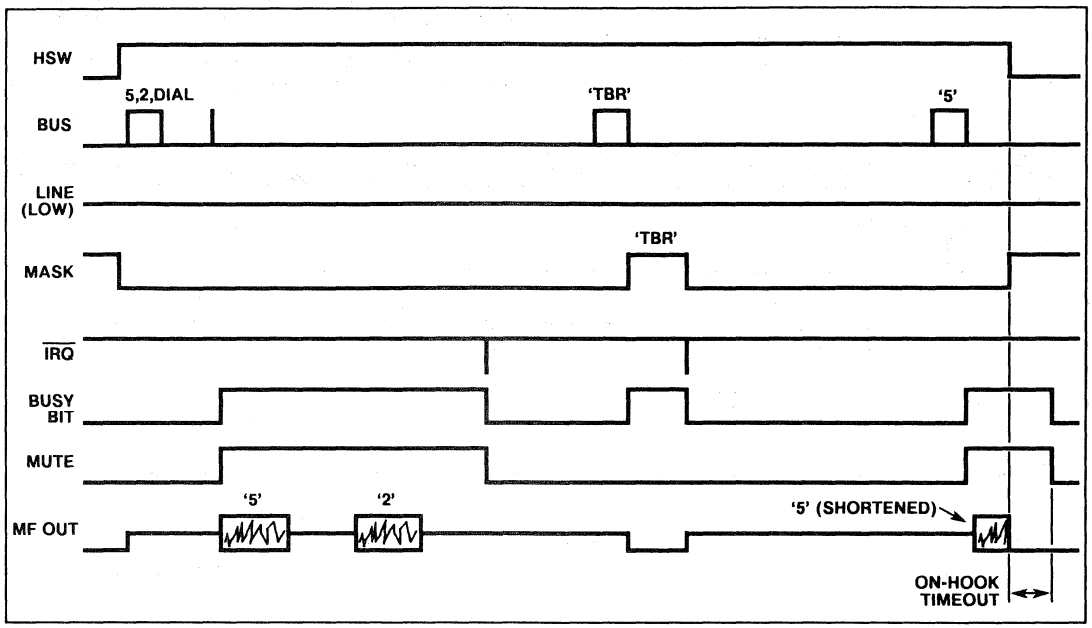


Fig.12 DTMF/phone mode timing diagram

	1209Hz	1336Hz	1477Hz	1633Hz
697Hz	1	2	3	A
770Hz	4	5	6	B
852Hz	7	8	9	C
941Hz	*	0	#	D

Table 19 Tone frequencies

Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	- 0.07	- 0.10	+ 0.19	- 0.15	- 0.17	- 0.20	- 0.22	- 0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 20 Tone frequenciy accuracy

PULSE DIALLING IN MODEM MODE

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The LINE output is used to control the on/off hook status whilst MF OUT is used for tone transmission.

The MF OUT output rises to its DC level as soon as the MODE bit is set and remains there during tone bursts. This is to avoid transients at the beginning and end of tone bursts.

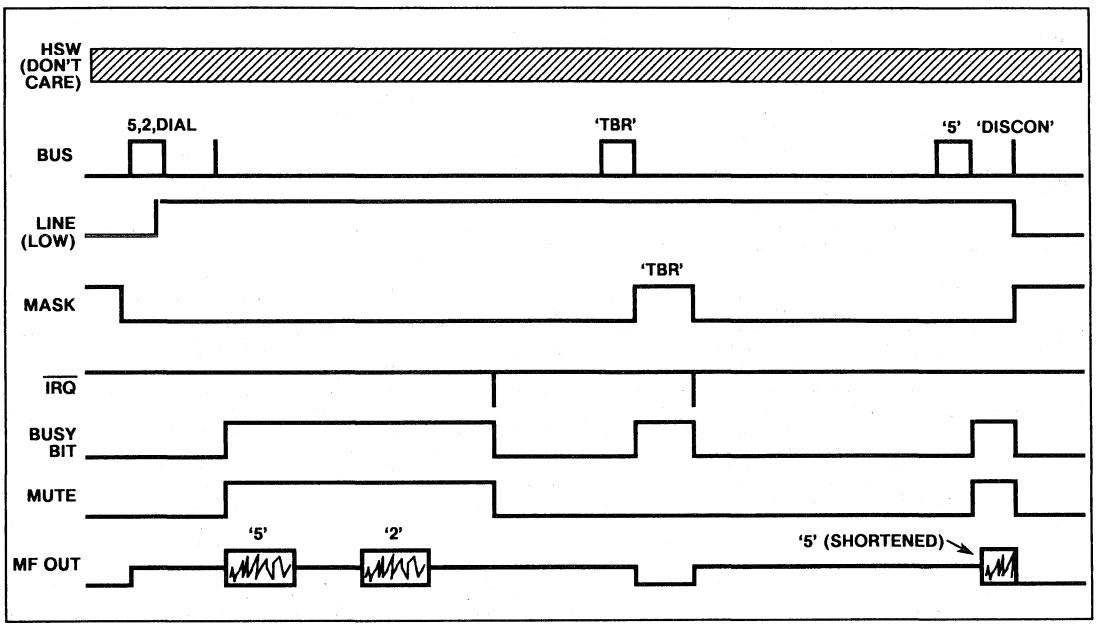


Fig.13 DTMF/Modem mode timing diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): T_{amb} = 25°C

DC CHARACTERISTICS at V_{DD} = 2.5V

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply Current:	On-hook		<0.2	5.0	μA	V_{DD} = 2.0V. See note 1.
	Off-hook		1.5		μA	MF OUT low
	MF tone sending			1.0	mA	
	LD impulsing			200	μA	
Output high voltage (MASK, MUTE and LINE outputs)		2.2			V	I = –1mA
Output low voltage (MASK, MUTE and LINE outputs)				0.3	V	I = +1mA
MF OUT DC level during tone sending			$0.5V_{DD}$		V	
MF OUT output resistance			15	20	kΩ	
Microprocessor interface:	Input high	-	2.0	V_{DD}	V	
	Input low	-	0	0.5	V	
	Output high	2.3	-	-	V	I = –50μA
	Output low	-	-	0.2	V	I = +50μA
$\overline{IRQ}$ Output	Output low	-	-	0.2	V	I = +50μA
	Output high leakage	-	-	1	μA	

NOTE 1. Specially tested versions with guaranteed lower on-hook supply current are available.

DC CHARACTERISTICS at V_{DD} = 5V

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply Current:	On-hook		1.5		μA	MF OUT low
	MF tone sending		0.5	2.0	mA	
	LD impulsing			0.5	mA	
Output high voltage (MASK, MUTE and LINE outputs)		4.55	4.8		V	I = -10mA
Output low voltage (MASK, MUTE and LINE outputs)			0.2	0.45	V	I = +10mA
Microprocessor interface:	Input high	-	2.0	V_{DD}	V	
	Input low	-	0	0.8	V	
	Output high	4.6	-	-	V	I = -1mA
	Output low	-	-	0.4	V	I = +1mA
$\overline{IRQ}$ Output	Output low	-	-	0.4	V	I = +1mA
	Output high leakage	-	-	1	μA	

NOTE 2. All other characteristics are as specified at V_{DD} = 2.5V given on page 1-89

AC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Tone output at V_{DD} = 2.5V:	Low group	285	320		mV rms	No load
	High group		405	455	mV rms	No load
Tone output at V_{DD} = 5V:	Low group	570	640		mV rms	No load
	High group		810	910	mV rms	No load
High-to-Low group amplitude ratio (pre-emphasis)		1.5	2	2.5	dB	All V_{DD}, see note 3.
Total harmonic distortion:	0-4 kHz		1.5		%	All V_{DD}
	0-10 kHz		2.5		%	All V_{DD}
	0-50 kHz		5.0		%	All V_{DD}
	0-200 kHz		6.5	10	%	All V_{DD}
Oscillator start-up time			< 0.1	1	ms	

NOTE 3. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition		Min.	Typ.	Max.	Units	Notes
Supply Voltage:	On-hook	1.8		5.7	V	For memory retention
	Off-hook	2.4		5.7	V	
Hookswitch Input:	On-hook			$0.2V_{DD}$	V	
	Off-hook	$0.8V_{DD}$			V	
Oscillating frequency			560		kHz	
Digit load to dial store accept time (BUF high time)				36	μs	See note 4

NOTE 4. Assumes oscillator is running. If oscillator is not running, add start-up time given in AC Characteristics above.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}–V_{SS}	- 0.3 to + 6.5V
Voltage on any pin (except HSW)	V_{SS} - 0.3V to V_{DD} + 0.3V
Voltage on HSW pin (See note 5)	V_{SS} - 0.3V min.
Current at any pin (except HSW)	± 1mA
Storage temperature	-55°C to + 125°C
Operating temperature range	-10°C to + 55°C

NOTES

5. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300μA max. no damage will occur.

6. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Section 2
PCM Circuits

DS3127-1.0

MJ1410

8 BIT FORMAT CONVERTER

The MJ1410 is realised in N-channel MOS technology and operates from a single 5V supply. The circuit can be clocked from d.c. up to 2.5MHz and has 3-state output buffers capable of driving two LSTTL loads. All inputs are TTL compatible.

The MJ1410 performs the complementary functions of serial-to-parallel and parallel-to-serial data conversion on 8 bits of data. Both these conversions are achieved using the same time-position matrix, which has eight inputs and eight outputs.

An 8-bit parallel word clocked into the eight inputs appears as a serial 8-bit data stream on one of the eight outputs. Successive parallel words at the inputs appear as serial data streams on each of the eight outputs in turn.

Conversely, a serial 8-bit data stream on one of the eight inputs appears as an 8-bit parallel word on the eight outputs. Successive parallel words appearing at the eight outputs correspond to the serial data on each of the eight inputs in rotation.

The conversion can be 'programmed' to start in any register by setting the appropriate binary value on the counter pre-load inputs and applying a pulse to the Sync input. If the loading sequence produced by the counter is not required it can be disabled by connecting 'clock' to 'sync'. At each positive clock edge the register loaded will depend on the data on the counter inputs on the previous positive clock edge.

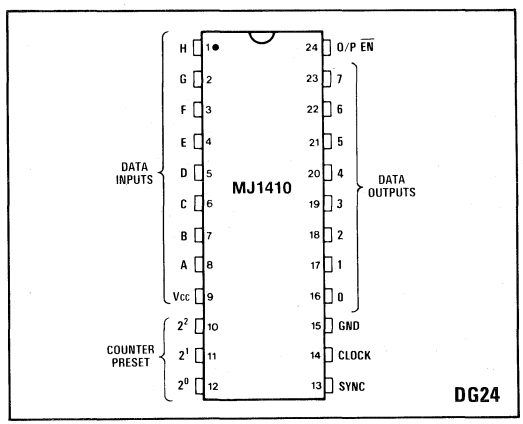


Fig.1 Pin connections

FEATURES

- Single 5V supply.
- Three-state outputs.
- All inputs TTL compatible.

FUNCTIONAL DESCRIPTION

Pin No.	Title	Function
1	H	Data i/p H
2	G	Data i/p G
3	F	Data i/p F
4	E	Data i/p E
5	D	Data i/p D
6	C	Data i/p C
7	B	Data i/p B
8	A	Data i/p A
	Data inputs	See Figs. 3 and 4
9	Vcc	Positive supply, 5V ± 5%
10	2^2	Counter preset i/p bit 2
11	2^1	Counter preset i/p bit 1
12	2^0	Counter preset i/p bit 0
		The counter is preset to the data on these i/ps on the 3rd positive clock edge following a negative edge on the 'sync' input.
13	SYNC	A negative edge on this i/p initiates the counter preset sequence which causes the conversion cycle to start in the register which corresponds to the binary value of the counter preset i/ps.
14	CLOCK	System clock
15	GND	Zero volts
16	0	Three state data o/p '0'
17	1	Three state data o/p '1'
18	2	Three state data o/p '2'
19	3	Three state data o/p '3'
20	4	Three state data o/p '4'
21	5	Three state data o/p '5'
22	6	Three state data o/p '6'
23	7	Three state data o/p '7'
	Data outputs	See Figs. 3 and 4
24	O/P $\overline{EN}$	A logic '1' on this i/p forces all the data outputs to a high impedance state.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{CC} = 5V, T_{amb} = 22°C ± 2°C, Test circuit: Fig.6.

Supply voltage V_{CC} = 5V ± 10%, Ambient operating temperature T_{amb} = 10°C to +70°C

STATIC CHARACTERISTICS

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level I/P voltage	V_{IL}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24	-0.3		0.8	Volts	
High level I/P voltage	V_{IH}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24	2.5		V_{CC}	Volts	
Low level I/P current/high level I/P current	I_{IN}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24		1	50	µA	
Low level O/P voltage	V_{OL}	16,17,18, 19,20,21, 22,23			0.5	Volts	I_{SYNC} = 1.6mA
High level O/P voltage	V_{OH}	16,17,18, 19,20,21, 22,23	2.5			Volts	I_{SOURCE} = 100uA
Low level O/P current sink capability	I_{OL}	16,17,18, 19,20,21, 22,23	-1.6			mA	
High level O/P current source capability	I_{OH}	16,17,18, 19,20,21, 22,23	100			µA	
OFF state O/P current	$I_{OFF\ L}$	16,17,18, 19,20,21, 22,23			40	µA	V_{OUT} = GND
	$I_{OFF\ H}$	16,17,18, 19,20,21, 22,23			-40	µA	V_{OUT} = V_{CC}
Power dissipation	P_{DISS}		90		500	mW	V_{CC} = 5.5V

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max.clock frequency	$F_{max.}$	2.4		10	MHz	
Min. clock frequency	$F_{min.}$	0			MHz	
Sync. pulse width (positive)	t_{SPP}	60			ns	Fig. 6
Sync. pulse width (negative)	t_{SPN}	100			ns	Fig. 6
Lead of sync. clocking edge on positive clock edge	t_{SL}	130			ns	Fig. 6
Set up time of counter inputs (2^0,2^1,2^2)	t_{SC}	70			ns	Fig. 6
Hold time of counter inputs	t_{HC}	60			ns	Fig. 6
Set up time of data inputs (A-H)	t_{SD}	80			ns	Fig. 6

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Hold time of data inputs	t_{HD}	85			ns	Fig. 6
Propagation delay, data out valid from output $\overline{\text{ENABLE}}$ low	t_{PDE}			100	ns	Fig. 6
Propagation delay, data out disabled from output $\overline{\text{ENABLE}}$ high	t_{PDD}			100	ns	Fig. 6
Propagation delay, clock to data out valid	t_{PCD}			200	ns	Fig. 6

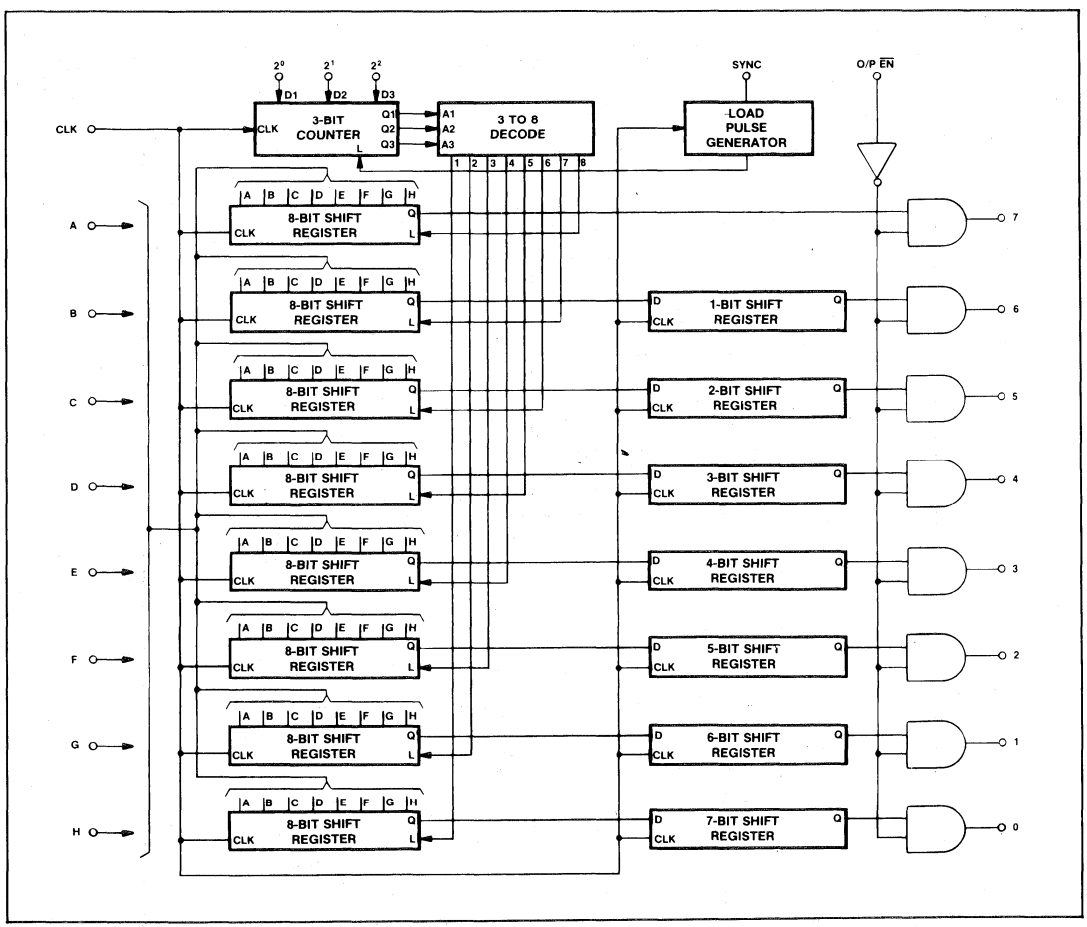


Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin w.r.t. ground = 7V max.
Storage temperature = -55°C to +125°C

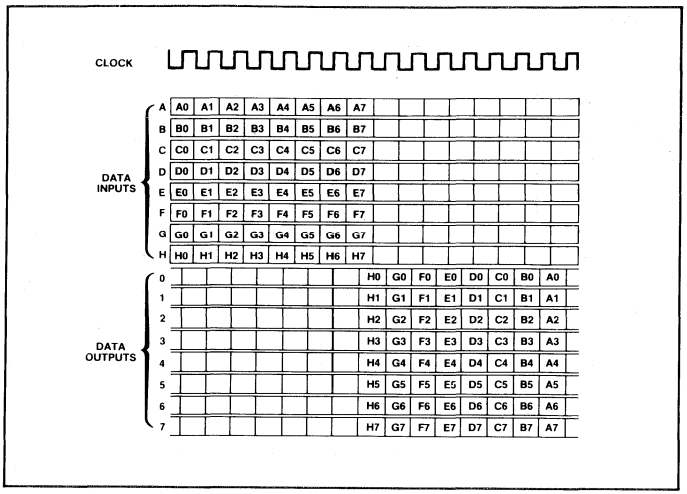


Fig.3 Data conversion

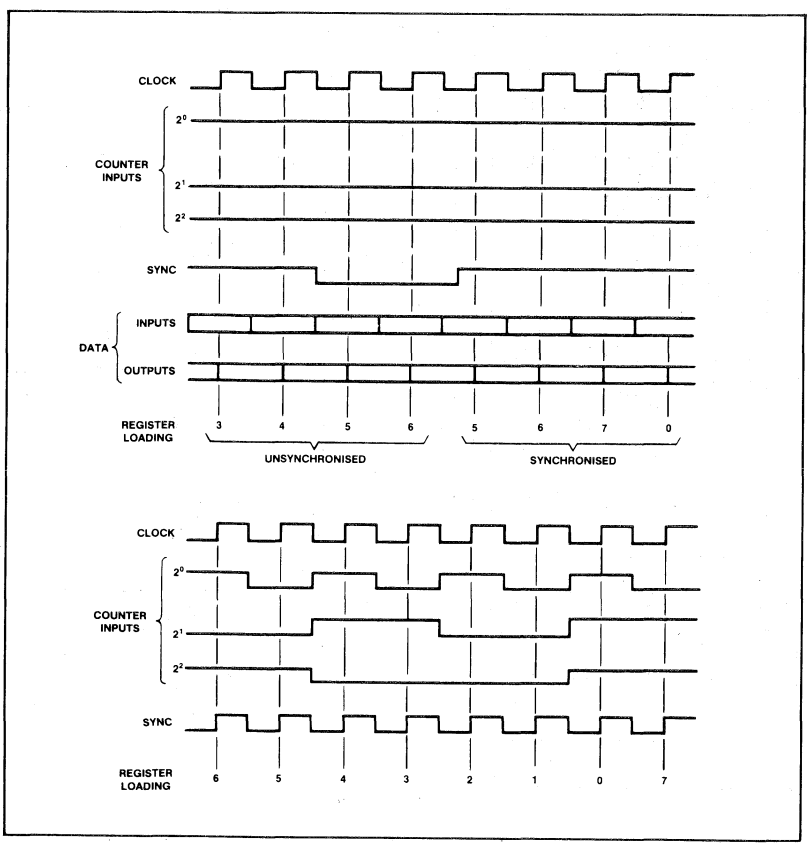


Fig.4 Input and output waveforms

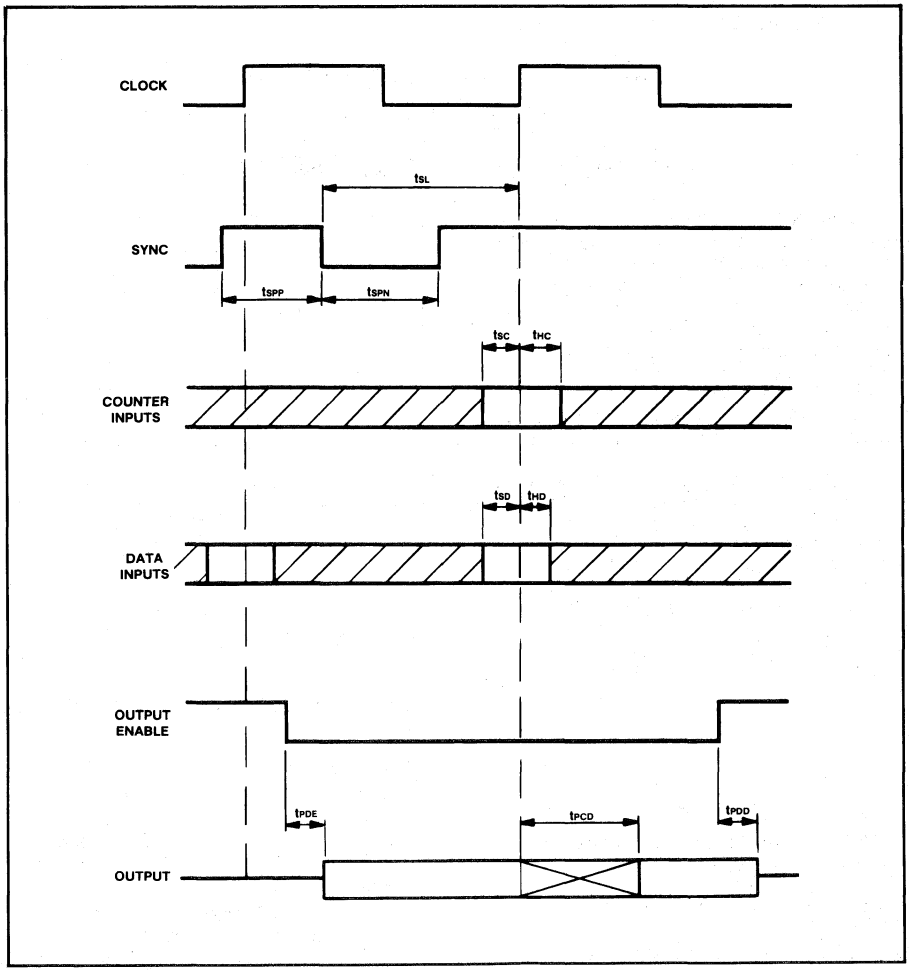


Fig.5 Timing details

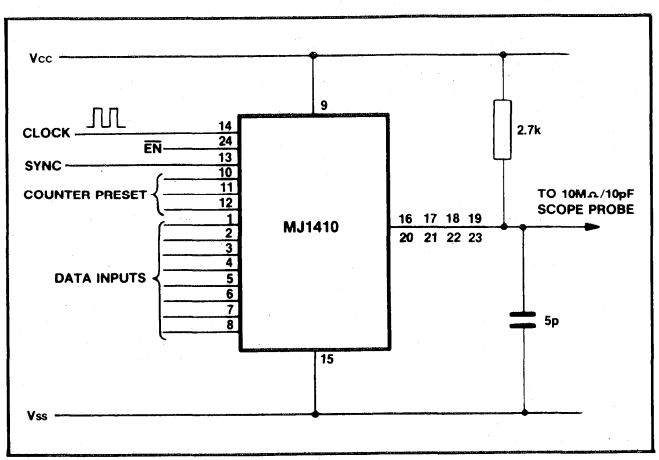


Fig.6 Test conditions

DS3129-1.0

2 MBIT PCM SIGNALLING CIRCUIT

MJ 1444

TIMESLOT ZERO TRANSMITTER

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1444 generates the synchronising word in accordance with CCITT recommendations G732. The MJ1445 has been designed to detect this synchronising word when received at the remote end of the transmission system.

The synchronising word is injected onto the PCM data highway during time slot 0 in alternate frames. The spare time slot 0 data bits, bit 1 in every frame and bits 3 to 8 inclusive in alternate frames (i.e. those not containing the synchronising word) are available as parallel inputs and are output onto the PCM data highway.

The data output of the MJ1444 is 'open collector' and can be wire-OR'd directly onto the highway.

The device also provides a time slot 0 channel pulse 'TS0', time slot 0 non-sync. frame 'TS0 $\overline{SF}$', and time slot 16 'TS16' outputs.

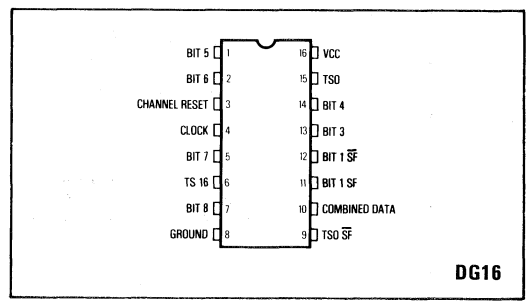


Fig.1 Pin connections

FEATURES

- 5V ± 5% Supply — 20 mA Typical
- Fully Conforms to CCITT Recommendation G732
- Outputs Directly Onto PCM Data Highway
- Provides Both Time Slot 0 and Time Slot 16 Channel Pulses
- All Inputs and Outputs are TTL Compatible

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

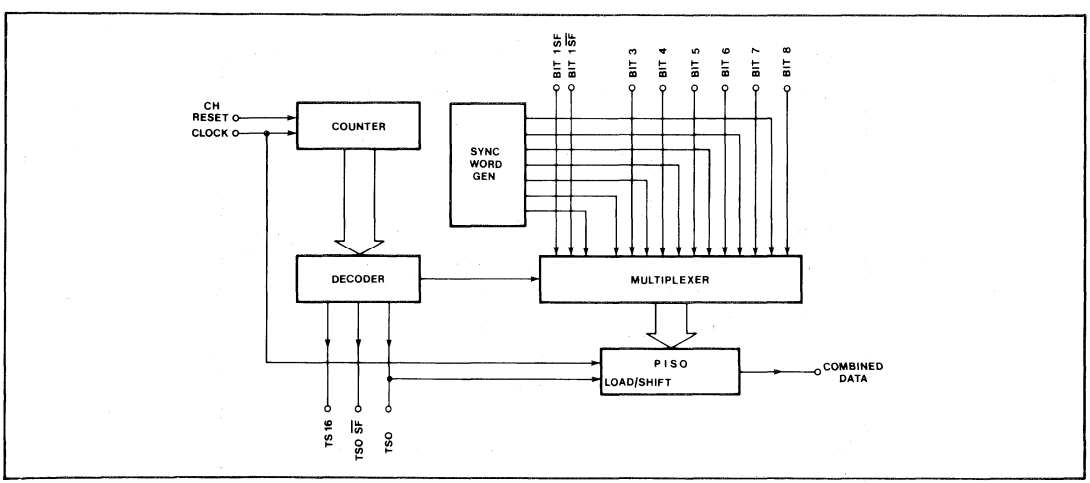


Fig.2 MJ1444 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient operating temperature -10°C to +70°C

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	1, 2, 3, 4, 5, 7, 11, 12, 13, 14.	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	μA	
High level input voltage	V_{IH}	11	2.4		V_{CC}		
Low level output voltage	V_{OL}	6, 9, 15 10			0.5 0.7	V V	$I_{sink} = 2mA$ $I_{sink} = 5mA$
High level output voltage	V_{OH}	6, 9, 15	2.8			V	$I_{source} = 200\mu A$
High level output leakage current	I_{OH}	10			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max clock frequency	F_{max}	3			MHz	
Propagation delay, clock to TS0, TS0 $\overline{SF}$, TS16 and combined data outputs.	t_P	80		200	ns	See Figs.5 and 6
Set up time channel reset to clock	T_{S1}	100		450	ns	$f_{clock} = 2.048MHz$
Hold time of channel reset input	t_{H1}	20		400	ns	
Set up time of bit 1 (SF) to datum B	t_{S2}	100			ns	
Hold time of bit 1 (SF) wrt datum B	t_{H2}	300			ns	
Set up time of bit 1 ($\overline{SF}$) and data bits 3—8 to datum B	t_{S2}	100			ns	
Hold time of bit 1 ($\overline{SF}$) and data bits 3—8 wrt datum B	t_{H2}	300			ns	

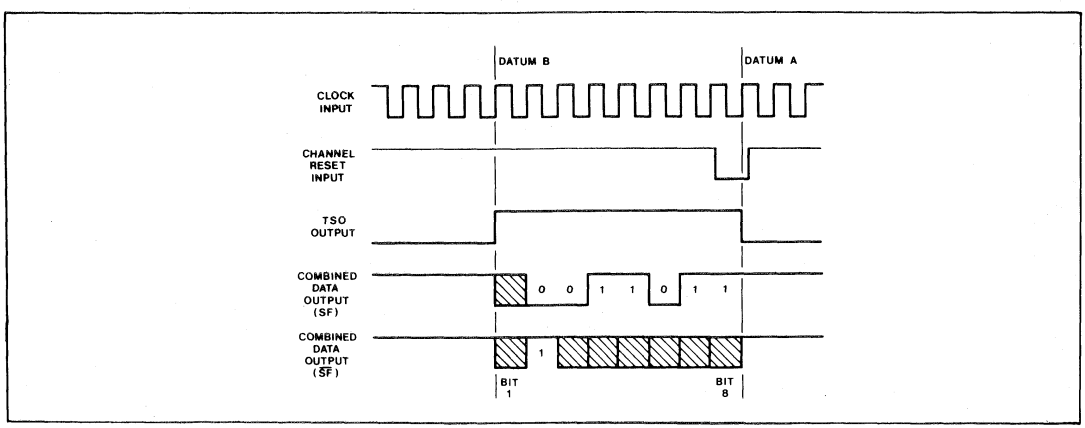


Fig.3 Data timing

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1, 2, 5, 7, 13, 14. Bits 3 to 8

Parallel data on these inputs is asynchronously loaded into bits 3 to 8 of the PISO shift register for transmission during Time slot 0 of non-sync. frames.

3. Channel Reset

A low going pulse at this input synchronises the MJ1444 with the other devices at the transmit end of the PCM link. It may be applied as a start pulse or repeated at the same instant in successive frames.

4. Clock

System clock input (2.048MHz for a 2 Mbit PCM system).

6. TS16

This output provides a positive pulse equivalent to 8 clock periods during time slot 16 of every 30 + 2 channel PCM frame.

8. GND

Zero volts.

9. TS0 $\overline{SF}$

This output provides a positive pulse equivalent to 8 clock periods during time slot 0 of non-sync. frames.

10. Combined data

This 'open collector' output injects the contents of the PISO shift register onto the PCM data highway during time slot 0 in successive frames. The contents of the PISO shift register are defined as follows:

	Bit 1	2	3	4	5	6	7	8
Sync. Frame	X	0	0	1	1	0	1	1
Non-sync. frame	X	1	X	X	X	X	X	X

X — indicates that these bits may be set according to the parallel data inputs.

11. Bit 1 SF

Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of sync. frames.

12. Bit 1 $\overline{SF}$

Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of non-sync. frames.

15. TS0

This output provides a positive pulse equivalent to 8 clock period during time slot 0 of every 30 channel PCM frame.

16. V_{CC}

Positive supply, 5V ±5%.

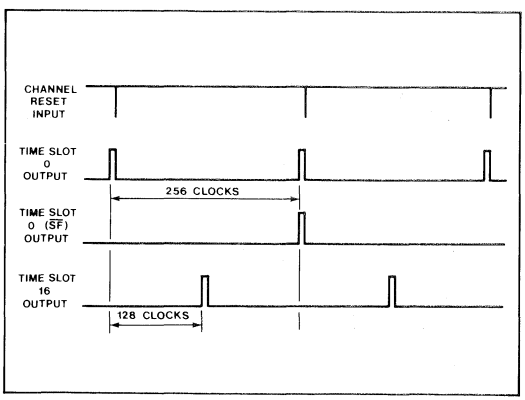


Fig.4 Sync. timing

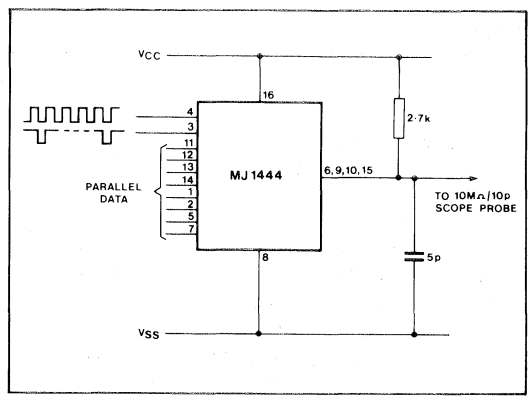


Fig.5 Test conditions (all outputs)

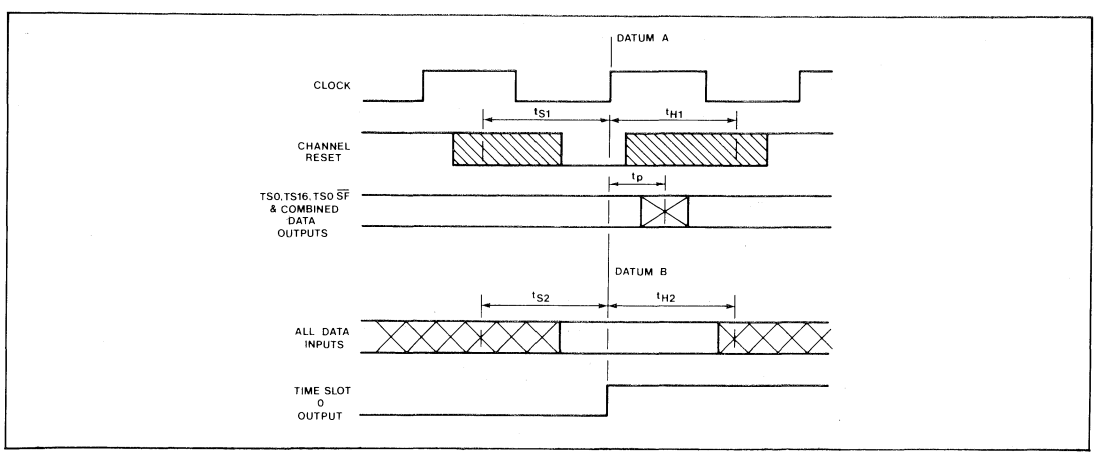


Fig.6 Timing definitions

DS3130-1.0

2 MBIT PCM SIGNALLING CIRCUIT

MJ1445

TIMESLOT ZERO RECEIVER

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 MBit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1445 establishes synchronisation by detecting the synchronising word when it is received at the remote end of the transmission system. The MJ1444 has been designed to generate this synchronisation word at the sending end of the system in accordance with CCITT recommendation G732.

Corruption of individual synchronisation words is signified by an 'Error' output, loss of synchronisation is indicated by a 'Sync Alarm' output and follows CCITT G732 in that loss of synchronism is assumed when 3 consecutive synchronisation words have been received with errors.

The 'Channel Reset' output goes low for the first period of the clock after time slot 0 in sync frames whenever the MJ1445 has established that the receiver terminal is in synchronisation in order that the rest of the receiver terminal may be reset.

The 'TSO' output is high for a period of 8 bits starting from the end of the first bit of the synchronising word. The spare data bits from the synchronising word are provided as parallel outputs.

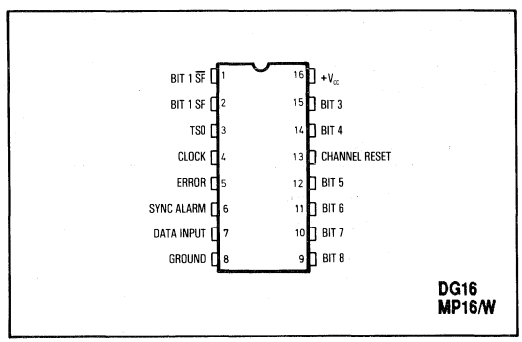


Fig.1 Pin connections

FEATURES

- 5V ±5% Supply – 20 mA Typical.
- Conforms to CCITT Recommendation G732
- Synchronising Word Error Monitor
- Out of Sync. Alarm
- All Inputs and Outputs are TTL Compatible

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd – 0.3V
Outputs	Vcc, Gnd –0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

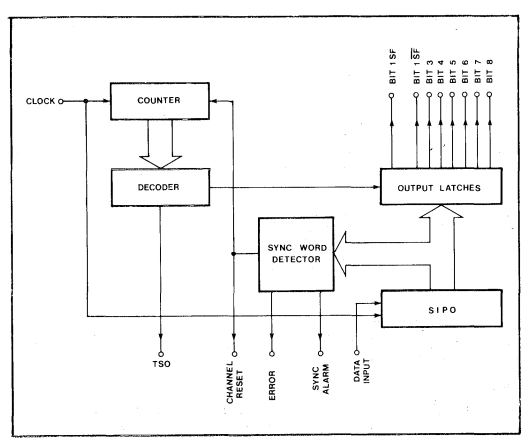


Fig.2 Block diagram MJ1445

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient temperature, $T_{amb} = -10°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	4, 7	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	4, 7		1	50	μA	
High level input voltage	V_{IH}	4, 7	2.4		V_{CC}	V	
Low level output voltage	V_{OL}	1, 2, 3, 5, 6 9, 10, 11, 12 13, 14, 15			0.5	V	$I_{sink} = 2mA$
High level output voltage	V_{OH}		2.8				$I_{source} = 200\mu A$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. clock frequency	f_{max}	2.2			MHz	
Input delay of data input	$t_{d\ data}$	20		200	ns	$f_{clock} = 2.048MHz$
Propagation delay, clock to TS0 output	$t_{d\ TS0}$	40		200	ns	Fig.3
Propagation delay clock to error output, sync alarm and CH. Reset output high	t_d	50		400	ns	Fig.3
Propagation delay, clock to CH. Reset output low ($T - t_p$)	t_p	100		450	ns	Fig.3
Propagation delay clock to spare bits	$t_{d\ SB}$	50		300	ns	Fig.3

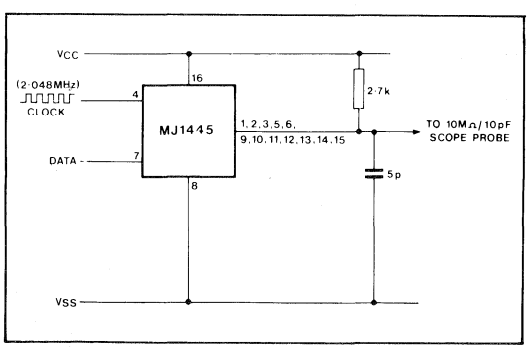


Fig.3 Test conditions, all outputs

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. Bit 1 $\overline{SF}$
This output is set to the level of data bit 1 during time slot 0 of non sync frames. The data becomes true on the first falling edge of the clock during TS1.

2. Bit 1 SF
This output is set to the level of data bit 1 during time slot 0 of sync frames. The data becomes true on the first falling edge of the clock during TS1.

3. TS0
This output provides a positive pulse of 8 clock periods in every frame starting from the end of the first bit of the synchronising word of the received data.

4. Clock
System clock input (2.048MHz for a 2MBit PCM system).

5.Error
This output goes high at the end of time slot 0 in the 2nd sync frame following the frame with sync word errors. If consecutive sync words occur with errors this output will remain high. If a sync alarm is generated this output will remain high until sync is regained.

6. Sync Alarm
This output goes high at the end of time slot 0 output in the 3rd consecutive sync frame containing sync word errors. It returns low at the end of TS0 output in the 3rd consecutive frame received correctly (sync and non sync).

7. Data input
Serial data (2MBit/s) at this input is clocked through the SIPO shift register and examined by the sync word detector.

8. GND
Zero volts

9, 10, 11, 12, 14, 15. Bits 3 to 8
These parallel outputs are set to the level of the spare data bits (3 to 8) of time slot 0 of non sync frames. The data becomes true on the first falling edge of the clock during TS1.

13. Channel reset
This output goes low for the first period of the clock after time slot 0 of the received data as long as synchronisation has been established. This pulse can be used to reset the rest of the receiver terminal.

16. V_{CC}
Positive supply $5V \pm 5\%$.

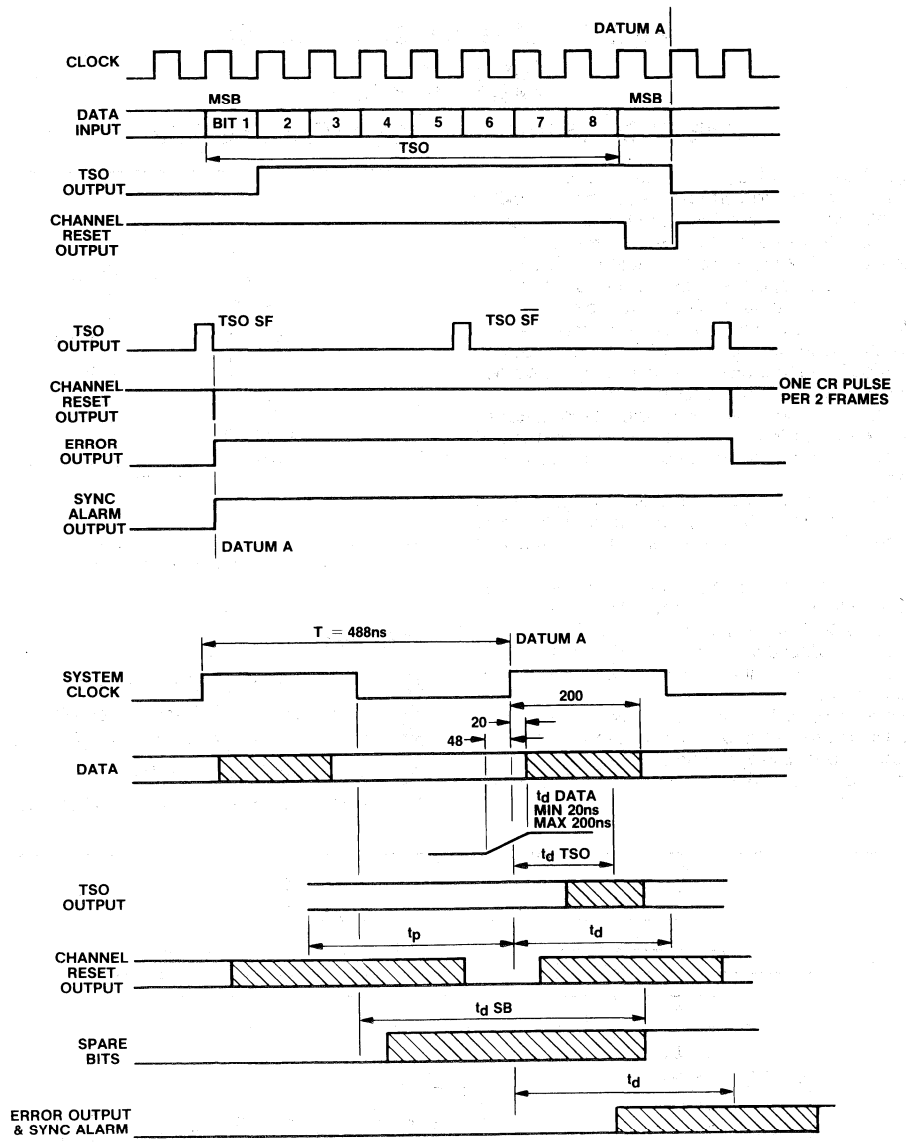


Fig.4 Timing diagram and output waveforms

DS3131-1.0

2 MBIT PCM SIGNALLING CIRCUIT

MJ1446

TIME SLOT 16 RECEIVER AND TRANSMITTER

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1446 has two modes of operation dependent on the state of the mode control input. With the mode control high the device is in the transmit mode and with the mode control low the device is in the receive mode.

In the transmit mode the device accepts 64kbits/sec signalling information in either binary or AMI format and outputs it at 2Mbits/sec on to the digital highway during time slot 16.

In the receive mode the device accepts 2Mbit/sec information from the digital highway, during time slot 16 and output is at 64kbits/sec in both binary and AMI format.

In both receive and transmit mode there is an AMI coded clock output, AMI output and $\overline{\text{AMI}}$ output which conforms to CCITT recommendation no G372 for a 64kbits/sec contradirectional interface. The alarm inhibit input causes the 8kHz timing signal to be removed from the AMI clock output.

The device is reset in both modes by a time slot 16 channel pulse and the alarm output provides an indication that the internal counter is operating correctly.

Also provided are 64kHz, 16kHz and 8kHz clock outputs.

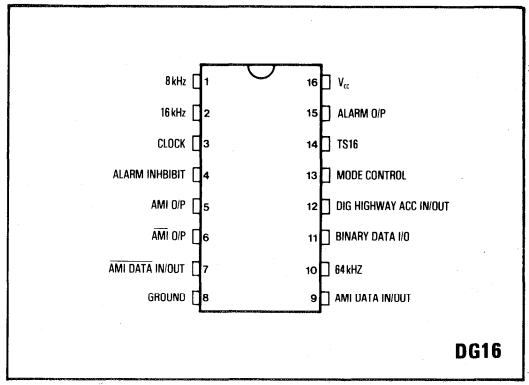


Fig.1 Pin connections

FEATURES

- 5V ±5% Supply — 20mA Typical
- Conforms to CCITT Recommendations
- Provides Both AMI and Binary Format Data Outputs
- Single Chip Receive or Transmit
- All Inputs and Outputs are TTL Compatible.

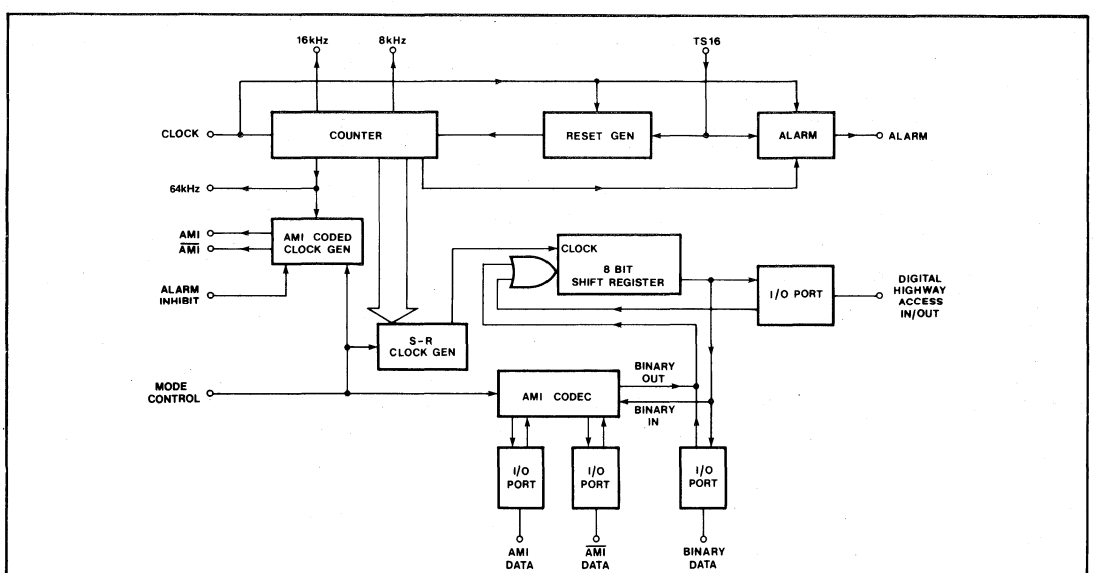


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC} = 5V ± 0.25V, Ambient temperature T_{amb} = -10°C to +70°C,

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	3, 4, 7, 9, 11, 12, 13, 14	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	μA	
High level input voltage	V_{IH}	11	2.4		V_{CC}	V	
Low level output	V_{OL}	1, 2, 5, 6, 7, 9, 10, 11, 15			0.5	V	I_{sink} = 2mA
		12			0.5	V	I_{sink} = 5mA
High level output voltage	V_{OH}	1, 2, 10, 5, 6, 15	2.8			V	I_{source} = 200μA
High level output leakage current	I_{CH}	7, 9, 11, 12			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20		mA	V_{CC} = 5.25V

Dynamic Characteristics (f_{clock} = 2.048MHz)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Propogation delay clock to data out to digital highway	t_p	20		200	ns	Fig.7
Propogation delay clock to 64kHz out	t_p	20		200	ns	Fig.7
Input delay, clock to digital highway access	$t_{d\,DATA}$	20		200	ns	
Input delay, clock to time slot 16	$t_{d\,TS16}$	80		200	ns	
Output delay 64kHz to 16kHz output	$t_{p\,16}$			70	ns	Fig.7
Output delay, 64kHz to 8kHz output	$t_{p\,8}$			170	ns	Fig.7
Output delay, 64kHz to binary data output (64kHz)	$t_{p\,BIN}$	20		450	ns	Fig.8
Output delay 64kHz to AMI, $\overline{AMI}$, AMI data & $\overline{AMI}$ data o/p's	$t_{p\,AMI}$	20		400	ns	Fig.8
Input delay, 64kHz to binary data in (64kHz)	$t_{d\,BIN}$			100	ns	

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. 8kHz
8kHz square wave output.

2. 16kHz
16kHz square wave output.

3. Clock
System clock input (2.048MHz for a 2Mbit PCM system)

4. Alarm inhibit
A high level on this input inhibits the 8kHz timing signal on the AMI clock outputs.

5. AMI output
Alternative Mark Inversion coded 64kHz.

6. $\overline{AMI}$ output

7. $\overline{AMI}$ Data in/out
In the transmit mode 64kHz signalling data in AMI format is accepted at these inputs for output to PCM highway during time slot 16.

8. GND
Zero volts.

9. AMI Data in/out
In the receive mode data accepted from the PCM highway during time slot 16 appears on these outputs at 64kbits/sec in AMI format.

10. 64kHz
64kHz square wave output.

11. Binary data in/out
In the transmit mode 64k bit/sec signalling data in binary form is accepted at this input for output to the PCM data highway during time slot 16. In the receive mode data is accepted from the PCM highway during TS16 and appears at this output at 64k bits/sec in binary format.

12. Digital Highway access in/out
In the receive mode 2Mbit/sec signalling data is accepted at this input during time slot 16 from the PCM digital highway. In the transmit mode signalling data is output to the PCM digital highway during time slot 16 at 2Mbits/sec.

13. Mode control
A high level on this input causes the MJ1446 to operate in the transmit mode while a low level causes it to operate in the receive mode.

14. TS16
This input should be connected to time slot 16 channel pulse of the PCM system to synchronise the MJ1446 with the rest of the system.

15. Alarm output
A high level on this output indicates that the internal counter has stopped or is out of synchronisation with the time slot 16 channel pulse.

16 V_{CC}
Positive supply 5V ±5%.

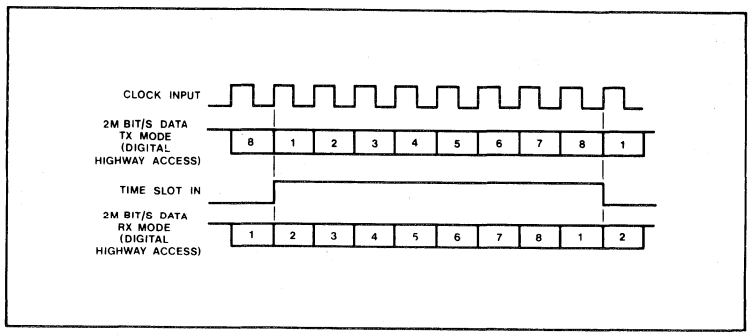


Fig.3 2MBit/s operation

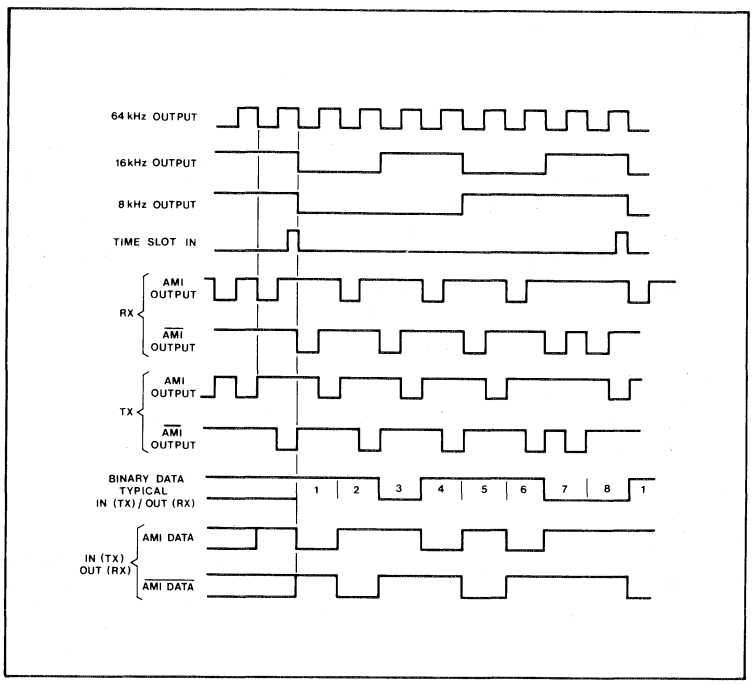


Fig.4 64kBit/s operation

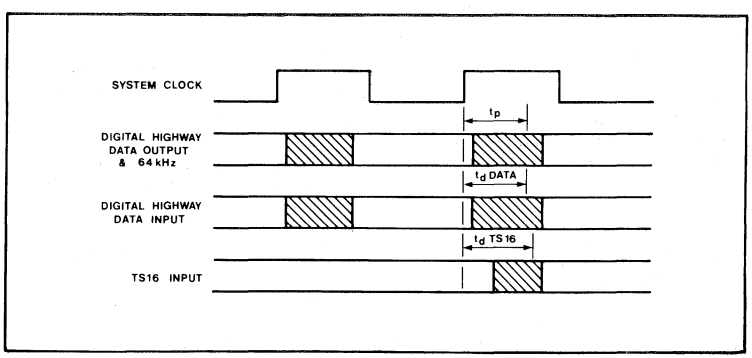


Fig.5 Timing diagram

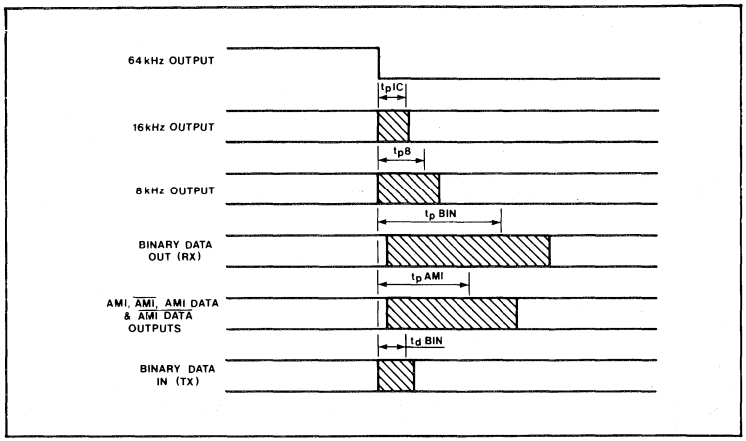


Fig.6 Timing diagram

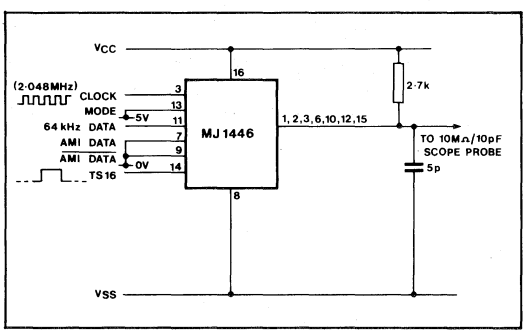


Fig.7 Test conditions (transmit mode)

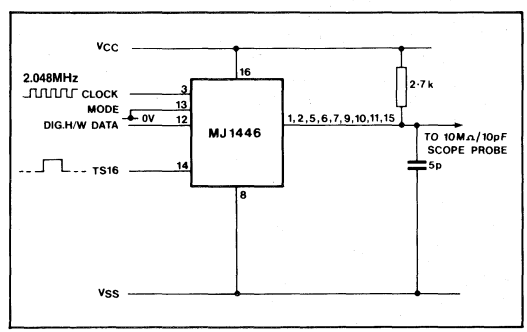


Fig.8 Test conditions (receive mode)

MV1442

HDB3 ENCODER/DECODER/CLOCK REGENERATOR

The GPS 2Mbit PCM signalling series comprises a group of circuits which will perform the common channel signalling and error detection functions for a 2.048Mbit PCM transmission link operating in accordance with the appropriate CCITT recommendations. The circuits are fabricated in CMOS and operate from a single +5V supply with all inputs and outputs being TTL compatible.

The MV1442 is an encoder/decoder for the HDB3 pseudo-ternary transmission code, described in Annex A of CCITT Recommendation G.703. The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of the HDB3 coding, all ones detection and loss of input (all zeros detection). In addition a loop back function is provided for terminal testing. The MV1442 may be selected to function in either internal or external clock recovery modes. Internal clock recovery mode may be selected for either 1.544MHz or 2.048MHz operation and in this mode an external 16.384MHz crystal (12.352MHz for 1.544MHz operation) is required. External clock recovery mode may be selected for 1.544MHz, 2.048MHz or 8.448MHz operation.

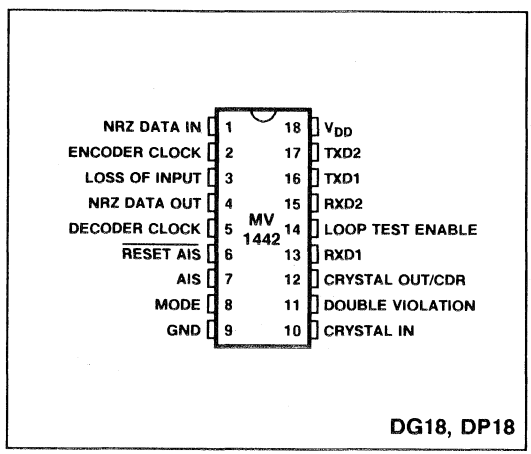


Fig.1 Pin connections - top view.

FEATURES

- On-chip Digital Clock Regenerator.
- HDB3 Encoding and Decoding to CCITT Recommendation G.703.
- Asynchronous operation.
- Simultaneous Encoding and Decoding.
- Clock recovery signal allows Off-chip Clock Regeneration.
- Loop Back Control.
- HDB3 Error Monitor.
- 'All Ones' Error Monitor.
- Loss of Input Alarm.
- Low Power Operation.
- 2.048MHz or 1.544MHz Operation in External or Internal Clock Recovery modes.
- 8.448MHz Operation in External Clock Recovery mode.

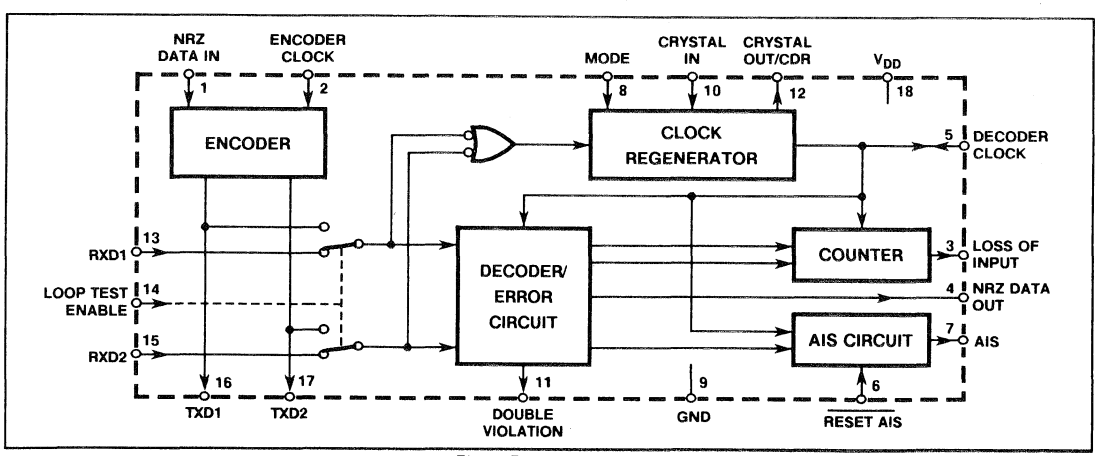


Fig.2 Block diagram.

FUNCTIONAL DESCRIPTION

High Density Bipolar 3 (HDB3) is a pseudo-ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to allow adequate clock recovery at the receiver. In any sequence of four consecutive binary zeros, the last zero is substituted by a mark of the same polarity as the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code, and ensures that successive violations alternate in polarity and as such introduce no DC component to the HDB3 signal.

The MV1442 consists of three main blocks, the HDB3 Encoder, the HDB3 Decoder and the Clock Regenerator. The function of each block is described separately below.

HDB3 ENCODER

The HDB3 Encoder is responsible for converting the incoming NRZ data into pseudo-ternary form for transmission over a PCM link. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703. The data to be encoded is input on the NRZ DATA IN pin and the encoding process is synchronised to the clock signal being input on the ENCODER CLOCK pin. The two TXD outputs, TXD1 and TXD2, represent the HDB3 data in pseudo ternary form. If a mark is to be transmitted the output goes high after the rising edge of clock. The length of the pulse is set by the positive clock pulse width. The timing diagram of the HDB3 Encoder is shown in Fig. 3.

HDB3 DECODER

The HDB3 Decoder is responsible for decoding the HDB3 pseudo-ternary data on its inputs, RXD1 and RXD2, into NRZ form to be output on the NRZ DATA OUT pin. In addition to this the decoder circuit provides three alarm outputs. The first of these alarms is DOUBLE VIOLATION. As its name suggests, a logic high on this output denotes that two successive violations have been received with the same polarity, thus violating the HDB3 coding laws. The second alarm, LOSS OF INPUT, is used to denote that 11 consecutive zeros have been received on the RXD inputs. The final alarm output is AIS (All ones). This alarm goes high if less than 3 decoded zeros have been detected in the preceding $\overline{\text{RESET AIS}} = 1$ period (i.e. between $\overline{\text{RESET AIS}} = 0$ pulses) and as such this alarm can be used as an 'all ones' detector. The decoding process and all the alarm circuitry is synchronised to the clock signal being input to this block on the DECODER CLOCK pin. This clock signal may be asynchronous with the ENCODER CLOCK signal. The timing diagrams of the HDB3 Decoder and alarm circuitry are shown in Figs. 4 to 7.

In addition to the normal mode of operation, a loop test mode is available for terminal testing. This mode is selected by taking the LOOP TEST ENABLE input high. In this mode, the HDB3 encoded pseudo-ternary data outputs of the Encoder block are fed back as the inputs to the Decoder block, which in turn decodes this data and outputs it in NRZ form.

CLOCK REGENERATOR

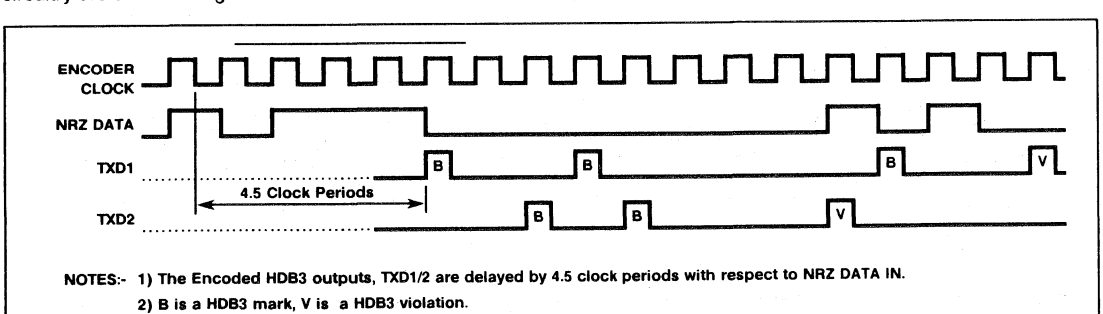
The Clock Regenerator block has two possible modes of operation. With the MODE pin high, internal crystal controlled clock regeneration is selected whilst with the MODE pin low, external clock regeneration is selected, using, for example, a tuned circuit.

In external clock regeneration mode, a logically OR'ed version of the HDB3 data, from the RXD inputs, is output to the external clock regeneration circuitry on the CRYSTAL OUT/CDR pin. The regenerated clock is then fed back into the MV1442 on the DECODER CLOCK pin. External clock regeneration may be used for operation with data rates of 1.544Mbit/s, 2.048Mbit/s or 8.448Mbit/s.

In internal clock regeneration mode, the logically OR'ed data is input to a digital clock regenerator, which constantly resynchronises a divide-by-8 counter to the incoming data stream. The clock thus regenerated is output to the decoder circuitry and to any external circuitry on the DECODER CLOCK pin. A crystal of frequency 8 times the required data rate must be connected between the CRYSTAL IN and CRYSTAL OUT/CDR pins. Thus the crystal frequency needs to be 16.384MHz or 12.352MHz for data rates of 2.048Mbit/s or 1.544Mbit/s respectively. Internal clock regeneration may not be used for operation at a data rate of 8.448Mbit/s.

The MV1442 is capable of withstanding up to 0.25UI of peak to peak input jitter at a jitter frequency of 2.048MHz without introducing errors into the decoded data. At lower jitter frequencies, the MV1442 is capable of withstanding much larger values of peak to peak input jitter. In the absence of input jitter, the MV1442 will produce an output jitter waveform in the form of a sawtooth ramping between 0UI and 0.125UI. The period of this waveform will be dependent upon the difference in frequencies between the remote transmitters clock and the crystal controlled clock of the MV1442.

The MV1442 was originally designed as a pin compatible replacement for the MV1441 with a much improved internal clock recovery circuit and allowing operation at 8.448MHz with external clock recovery selected. However, there are certain minor differences between the two circuits which are described in a separate Applications Brief.



NOTES:- 1) The Encoded HDB3 outputs, TXD1/2 are delayed by 4.5 clock periods with respect to NRZ DATA IN.
2) B is a HDB3 mark, V is a HDB3 violation.

Fig. 3: Encoder waveforms.

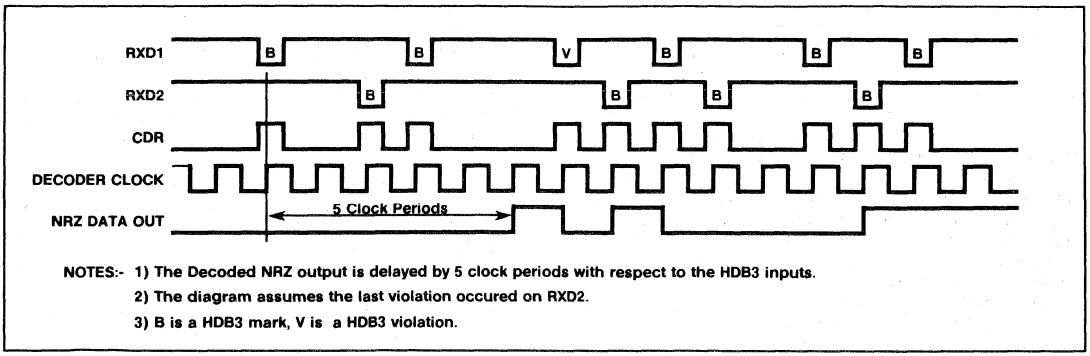


Fig. 4 Decoder waveforms.

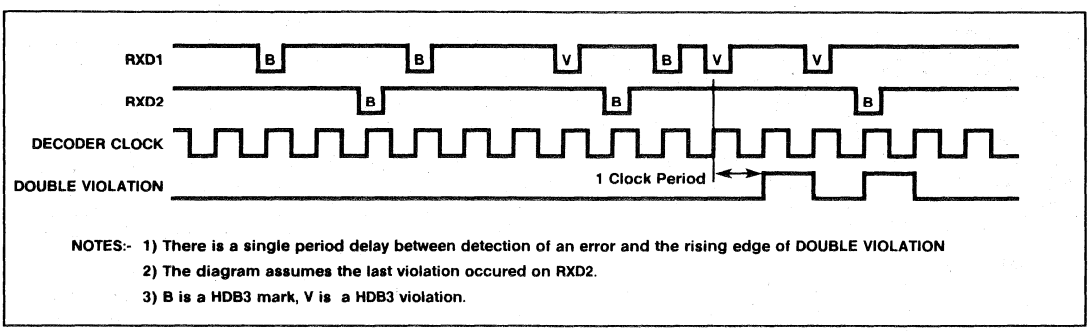


Fig. 5 HDB3 Double violation waveforms.

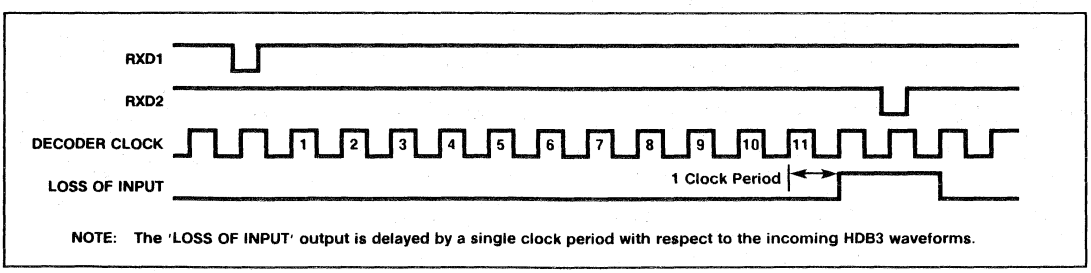


Fig. 6 Loss of input waveforms.

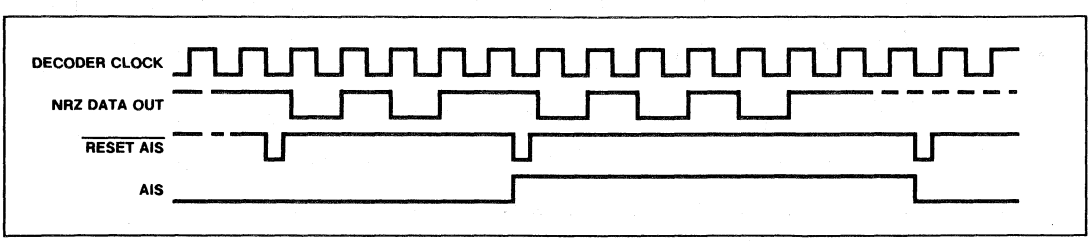


Fig. 7 AIS and $\overline{\text{RESET AIS}}$ waveforms.

PIN DESCRIPTIONS

Pin number	Pin name	Pin descriptions
1	NRZ DATA IN	Input pin for data to be encoded into pseudo-ternary HDB3 form. This data is clocked into the Encoder block by the falling edge of ENCODER CLOCK.
2	ENCODER CLOCK	Clock input for the encoding of data on pin 1.
3	LOSS OF INPUT	Output from the loss of input circuit. This output goes high one clock period after the detection of eleven consecutive zeros on the decoder inputs. Any logic '1' at the input (RXD1 or RXD2 = 0) resets this count after a single clock period delay.
4	NRZ DATA OUT	NRZ data output obtained from the decoding of the pseudo-ternary inputs to the Decoder block.
5	DECODER CLOCK	Clock input to the Decoder block, for decoding data on RXD1 and RXD2, or TXD1 and TXD2 in loop test mode. In internal clock regeneration mode, this pin is used to output the regenerated clock to external circuitry. In external clock regeneration mode, this pin is used to input the externally regenerated clock signal direct to the Decoder block.
6	$\overline{\text{RESET AIS}}$	Reset input to the decoded zero counter. A logic '0' on this input resets a decoded zero counter. It will also reset the AIS output to '0' provided 3 or more zeros have been decoded in the preceding $\overline{\text{RESET AIS}}$ = 1 period, or set AIS to '1' if less than 3 zeros have been decoded in the preceding $\overline{\text{RESET AIS}}$ = 1 period. This may be used to indicate loss of timeslot zero. A logic '1' on this pin enables the decoded zero counter.
7	AIS	Output from AIS circuit (see description for pin 6).
8	MODE	Input pin for selection of clock regeneration mode. A logic '1' on this input selects internal crystal controlled clock regeneration whilst a logic '0' selects external clock regeneration.
9	GND	Digital ground. 0V.
10	CRYSTAL IN	Input to crystal oscillator amplifier when in internal clock regeneration mode, with the crystal connected between pins 10 and 12. Alternatively, this pin may be used as the 16.384/12.352 MHz input to the internal clock regeneration circuitry if one oscillator is shared between several decoders. This pin has no function when external clock regeneration is selected and should be tied to GND.
11	DOUBLE VIOLATION	Output from the error detector circuit. This output goes high for one period of Decoder clock, one period after the detection of a HDB3 violation of the same polarity as the previous HDB3 violation.
12	CRYSTAL OUT/CDR	In external clock regeneration mode, this pin is used to output the OR function of the two HDB3 inputs, RXD1 and RXD2 (or TXD1 and TXD2 if loop test mode is selected), to an external clock regeneration circuit. In internal clock regeneration mode, this is the output which forms the crystal oscillator with pin 10.
13	RXD1	HDB3 input 1 to Decoder block. This input asynchronously latches the incoming HBD3 encoded data and is falling edge sensitive.
14	LOOP TEST ENABLE	Input pin for selection of normal or loop back operation. A logic low on this pin selects normal operation, with encode and decode being independent and asynchronous. A logic high on this pin internally connects TXD1 to RXD1 and TXD2 to RXD2. Note that in loop back mode, a decoder clock must be supplied (or regenerated from pin 12) along with the encoder clock.
15	RXD2	HDB3 input 2 to Decoder block. See pin 13 description.
16	TXD1	HDB3 Encoded output 1 from Encoder block. This output goes high after the rising edge of clock if a mark is to be transmitted. The length of the pulse is set by the positive clock pulse width.
17	TXD2	HDB3 Encoded output 2. See pin 16 description.
18	V_{DD}	Digital supply voltage. 5V ± 10%.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{DD} = 5V ± 0.5V Ambient Temperature T_{amb} = 0°C to + 70°C.

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0		0.8	V	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	V	
Low Level Output Voltage	V_{OL}			0.4	V	I_{SINK} = 2mA
High Level Output Voltage	V_{OHT}	2.4			V	I_{SOURCE} = 2mA
	V_{OHC}	V_{DD}-1.0			V	I_{SOURCE} = 1mA
Input Leakage Current	I_{IN}	-10		+ 200	µA	V_{IN} = V_{DD} or GND.
Supply Current	I_S			15	mA	1.544/2.048MHz Operation with Internal clock regeneration, Note 1.
				5	mA	1.544/2.048MHz Operation with External clock regeneration, Note 1.
				15	mA	8.448MHz Operation, Note 1.
Input Capacitance	C_{IN}		5		pF	All Inputs.
Output Capacitance	C_{OUT}		5		pF	All Outputs.

NOTES
1. All supply currents measured with outputs unloaded.

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Clock Period	t_{CP}	100			ns	Refer Fig. 8.
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	Refer Fig. 8.
Clock High/Low Time	t_{CH}/t_{CL}	30			ns	Refer Fig. 8.
Encoder Data Setup Time	t_{EDS}	10			ns	Refer Fig. 9.
Encoder Data Hold Time	t_{EDH}	10			ns	Refer Fig. 9.
TXD1/TXD2 Output Propagation Delay	t_{EPDR}/ t_{EPDF}			40	ns	Note 2, refer Fig. 9.
CDR Propagation Delay	t_{CPDR}/ t_{CPDF}			40	ns	Note 2, refer Fig. 10.
RXD1/2 Data Setup Time	t_{RS}	15			ns	Refer Fig. 10.
RXD1/2 Pulse Width	t_{RW}	10			ns	Refer Fig. 10.
Decoder Output Propagation Delay	t_{OPD}			40	ns	Notes 2 and 3, refer Fig. 10.
$\overline{\text{RESET AIS}}$ Hold-Off Time	t_{RAHO}	10			ns	Refer Fig. 10.
$\overline{\text{RESET AIS}}$ Pulse Width	t_{RAW}	10			ns	Refer Fig. 10.
$\overline{\text{RESET AIS}}$ Setup Time	t_{RAS}	10			ns	Refer Fig. 10.
AIS Output Propagation Delay	t_{APD}			40	ns	Note 2, refer Fig. 10.

NOTES
2. All propagation delays are measured with the relevant output loaded with a 50pF capacitor.
3. t_{OPD} applies to outputs NRZ DATA OUT, LOSS OF INPUT and DOUBLE VIOLATION, but does not apply to AIS.

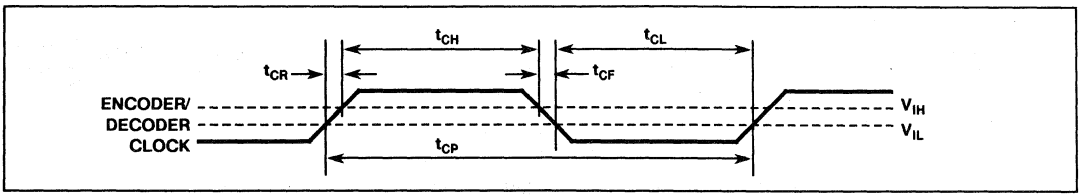


Fig. 8: Clock timing parameters.

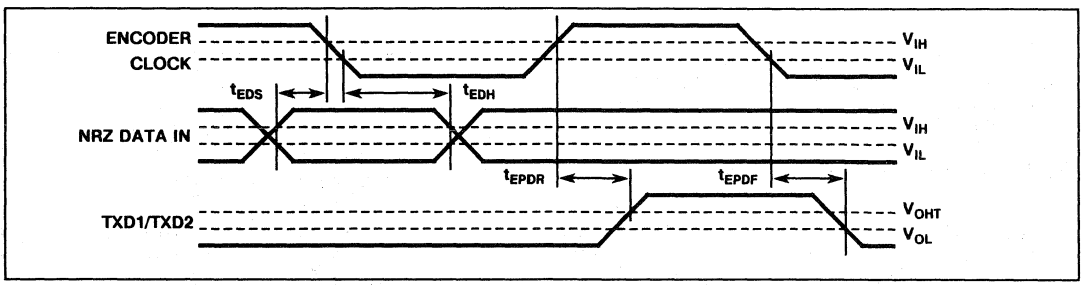


Fig. 9 Encoder timing parameters.

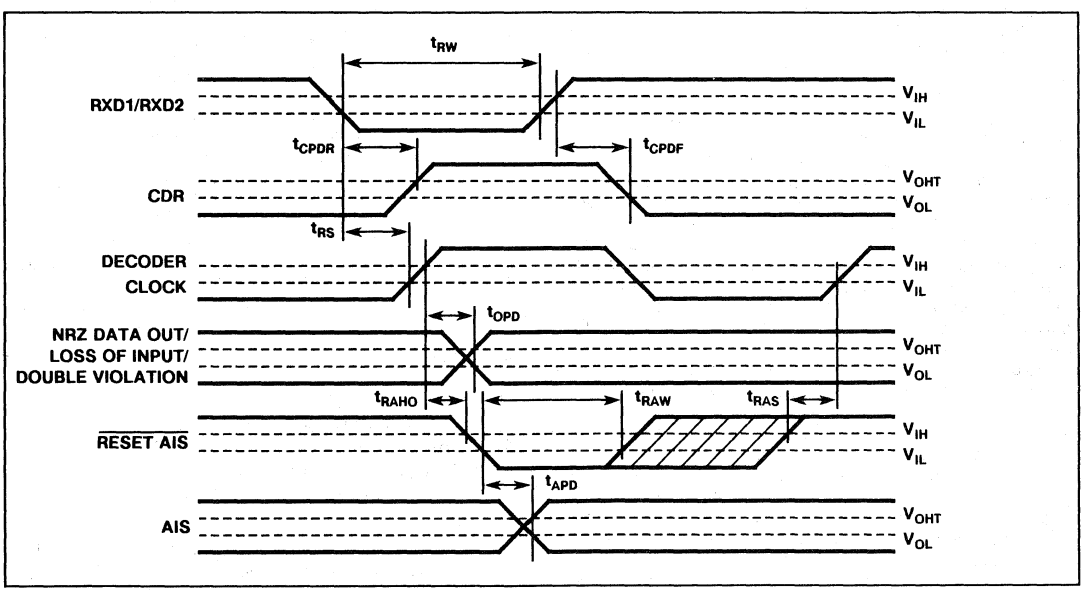


Fig. 10 Decoder timing parameters.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings	
$+V_{DD}$	-0.5 to +7V
Inputs	V_{DD} +0.5V to GND -0.5V
Outputs	V_{DD} +0.5V to GND -0.5V

MV1443

TIMESLOT ZERO TRANSMITTER AND RECEIVER

The MV1443 combines the Timeslot Zero Transmitter and Receiver functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The circuit is fabricated in CMOS and operates from a single +5V supply. All inputs and outputs are TTL compatible.

The transmitter half of the circuit is responsible for generating the timeslot zero synchronising word in accordance with CCITT Recommendation G.704. During alternate frames, denoted sync frames, the CCITT Frame Alignment Signal (FAS - 0011011) is combined with the D1S input and injected on to the PCM highway via the Q-TX output pin. During the other interleaved frames, denoted non-sync frames, bit 2 is set to '1' to avoid imitation of the FAS and this is combined with the D1N input for bit 1 and the D3N-D8N user data inputs for bits 3-8, and injected on to the PCM highway. The position of Timeslot Zero is specified by the FRS input. This should be a high going pulse, 8 clock periods long, masking timeslot zero of each frame.

The receiver half of the circuit searches for the FAS in the incoming data stream and when this is present achieves frame alignment in accordance with the frame alignment strategy described in CCITT Recommendation G.732. When frame alignment has been achieved various timing outputs are produced which may be utilised by external circuitry. These timing outputs will free run if frame synchronisation is subsequently lost. The RST input may be used to reset the synchronisation process, putting the receiver out of sync.

Two alarm outputs to signal errors in the incoming data stream are provided. The ER output signals that a single corrupted FAS has been received whilst the SA output signals that the receiver has lost frame alignment.

When in sync, the receiver extracts the 6 user data bits of the non-sync frame timeslot zero. These are latched and output on pins Q3N-Q8N for bits 3-8 respectively. In addition, the first bit of timeslot zero is also extracted, under the control of the CRC mode input. When CRC is low, the Q1S and Q1N outputs are extracted from the first bit of all sync and non-sync frames respectively. When CRC is high, the Q1S and Q1N outputs are latched from the first bit of frames 13 and 15 of the CCITT CRC multiframe respectively. The position of these frames is determined from the FRS13 and FRS15 inputs.

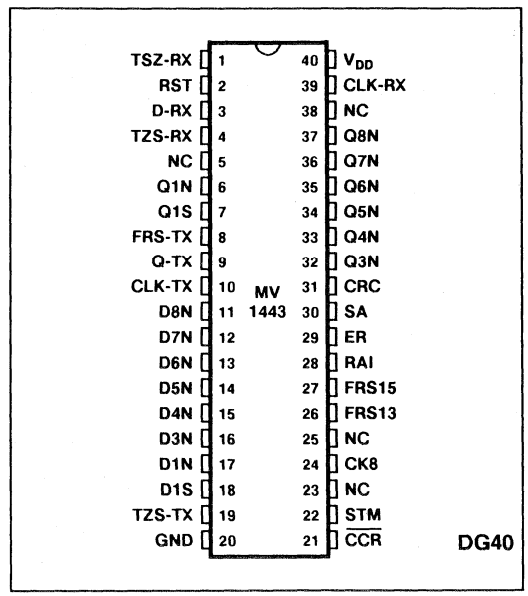


Fig.1 Pin connections - top view.

FEATURES

- Single +5V Supply.
- All Inputs and Outputs TTL compatible.
- Transmitter Generates FAS in Accordance with CCITT Recommendation G.704.
- Enables Access to User Data Bits of Timeslot
- Zero.
- Receiver Frame Synchronisation carried out in accordance with CCITT Recommendation G.732.
- Provides Alarm Outputs for Reception of Corrupted Alignment word and loss of Frame Alignment.
- Extracts the International spare bits (Q1S and Q1N) from Alternate Frames or from Frames 13 and 15 of the CCITT CRC multiframe.

MV1444

COMBINED TIMESLOT ZERO TRANSMITTER AND HDB3 ENCODER

The MV1444 combines the Timeslot Zero Transmitter and HDB3 Encoder functions required by a 2.048Mbit PCM transmitter operating in accordance with the appropriate CCITT Recommendations. The circuit is fabricated in CMOS and operates from a single +5V supply. All inputs and outputs are TTL compatible.

The Timeslot Zero Transmitter half of the circuit is responsible for generating the timeslot zero synchronising word in accordance with CCITT Recommendation G.704. During alternate frames, denoted sync frames, the CCITT Frame Alignment Signal (FAS - 0011011) is combined with the D1S input and output on to the PCM highway. During the other interleaved frames, denoted non-sync frames, bit 2 is set to '1' to avoid imitation of the FAS. This is combined with the D1N input for bit 1 and the user data inputs, D3N to D8N, for bits 3 to 8 of timeslot zero.

The data being output from the Timeslot Zero Transmitter is multiplexed together with the other 31 timeslots of data by the transmission multiplexer, and the data stream thus created is fed in to the HDB3 Encoder.

The HDB3 Encoder half of the circuit is responsible for converting the incoming PCM data stream from the transmission multiplexer from NRZ form into pseudo-ternary HDB3 transmission code. This process is carried out in accordance with Annex A to CCITT Recommendation G.703.

FEATURES

- Single +5V Supply.
- All Inputs and Outputs TTL Compatible.
- Timeslot Zero Transmitter Generates FAS in accordance with CCITT Recommendation G.704.
- Enables Access to 6 National Data Bits and 2 International Data Bits of Timeslot Zero.
- On-Chip Transmission Multiplexer allows combination of Timeslot Zero Data with remaining 31 Timeslots of data.
- HDB3 Encoding to CCITT Recommendation G.703, Annex A.

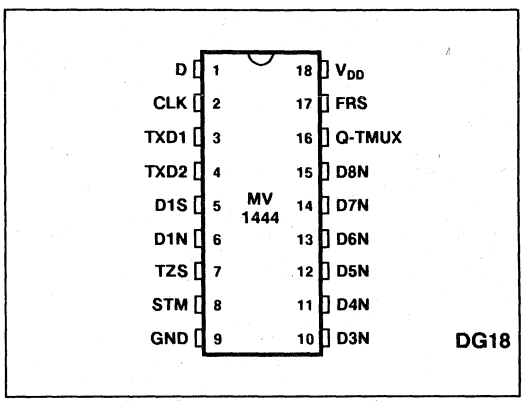


Fig.1 Pin connections - top view.

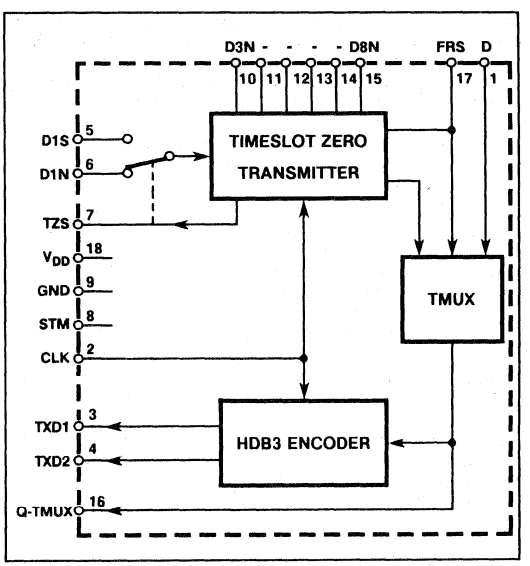


Fig.2 Block diagram.

MV1445

COMBINED HDB3 DECODER AND TIMESLOT ZERO RECEIVER

The MV1445 combines the HDB3 Decoder and Timeslot Zero Receiver functions required by a 2.048Mbit PCM receiver operating in accordance with the appropriate CCITT recommendations. The circuit is fabricated in CMOS and operates from a single +5V supply. All inputs are TTL compatible.

The HDB3 Decoder half of the circuit is responsible for decoding the incoming HDB3 pseudo-ternary data back in to NRZ form. This process is carried out in accordance with Annex A to CCITT Recommendation G.703.

Error monitoring functions are provided to detect violations of the HDB3 coding and loss of input (all zeros detection). In addition, either internal or external clock recovery may be used, with internal clock recovery requiring an external 16.384MHz crystal.

The Timeslot Zero Receiver half of the circuit searches for the Frame Alignment Signal (FAS) in the decoded data stream from the HDB3 decoder. Synchronisation to this pattern is carried in out in accordance with the strategy described in CCITT Recommendation G.732. When synchronisation has been achieved, the receiver produces various timing outputs which will free run if synchronisation is subsequently lost. Two alarms are provided to signal reception of a corrupted FAS and loss of synchronisation.

When in sync, the receiver extracts the 6 user data bits of the non-sync frame timeslot zero. In addition, the International spare bits of timeslot zero are extracted and latched on to the Q1S and Q1N outputs from sync and non-sync frames respectively.

A variant of the MV1445 is available in a 40-pin package with additional features. As well as the double violation and loss of input alarms produced by the HDB3 Decoder, the expanded MV1445 also includes an all ones alarm output. This output will go high if less than three zeros have been detected in the preceding $\overline{\text{RESET AIS}}$ = 1 period.

As previously described, the Timeslot Zero Receiver of the 28 pin part will extract the International spare bits of each frame. The 40-pin part performs this function in one of two ways under control of the CRC mode input. When CRC is low the Q1S and Q1N outputs are extracted from the first bits of sync and non-sync frames respectively, as described above. However, when CRC is high, the outputs are extracted from the first bits of frames 13 and 15 of the CCITT CRC multiframe respectively. The position of these frames is determined by the FRS13 and FRS15 inputs.

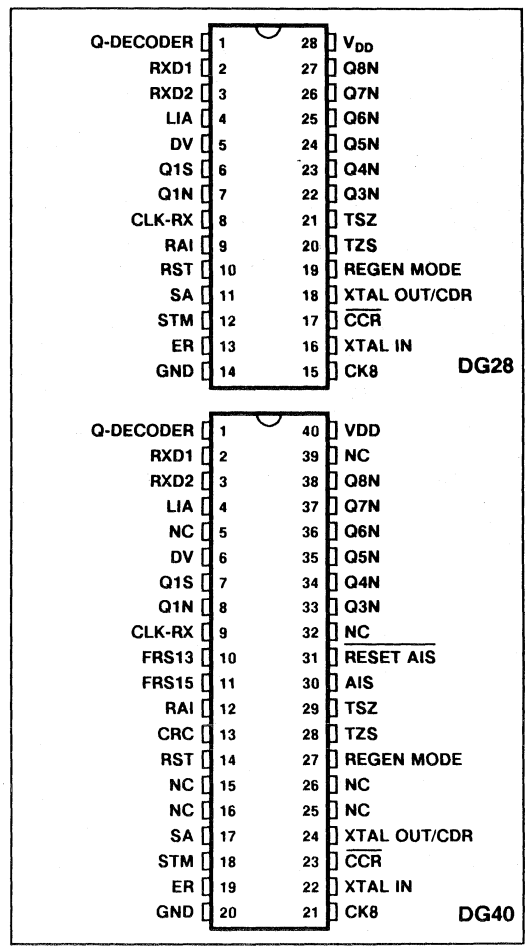


Fig.1: Pin connections - top view.

FEATURES

- Single +5V Supply.
- All Inputs and Outputs TTL Compatible.
- HDB3 Decoding to CCITT Recommendation G.703.
- HDB3 Error Monitor & Loss of Input Alarm.
- On Chip Digital Clock Regenerator.
- Alarms for Corrupted FAS and Loss Of Sync.
- DG40 has 'All Ones' Monitor and CRC Operation.
- Receiver Frame Synchronisation carried out in accordance with CCITT Recommendation G.732.

8.5 MBIT PCM SIGNALLING CIRCUIT
MV1448
HDB3 ENCODER/DECODER

This 8.544MBit PCM Signalling Circuit will perform the signalling and error detection functions for a 8.544MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuit is fabricated in CMOS and operates from a single 5V supply with TTL compatible inputs and outputs.

The MV1448 is an encoder/deocder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol. III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeros detection). In addition a loop back function is provided for terminal testing.

FEATURES

- HDB3 Encoding and Decoding to CCITT rec. G703
- Asynchronous Operation
- Simultaneous Encoding and Decoding
- Clock Recovery Signal Allows Clock Regeneration from Incoming HDB3 Data
- Loop Back Control
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector)
- Decoded Data in NRZ Form
- Low Power Operation
- 2.048MHz or 8.544MHz Operation

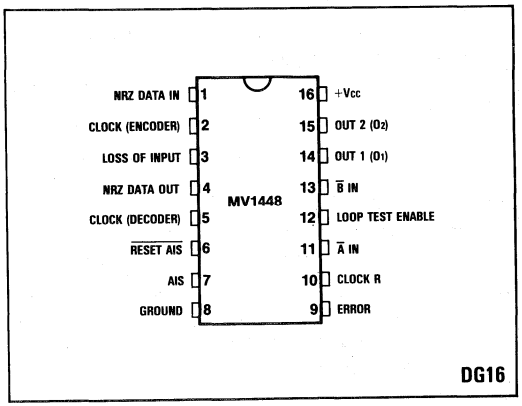


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	-0.5V to +7V
Inputs	Vcc+0.5V to GND -0.3V
Outputs	Vcc to GND -0.3V

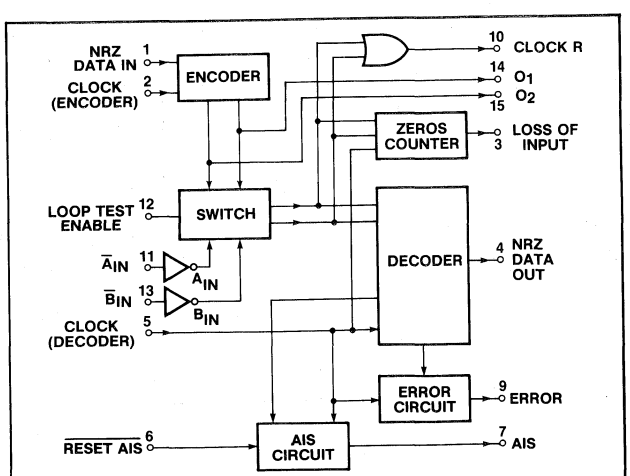


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC} = 5V ± 0.5V Ambient temperature T_{amb} = 0°C to +70°C

Static characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	All inputs	-0.3		0.8	V	
Low level input current	I_{IL}				50	μA	V_{IL} = 0V
High level input voltage	V_{IH}		2.0		V_{CC}	V	
High level input current	I_{IH}				50	μA	V_{IH} = 5V
Low level output voltage	V_{OL}	All outputs			0.4	V	Isink = 2.0mA
High level output voltage	V_{OH}		2.8			V	Isource = 2mA } both
			V_{CC}-0.75			V	Isource = 1mA } apply
Supply current	I_{CC}			2	4	mA	All inputs to 0V All outputs open circuit

Dynamic characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. clock (encoder) frequency	$Fmax_{enc}$	10			MHz	Figs. 10, 15
Max. clock (decoder) frequency	$Fmax_{dec}$	10			MHz	Figs. 11, 15
Propagation delay clock encoder to O_1, O_2	tpd1A/B		50		ns	Figs. 8, 10, 15 See Note 1
Rise and fall times O_1, O_2				20	ns	Figs. 10, 15
tpd1A - tpd1B difference				20	ns	Figs. 10, 15
Propagation delay clock to clock regenerate (clock R)	tpd3		50		ns	Loop test enable = '1', Figs. 10, 15
Setup time of NRZ data in to clock (encoder)	ts3		40		ns	Figs. 7, 10, 15
Hold time of NRZ data in	th3		40		ns	Figs. 7, 10, 15
Propagation delay A_{IN}, B_{IN} to clock regenerate	tpd2 low-high			76	ns	Loop test enable = '0',
	tpd2 high-low			50		Figs. 13, 15
Propagation delay clock (decoder) to error	tpd4			50	ns	Figs. 12, 15
Propagation delay $\overline{\text{Reset AIS}}$ falling edge to AIS output	tpd5		50	44	ns	Loop test enable = '0', Figs. 14, 15
Propagation delay clock (decoder) to NRZ data out	tpd6			50	ns	Figs. 7, 11, 15 See Note 2
Setup time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to clock (decoder)	ts1	15	40		ns	Figs. 7, 11, 15
Hold time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to clock (decoder)	th1	4	5		ns	Figs. 7, 11, 15
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	9			ns	Figs. 7, 14, 15
Setup time clock (decoder) to $\overline{\text{Reset AIS}}$	ts2		50		ns	Figs. 7, 14, 15
Setup time $\overline{\text{Reset AIS}}$ = '1' to clock (decoder)	ts2	31			ns	Figs. 14, 15
Propagation delay clock (decoder) to LIP			50	87	ns	

High Density Bipolar 3 (HDB3) is a pseudo-ternary signal in which the number of consecutive zeros that may occur is restricted to a maximum number of three. In any sequence of four consecutive binary zeros, the ultimate zero is substituted by a 'mark' (+ or -) of the same polarity as the previous mark, i.e. it violates AMI code (Alternate Mark Inversion) and is termed a 'violation'. To ensure parity between marks of opposite polarity, the first zero is substituted by an additional mark when there would otherwise be an even number of marks between 'violations'. Thus violations alternate in polarity.

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. NRZ data in

Input data for encoding into ternary form. The data is clocked by the negative going edge of the Clock (Encoder).

2. Clock (Encoder)

Clock for encoding data on pin 1.

3. LIP

Loss if input circuit detects eleven consecutive zeros at the decoder input and then gives an output high. Any logic '1' at the input (A_{IN} or B_{IN} = '0') resets this count.

4. NRZ data out

Decoded binary data from pseudo-ternary inputs A_{IN} and B_{IN}.

5. Clock (Decoder)

Clock for decoding data on A_{IN} and B_{IN}, or O_1 and O_2 in loop test mode.

6,7. $\overline{\text{Reset AIS}}$, AIS

Logic '0' on Reset AIS resets a decoded zero counter and either resets AIS output to '0' provided 3 or more zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period, or sets AIS to '1' if less than 3 zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period to indicate loss of time slot zero. Logic '1' on $\overline{\text{Reset AIS}}$ enables the internal decoded zero counter.

8. Ground

Zero volts.

9. Error

A logic '1' indicates that a violation of the HDB3 encoding law has been detected i.e. 3 '1's of the same polarity.

10. Clock R

OR function of $\overline{A}_{IN}$, $\overline{B}_{IN}$ for clock regeneration when pin 12 = '0', OR function of O_1, O_2 when pin 12 = '1'.

11,13. $\overline{A}_{IN}$, $\overline{B}_{IN}$

Inputs representing the received ternary PCM signal. $\overline{A}_{IN}$ = '0' represents a positive going '1', $\overline{B}_{IN}$ = '0' represents a negative going '1'. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ are sampled by the positive going edge of the clock decoder. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ may be interchanged.

12. Loop test enable

TTL input to select normal or loop back operation. Pin 14 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 14 = '1' O_1, is connected internally to A_{IN} and O_2 to B_{IN}. Clock R becomes the OR function of O_1, O_2. N.B. A decode clock has to be supplied, or regenerated. The delay from NRZ in (pin 1) to NRZ out (pin 4) is about 6¾ clock periods in loop back.

14,15. O_1, O_2

Outputs representing the ternary encoded PCM HDB3 signal for line transmission. O_1 and O_2 are in Return to zero from and are clocked out on the positive going edge of the encode clock. The length of O_1 and O_2 pulses is set by the positive clock pulse length. Use suitable line drivers from these two outputs such that O_1 gives positive going pulse and O_2 gives negative going pulse.

16. $+V_{CC}$

Positive 5V ± 10% supply.

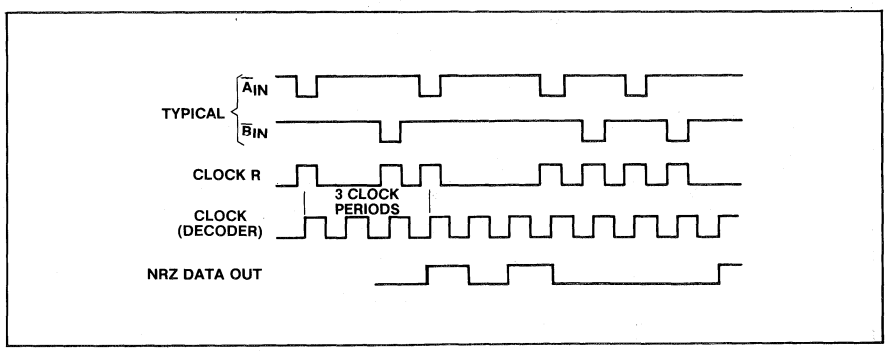


Fig. 3 Decode waveforms

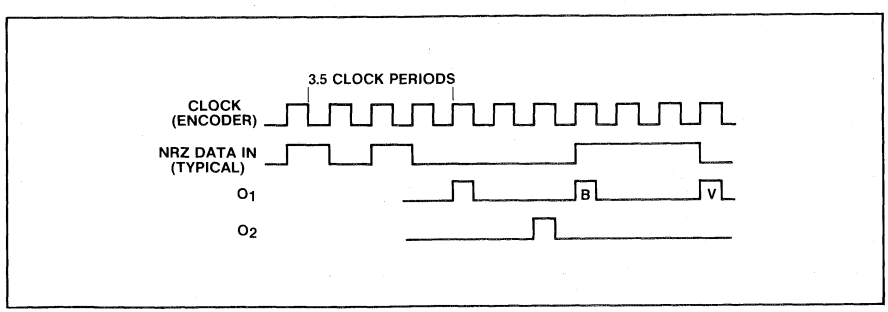


Fig.4 Encode waveforms

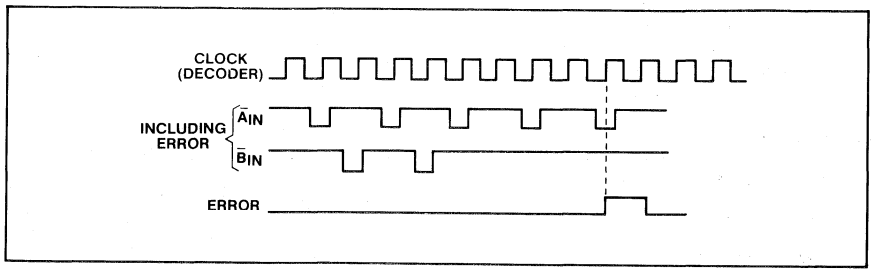


Fig.5 HDB3 error output waveforms

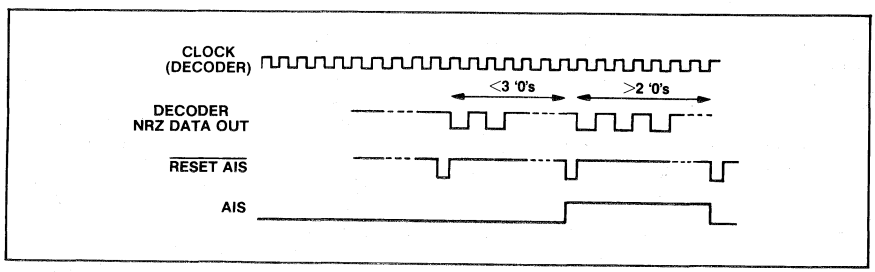


Fig.6 AIS error and Reset waveforms

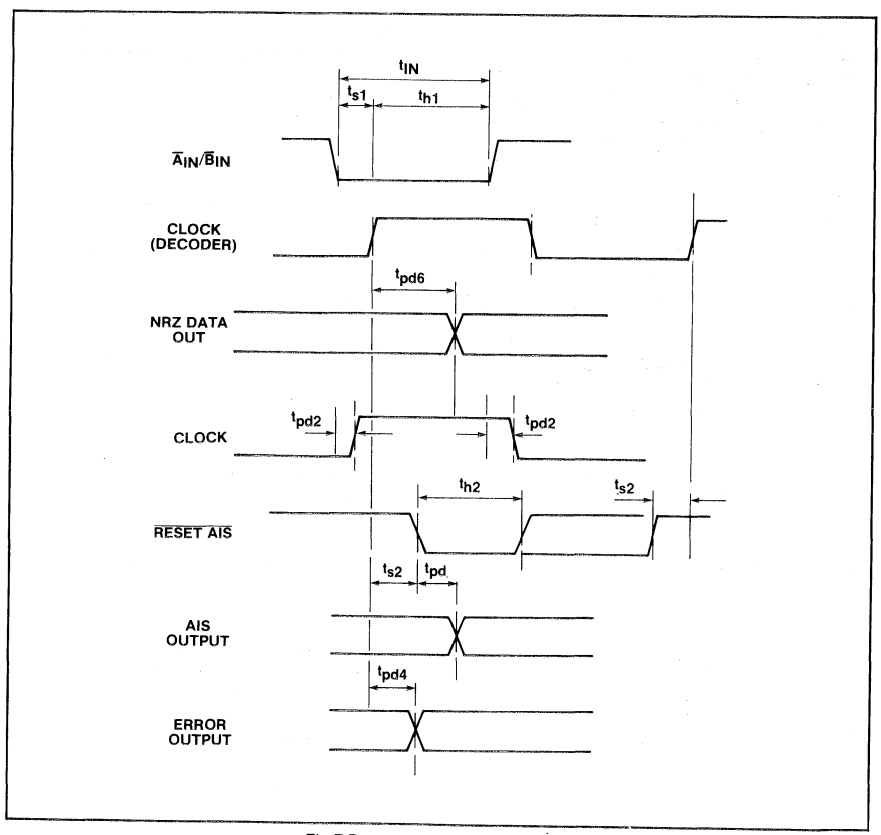


Fig.7 Decoder timing relationship

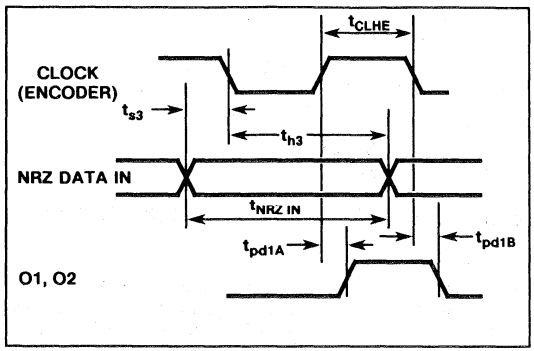


Fig. 8 Encoder timing relationship

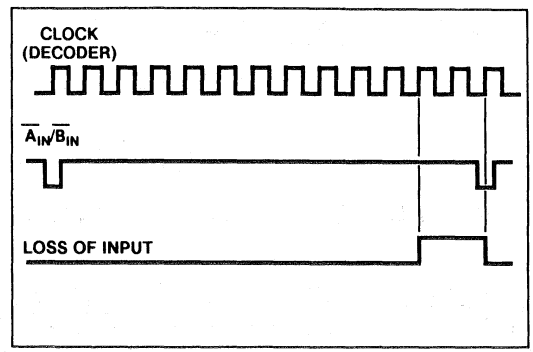


Fig. 9 Loss of input waveforms

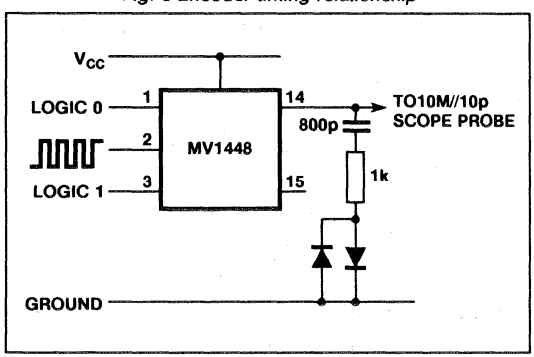


Fig. 10

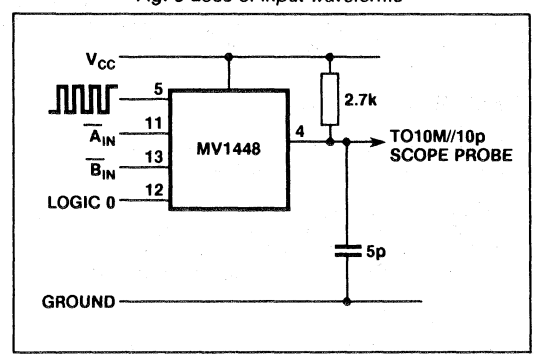


Fig. 11

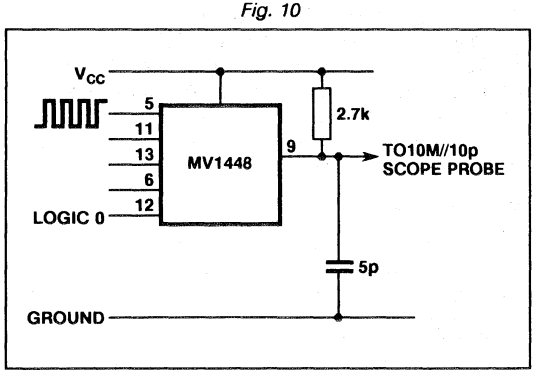


Fig. 12

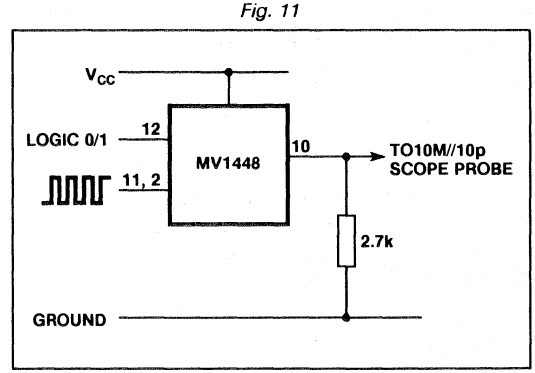


Fig. 13

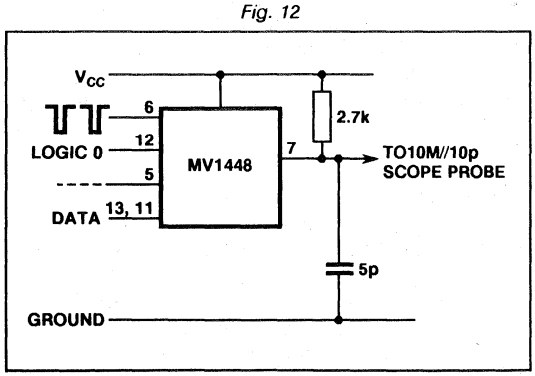


Fig. 14

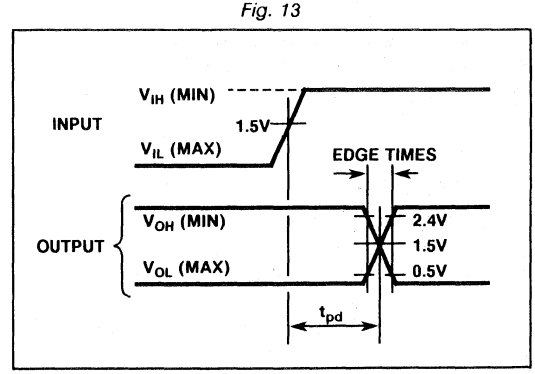


Fig. 15 Test timing definitions

PCM MACROCELLS

2.048MBit PCM-30 MACROCELLS for HDB3, CRC, TS0 & TS16 FUNCTIONS

The following information outlines the functions available from a family of Telecom PCM Macrocells, contained within GEC Plessey Semiconductors' CLA60000 Semi-custom library. These cells have been designed around the most important functions required by a 2.048MBit PCM link operating in accordance with appropriate CCITT Recommendations. It is intended that these macrocells can be used in custom designs using the CLA60000 cell library, in the same manner as for the GPS MV1403 PCM Demonstrator chip. More information on the operation of each macrocell can be found in the descriptions contained in the MV1403 data sheet (page 2-33). For detailed data on each macrocell, reference should be made to the CLA60000 Design Manual.

TRANSMIT FUNCTIONS

The following macrocells provide the stated functionality for the transmit side of a PCM-30 link :-

TXTSZ = Time Slot Zero generator.
TXTS16 = Time Slot 16 data generator.
HDB3EC = High Density Bipolar 3 Encoder.
CRCGEN = Cyclic Redundancy Check data generator.

TXTSZ FEATURES

- Generates Time Slot Zero Sync Pattern.
- Inserts Signalling Data into the Spare Bits of TS0.
- Meets CCITT Recommendation G.704.
- Sync and Non-sync Identification Output.
- Scan Path Testability.

TXTS16 FEATURES

- Receives Signalling Data at 64kHz.
- Transmits Signalling Data at 2.048MHz in TS16.
- Derives TS16 Marker Output.
- Scan Path Testability.

HDB3EC FEATURES

- Inputs Data at 2.048MHz NRZ.
- Transmits Data as Pseudo-Ternary HDB3.
- Meets CCITT Recommendation G.703.
- Input NRZ Data Delayed Output.
- Scan Path Testability.

CRCGEN FEATURES

- Inputs Data at 2.048MHz NRZ.
- Generates 4 Bit CRC Data.
- Generates 6 Bit CRC Multiframe Sync Word with 2 User-Defined Data Bits.
- CRC or Signalling Data Inserted into TS0 Bit 1.
- Meets CCITT Recommendation G.704.
- Scan Path Testability.

RECEIVE FUNCTIONS

The following macrocells provide the stated functionality for the receive side of a PCM-30 link :-

RXTSZ = Time Slot Zero Receiver.
RXTS16 = Time Slot 16 data Receiver.
HDB3DC = High Density Bipolar 3 Decoder.
CRCCHK = Cyclic Redundancy Check data tester.

RXTSZ FEATURES

- Receives 2.048MBit Data Stream.
- Detects Time Slot Zero Sync Pattern.
- Meets CCITT Recommendation G.732.
- Time Slot Zero & Sync Frame Marker Outputs.
- Error, Loss of Sync & Remote Alarm Outputs.
- Extracts Signalling Data from TS0.
- Outputs 4KHz and 8KHz Clocks.
- Scan Path Testability.

RXTS16 FEATURES

- Receives Signalling Data at 2.048MHz in TS16.
- Outputs Signalling Data at 64kHz.
- Scan Path Testability.

HDB3DC FEATURES

- Receives Data as Pseudo-Ternary HDB3.
- Outputs Data at 2.048MHz NRZ.
- Meets CCITT Recommendation G.703.
- Double Violation & Loss Of Input Alarm Outputs.
- Outputs Logical 'OR' of Input Data to Assist Clock Recovery.
- Scan Path Testability.

CRCCHK FEATURES

- Input Data at 2.048MHz NRZ.
- Detects 6 Bit CRC Multiframe Sync Word & Outputs 2 User-Defined Data Bits.
- Compares Generated & Input CRC Check Data.
- Multiframe Sync Alarm & CRC Error Outputs.
- Outputs Frame 13 & Frame 15 Markers.
- Scan Path Testability.

MV1403

PCM MACROCELL DEMONSTRATOR

The MV1403 contains 8 PCM macrocells which can be configured so as to perform the common channel signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link, operating to the appropriate CCITT recommendations. The MV1403 also allows access to all the macrocells individually and is implemented in GPS CMOS technology utilising the CLA60000 series gate array, offering high performance, low power and fast turn-round. The following macrocells are included in the MV1403.

Timeslot Zero Transmitter - **TXTSZ**
Timeslot Sixteen Transmitter - **TXTS16**
Cyclic Redundancy Check Generator - **CRCGEN**
High Density Bipolar (HDB) 3 Encoder - **HDB3EC**
Timeslot Zero Receiver - **RXTSZ**
Timeslot Sixteen Receiver - **RXTS16**
Cyclic Redundancy Checker - **CRCCHK**
High Density Bipolar (HDB) 3 Decoder - **HDB3DC**

With the MV1403 set up to combine the internal macrocells, two demonstration modes are available, referred to as Transmit and Receive demonstration modes.

In Transmit demonstration mode, timeslot zero sync word (including user data bits and optional CRC check bits), timeslot sixteen data and 30 voice channels are combined and transmitted as pseudo-ternary HDB3 encoded outputs. The Transmit demonstration mode can also be set to generate CRC multiframe data in accordance with CCITT Recommendation G. 704.

In Receive demonstration mode, the pseudo-ternary HDB3 inputs are decoded back to NRZ form and frame synchronisation is achieved by detection of the Frame Alignment signal in the incoming data stream. This permits extraction of user data bits, timeslot sixteen data and voice channel data. An optional CRC mode generates CRC multiframe alignment and a cyclic redundancy check is carried out on the incoming data. In addition receive demonstration mode generates appropriate alarms for loss of input, double violation on the HDB3 inputs, loss of frame or CRC multiframe alignment, detection of erroneous frame alignment word, remote alarm received from the transmitter, and detection of a CRC error in either sub-multiframe 1 or 2.

FEATURES

- Single +5V Supply
- All Inputs and Outputs TTL Compatible
- Selectable as PCM Transmitter or Receiver
- Allows Access to all 8 Macrocells Individually
- HDB3 Encoding and Decoding to CCITT Recommendation G. 703
- Transmitted Frame Structure to CCITT Recommendation G. 704
- Receiver Frame Synchronisation to CCITT Recommendation G. 732
- Selectable CRC Mode
- CRC Generation and Checking to CCITT Recommendation G. 704

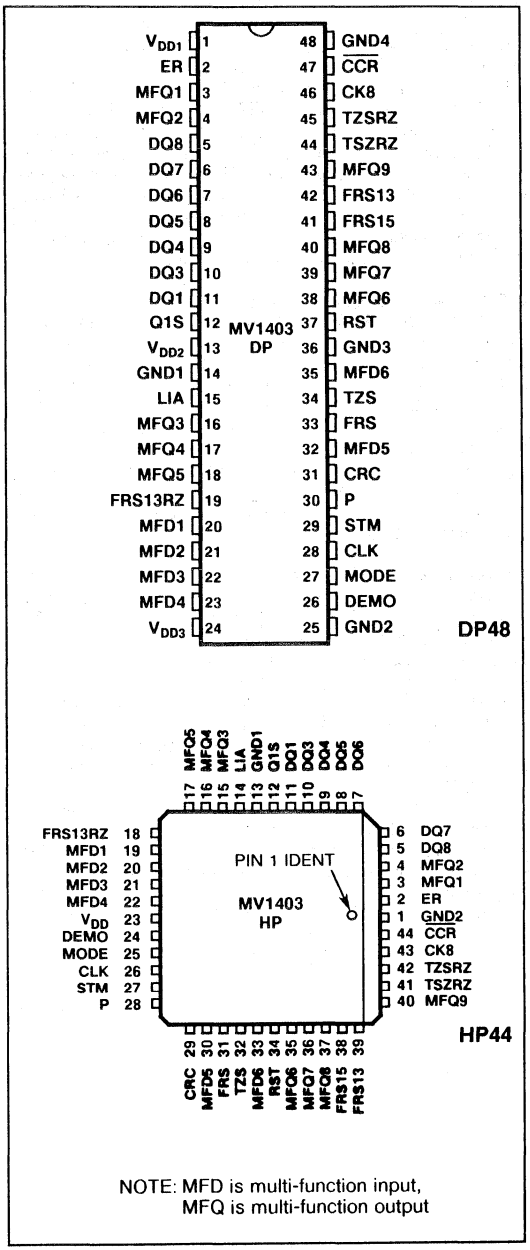


Fig.1 Pin connections - top view

FUNCTIONAL DESCRIPTION

The MV1403 PCM macrocell demonstrator contains a family of 4 Transmit PCM and 4 Receive PCM macrocells which may be configured to function individually, or be connected together to form demonstrations of their operation. In order to keep the pin count to a minimum, some of the input and output pins are shared. Pin functions thus depend upon whether the device is configured as a transmitter or receiver. The operational modes of the MV1403 are selected under control of the MODE and DEMO pins, as shown in Table 1. Note that the MODE pin selects either the transmit or receive set of macrocells and that the DEMO pins selects either individual or combined connections.

In addition the operation of the MV1403 is controlled by a further two control inputs, STM and CRC. The STM pin is used for device testing and should be tied low for normal operation. The CRC control pin selects whether or not the device performs the CRC generation/checking procedure. A logic 'High' on this pin puts the device in Cyclic Redundancy Generate/Check mode.

More detailed information about all 8 macrocells can be found in the individual macrocell publications.

INDIVIDUAL TRANSMIT MODE, TX1

In this mode (MODE = 0, DEMO = 0) the four transmitter macrocells (TXTSZ, TXTS16, CRCGEN and HDB3EC) are all accessed individually. The functional diagram of the MV1403 in this mode is shown in Fig. 2. All four macrocells are synchronised to a common 2.048MHz clock, and the TXTSZ, TXTS16 and CRCGEN macrocells are also synchronised to a second timing input, FRS (Frame Sync). This is an 8 clock period high going pulse at 8kHz which masks timeslot zero to enable frame alignment. The function of each transmit macrocell is now described separately.

Timeslot Zero Transmitter

The Timeslot Zero Transmitter macrocell generates a Frame Alignment Signal (FAS) in accordance with CCITT Recommendation G. 704. This is combined with the international spare bit (the D1 input) and output on Q during timeslot zero of alternate frames, denoted sync frames. During the other interleaved frames, denoted non-sync frames, bit 2 is fixed at logic 1 to avoid imitation of the FAS. This bit is slotted together with the international spare bit (D1 input) and 6 user data bits (the D3N-D8N inputs) for output on Q.

A TZS output (Timeslot Zero Sync frame) is provided to denote whether a sync frame or non-sync frame is being output. It changes state one clock period after the end of timeslot zero and is high during timeslot zero of sync frames.

Fig. 3 shows the timing diagram for this macrocell.

Timeslot Sixteen Transmitter

This macrocell takes in a continuous 64kbit data stream (D input) and outputs it in 8 bit packets at a bit rate of 2.048 Mbit during timeslot 16 of successive frames on its Q output. The position of timeslot 16 is determined from the FRS timing input, which masks timeslot zero. The TS16 output is an 8 clock period high going pulse at 8kHz, similar to FRS, but high during the 8 bits of timeslot sixteen.

Fig. 4 shows the timing diagram for this macrocell.

Cyclic Redundancy Check Generator

This macrocell has two modes of operation, selected by its EN control input. When EN is 'high', CRC generation mode is selected. However, both modes are concerned with producing the data bit to be inserted into the international spare bit of timeslot zero (CCITT G. 704 structure). In non-CRC mode, this data is selected to be either the D1S (sync frames) or D1N (non-sync frames) input depending upon whether a sync or non-sync frame is about to be transmitted (determined by the TZS input).

With CRC mode enabled, the macrocell generates CRC words and outputs this data during the international spare bit of sync frames. During non-sync frames, the 6 bit CRC Multiframe Alignment Signal is output along with the two user data inputs, D1S and D1N. This procedure is carried out in accordance with CCITT Recommendation G. 704. The CRC word is generated from the incoming data stream on the D input pin. CCITT Recommendation G. 704 defines the 16 frame CRC multiframe structure, not related to the possible use of a 16 frame multiframe structure in timeslot 16. Each 16 frame CRC multiframe is divided into two 8 frame sub-multiframes, denoted sub-multiframes 1 and 2 (SMF1 and SMF2). The CRC procedure is carried out on each sub-multiframe of data and the resulting 4 bit CRC word is output during the international spare bit of sync frames during the following sub-multiframe. All data is output on the Q output pin. Table 2 displays the CRC multiframe structure in more detail.

High Density Bipolar (HDB3)Encoder

The HDB3 Encoder macrocell converts the incoming NRZ data on its D input pin into HDB3 pseudo-ternary form for transmission over a 2.048 Mbit PCM link in accordance with CCITT Recommendation G.703. The two TXD outputs represent the HDB3 data in pseudo-ternary form. They are always low during the high half cycle of CLK, but may be high or low during the low half cycle. The Q output represents the D input but delayed by one period. Fig. 5 shows the timing diagram of this macrocell.

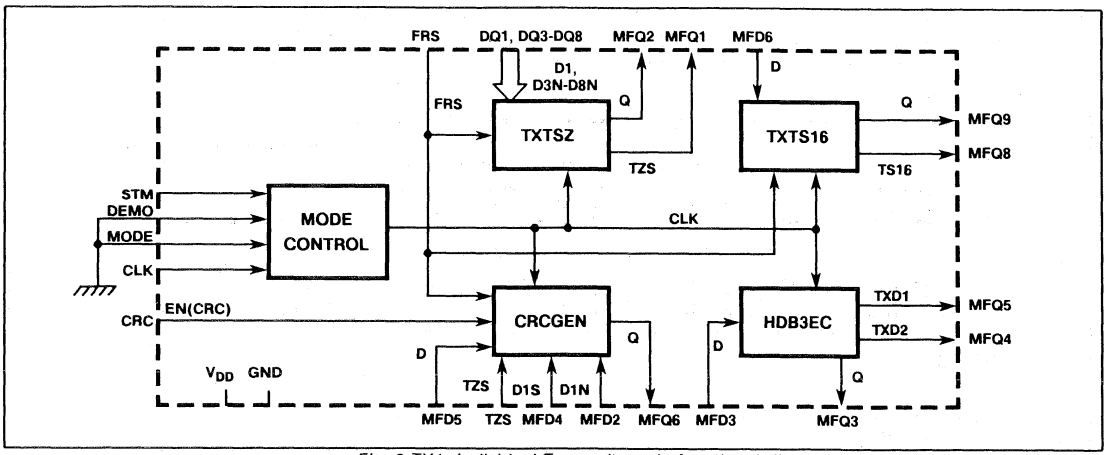


Fig. 2 TX1 Individual Transmit mode functional diagram

Mode name	MODE input	DEMO input	CRC input	STM input	Mode description
TX1	0	0	0/1	0	MV1403 is configured as individual Transmit PCM macrocells.
TX2	0	1	0/1	0	MV1403 is configured as a PCM Transmitter demonstration, using the Transmit macrocells.
RX1	1	0	0/1	0	MV1403 is configured as individual Receive PCM macrocells.
RX2	1	1	0/1	0	MV1403 is configured as a PCM Receiver demonstration, using the Receive macrocells.
TX1/2	0	0/1	0	0	CRC generation mode of the CRCGEN macrocell is disabled.
TX1/2	0	0/1	1	0	CRC generation mode of the CRCGEN macrocell is enabled.
RX1/2	1	0/1	0	0	CRC mode of the RXTSZ macrocell is disabled.
RX1/2	1	0/1	1	0	CRC mode of the RXTSZ macrocell is enabled.
–	X	X	X	1	MV1403 is configured in device test mode. This mode should not be used for normal operation.

Table 1 Operational modes of the MV1403

	CRC Multiframe															
	Sub-Multiframe 1 (SMF1)								Sub-Multiframe 2 (SMF2)							
Frame number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit one of timeslot zero	C1	0	C2	0	C3	1	C4	0	C1	1	C2	1	C3	D1S	C4	D1N

NOTES
1. CI, C2, C3, C4 are the 4 bits of the CRC word.
2. 001011 is the CRC Multiframe Alignment Signal (MAS).
3. Even numbered frames are denoted Sync frames; odd numbered frames are denoted non-sync frames.

Table 2 Structure of the CCITT CRC Multiframe

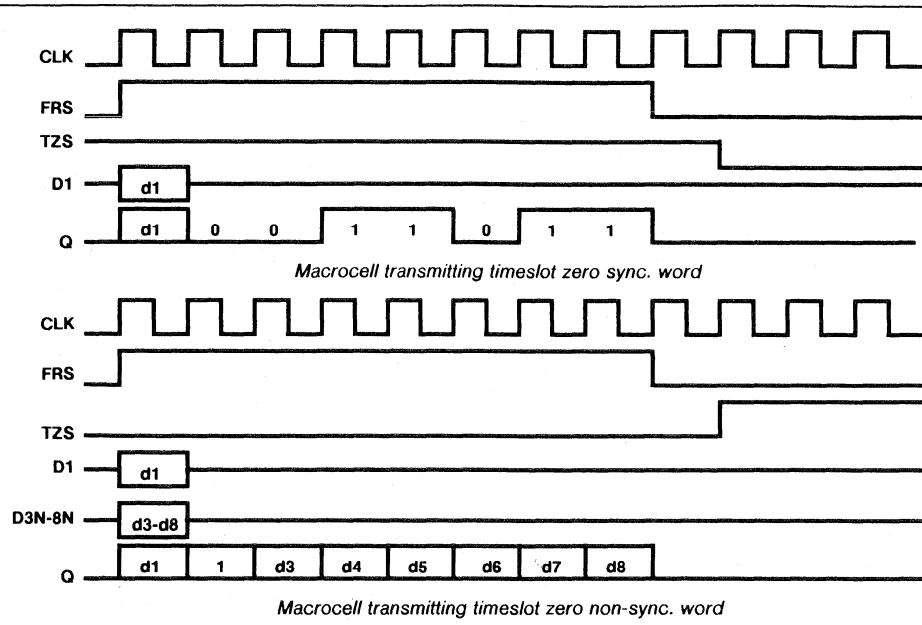


Fig. 3 Timeslot zero transmitter timing

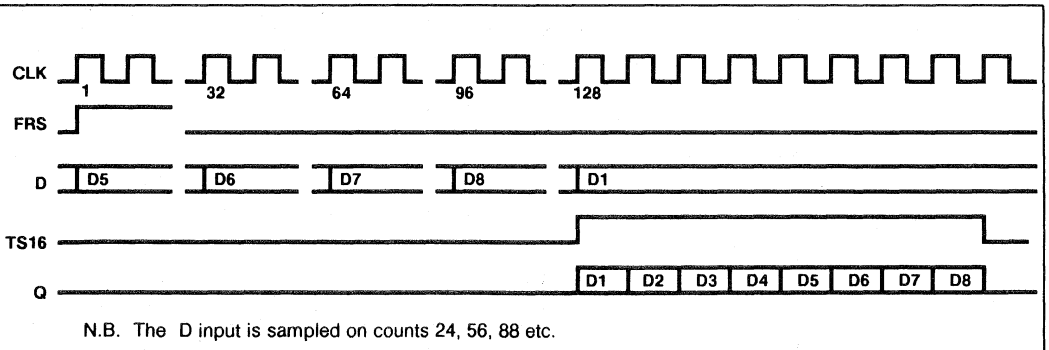


Fig. 4 Timeslot sixteen transmitter timing

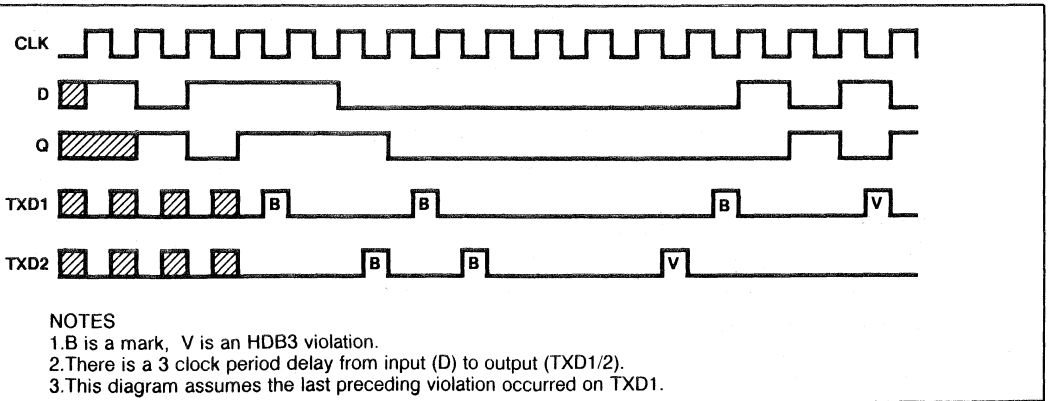


Fig. 5 HDB3 encoder timing

TRANSMIT DEMONSTRATION MODE, TX2

Transmit demonstration mode (MODE = 0, DEMO = 1) uses the four transmitter macrocells connected together internally, to demonstrate how they may be utilised to perform the common channel signalling and error detection functions of a 2.048 Mbit 30 channel PCM transmitter. The functional diagram of the MV1403 in this mode is now as shown in Fig. 6. Again all four macrocells are synchronised to a common 2.048MHz clock with frame synchronisation achieved from the FRS input.

The Timeslot Zero transmitter alternately outputs sync words and non-sync words, during timeslot zero, denoting which by its TZS output. The user data bits of the non-sync word (D3N-D8N) are available as parallel data inputs. The Timeslot Zero data is used as one of the inputs to the transmission multiplexer.

The Timeslot Sixteen transmitter takes in the continuous 64kbit data stream from its D input and outputs this in 8 bit bursts during timeslot 16. This data along with the TS16 frame marker are also used as inputs to the transmission multiplexer, TMUX.

The transmission multiplexer forms a single PCM data stream at its Q output by multiplexing the timeslot zero and timeslot 16 data with the remaining 30 channels (timeslots 1-15 and 17-31) of voice data. This is controlled by the two frame marker inputs to the multiplexer, FRS and TS16.

The output from TMUX is input to the Cyclic Redundancy Check Generator and HDB3 Encoder macrocells.

When in CRC mode (EN = 1), the CRC Generator macrocell performs its CRC procedure on this incoming data stream. In non-CRC mode, this macrocell uses its two data inputs, D1S and D1N, along with the timing input, TZS, to determine its output. However, in CRC mode the output consists of the CRC word data bits interleaved with the CRC multiframe alignment word and the two user data bits, D1S and D1N, as previously displayed in Table 2. In either case, the output data is input directly to the international spare bit input of the Timeslot Zero Transmitter. The TZS input of the CRC generator is connected directly to the TZS output of the Timeslot Zero Transmitter.

The output data from the transmission multiplexer is also input to the HDB3 Encoder macrocell. This macrocell converts the incoming NRZ data into pseudo-ternary HDB3 transmission code, ensuring adequate clock recovery at the receiver. This data is output on the TXD1 and TXD2 output pins. The Q output of the HDB3 Encoder macrocell is a single period delayed version of its D input and as such allows the output from the transmission multiplexer to be observed.

Fig. 6 shows that all of the internal connections except the output from TMUX, are also available as outputs from the MV1403, allowing the interaction of the macrocells to be observed.

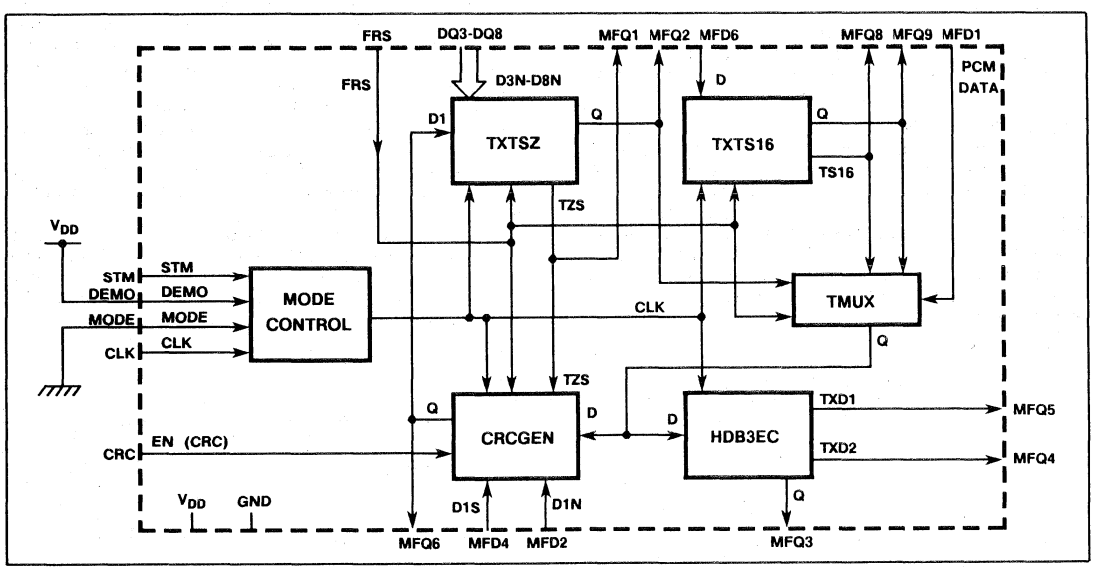


Fig. 6 TX2 Transmit demonstration mode functional diagram

INDIVIDUAL RECEIVE MODE, RX1

In this mode (MODE = 1, DEMO = 0) the MV1403 allows access to the four receiver macrocells (HDB3DC, RXTSZ, RXTS16 and CRCCHK) individually. The functional diagram for the MV1403 in RX1 mode is shown in Fig. 7. The only common connection between the macrocells is the 2.048MHz clock used to synchronise the four macrocells. The function of each individual macrocell is now described separately.

High Density Bipolar (HDB3) Decoder

The HDB3 decoder macrocell decodes the HDB3 pseudo-ternary input data on its inputs, RXD1 and RXD2, into NRZ form to be output on Q. This process is carried out in accordance with CCITT Recommendation G. 703. In addition the macrocell provides two alarm outputs, DV and LIA and a clock recovery output, CDR.

The first of these, DV, is used to signal that a double polarity violation has occurred on one of the pseudo-ternary inputs, whilst the second, LIA (Loss of Input Alarm), signals that eleven consecutive zeros have been received on the inputs. The CDR output is provided to assist regeneration of the 2.048MHz clock. This output is essentially just a logical 'OR' function of the two RXD inputs.

Since either a regenerated clock from the input data or a clock local to the PCM receiver may be used to synchronise the receiver, the two input signals cannot be guaranteed to straddle a rising clock edge and as such the two inputs were made asynchronous by the use of set-reset type latches before the first synchronous storage elements on the inputs.

However, to ensure correct operation of the macrocell the rising edge of either of the RXD inputs should not occur within 50ns of the rising edge of CLK. The timing diagram for this macrocell is shown in Fig. 8.

Timeslot Zero Receiver

This macrocell is principally responsible for searching for and locking on to the Frame Alignment Signal (FAS) present in timeslot zero of the incoming data stream on the D input. This process is carried out in accordance with the loss and recovery of frame alignment strategy described in CCITT Recommendation G.732. When frame alignment has been achieved this macrocell outputs various timing reference signals for use by the other macrocells and external circuitry.

The most important reference signal is the TSZ (Timeslot Zero) output, which is equivalent to the FRS input signal required by the transmitter macrocells. It is an 8 clock period long active high pulse masking Timeslot Zero, allowing the other macrocells to achieve frame alignment. This output will free run when frame alignment is lost. The second timing output is TZS (Timeslot Zero Sync. frame). This 4kHz signal changes state once per frame, one period after the end of Timeslot Zero to identify sync and non sync frames. The TZS output is high during Timeslot Zero of sync frames.

Two timing outputs, $\overline{\text{CCR}}$ (Channel Reset) and CK8, are not used by the other macrocells but may be used by external circuitry. $\overline{\text{CCR}}$ is a low going pulse, one period wide, occurring immediately after each timeslot zero sync frame. CK8 is an 8kHz signal going low at the end of bit 7 in each timeslot zero and high at the end of bit 7 in each timeslot sixteen. The TZS, CK8 and $\overline{\text{CCR}}$ outputs also free run when frame alignment is lost.

Two alarm outputs are provided to signal errors in the incoming data stream. The first of these, is an error alarm, ER, which goes high for one frame following the frame in which a Timeslot Zero sync word, containing a corrupted alignment pattern, has been received. This alarm is only active whilst the receiver is in sync. Note that three consecutive errors of this type will put the receiver out of sync. Thus the second alarm output, SA (Sync. Alarm), goes high when the receiver is out of sync. In additon to the frame synchronisation process, the Timeslot Zero Receiver is also responsible for extracting the user data bits of non-sync words and the two international spare bits. The former of these are accessed via the parallel outputs Q3N-Q8N. The third bit of non-sync words (Q3N) is used as the remote alarm bit from the transmitter and a third alarm output RAI (Remote Alarm Indication), is derived from this bit. This alarm is a persistence checked version of Q3N and when the receiver is in sync, this alarm goes high when two consecutive Q3N bits have been received as high.

In order to extract the international spare bits of Timeslot Zero, the macrocell must be in sync with CRC mode correctly enabled or disabled. This is done using the M input with a logic 'high' on this pin putting the macrocell in CRC mode.

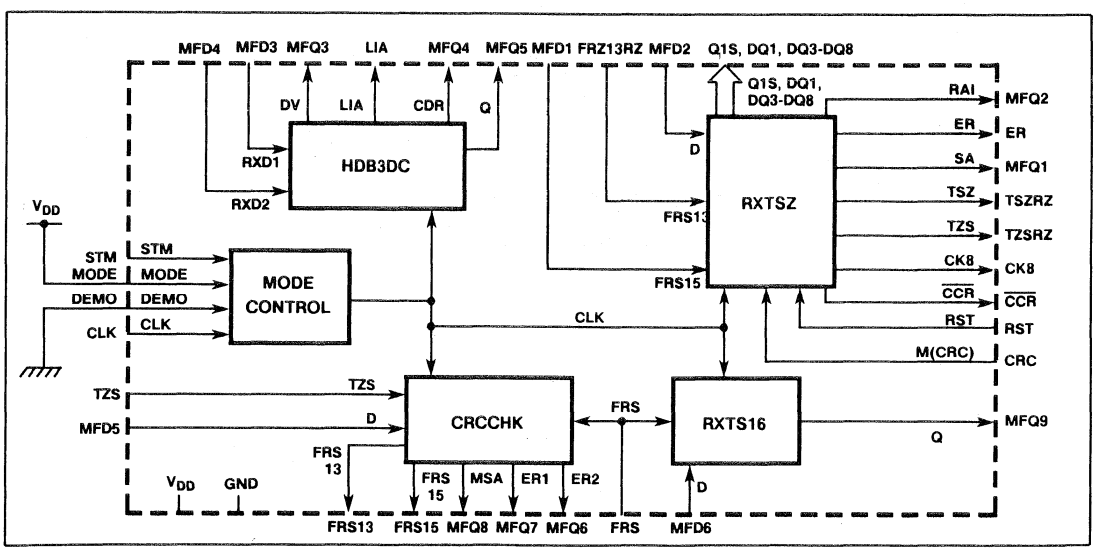
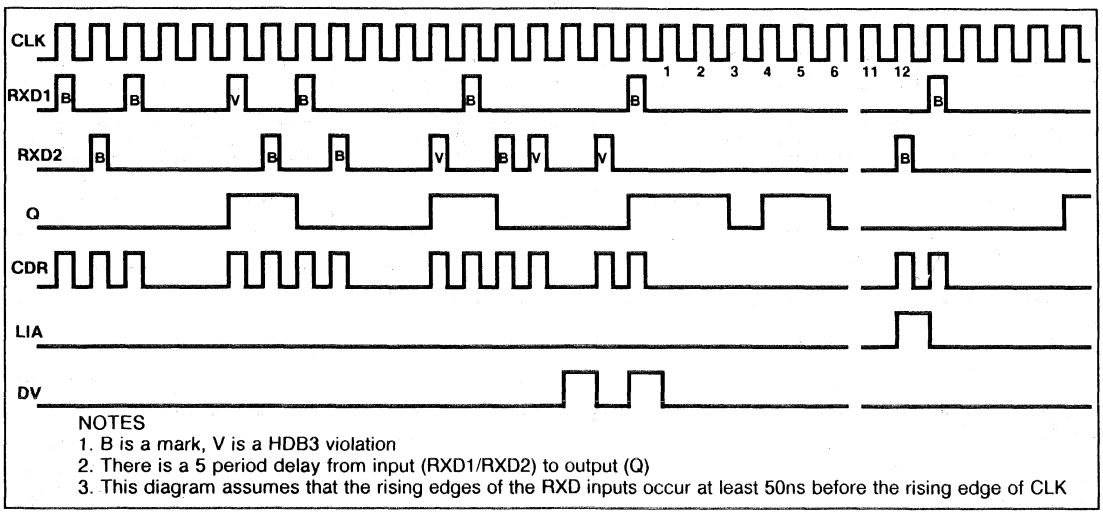


Fig. 7 RX1 individual receive mode functional diagram



NOTES
1. B is a mark, V is a HDB3 violation
2. There is a 5 period delay from input (RXD1/RXD2) to output (Q)
3. This diagram assumes that the rising edges of the RXD inputs occur at least 50ns before the rising edge of CLK

Fig. 8 HDB3 decoder timing - macrocell decoding HDB3 data and detecting errors

When in non CRC mode the international spare bit outputs, Q1S and Q1N, represent data extracted from the bit 1 position of all sync frames and non-sync. frames respectively. If CRC mode is enabled, these outputs now represent data extracted from the bit 1 position of frames 13 and 15 respectively of the CRC multiframe structure. In order to accomplish this, two timing inputs, FRS13 and FRS15, are required. These inputs are required to be high during bit 8 of the appropriate frame, low during bit 8 of any other non-sync frame and any state elsewhere. A final input to this macrocell, RST, may be used to reset the synchronisation process, putting the macrocell out of sync.

Timing diagrams for the Timeslot Zero Receiver macrocell are shown in Fig. 10.

Timeslot Sixteen Receiver

The Timeslot Sixteen Receiver macrocell extracts the 8 bits of common channel signalling data present in Timeslot 16 of successive frames of PCM data input on D. This 2.048Mbit input data burst is stored and output as a continuous 64kbit data stream. A single timing input, FRS, also common to the CRCCHK macrocell, is required, this input being an 8 bit pulse masking Timeslot Zero. Fig. 9 shows the timing of this macrocell.

Cyclic Redundancy Checker

The Cyclic Redundancy Checker macrocell (CRCCHK) performs a cyclic redundancy check procedure on the received data in accordance with CCITT Recommendation G.704, this procedure being performed on the data input on its D input pin. The macrocell also extracts the first bit of each Timeslot Zero (the first bit of each frame) and searches for the CRC Multiframe Alignment Signal (MAS) in the bits from non-sync frames.

When the MAS has been found the macrocell synchronises to it. This process requires two timing inputs, FRS and TZS. The FRS input must be high only during timeslot zero and TZS must be high during timeslot zero of sync frames.

The macrocell generates CRC words from the input data and extracts the CRC bits being received in the first bit of sync frames. Each generated CRC word is compared with the CRC word received in the next sub-multiframe. Associated with this process are three alarm outputs, MSA, ER1 and ER2. The MSA (Multiframe Sync Alarm) output indicates whether multiframe synchronisation has occured. It is high whilst the macrocell is out of sync, and goes low after the beginning of frame 11 in which a correct alignment pattern has been received. The two error outputs, ER1 and ER2 indicate that CRC errors were detected in sub-multiframes 1 and 2 respectively. These two outputs can only change state on the first rising clock edge after the first bit of frames 0 and 8 respectively.

When in CRC multiframe alignment, the macrocell also produces two timing outputs, FRS13 and FRS15, to reference the positions of frames 13 and 15. These signals may be used to allow the Timeslot Zero Receiver macrocell to extract the international spare bits of these frames.

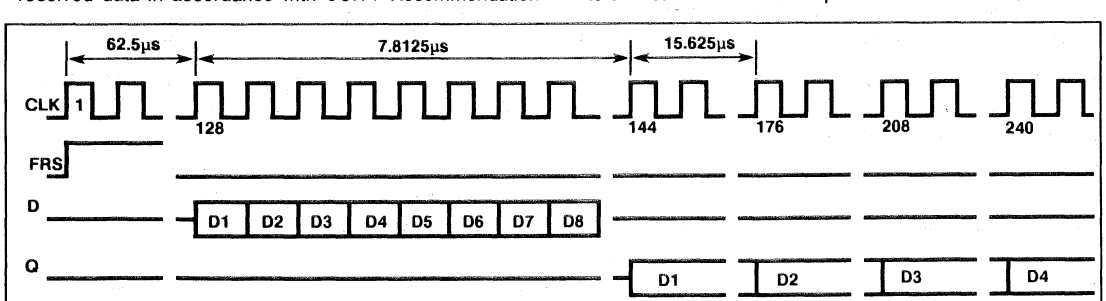


Fig. 9 Timeslot sixteen receiver timing

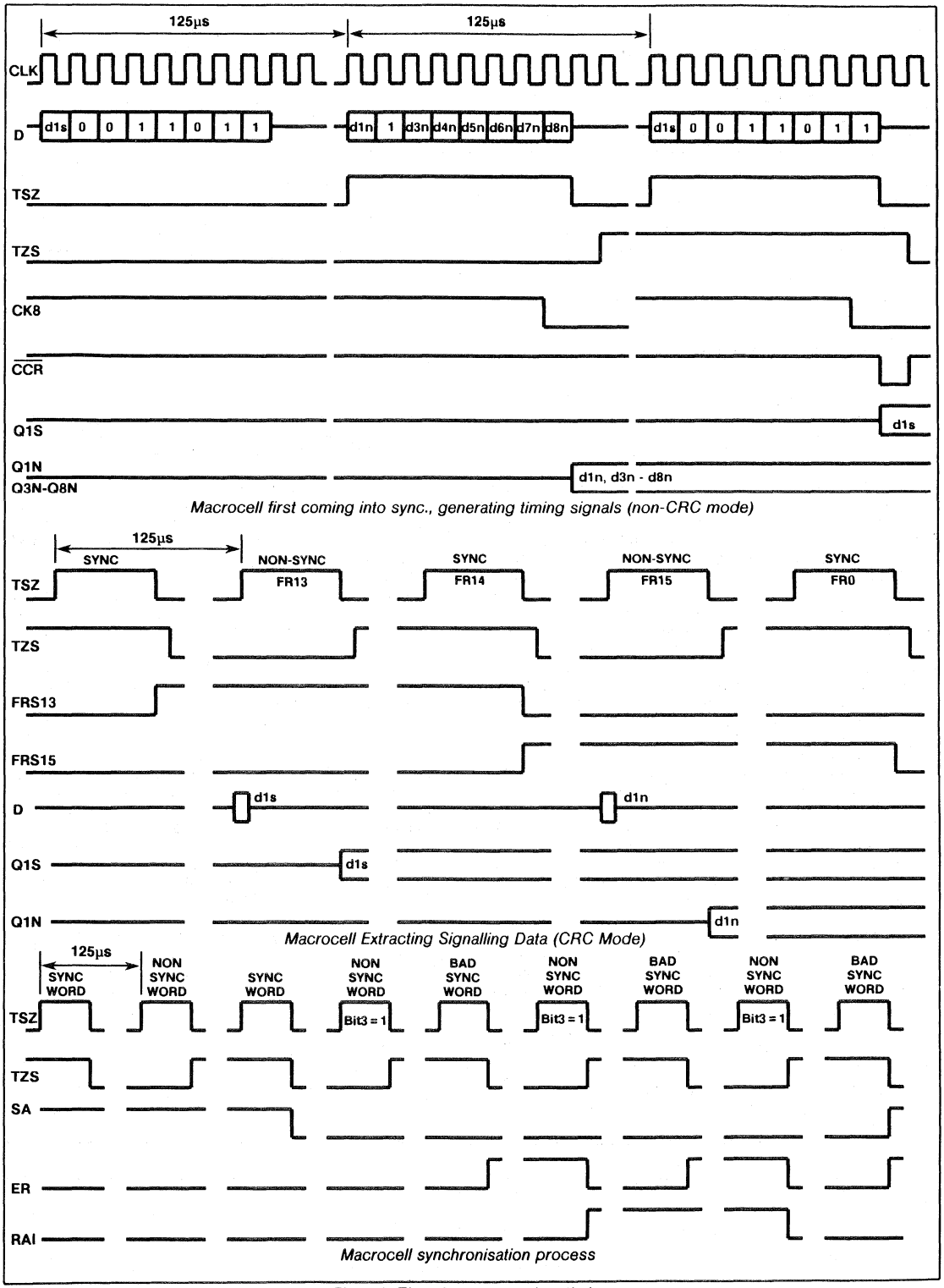


Fig. 10 Timeslot zero receiver timing

RECEIVE DEMONSTRATION MODE, RX2

In the last mode (MODE = 1, DEMO = 1) the four receiver macrocells are connected together internally to demonstrate how they may be utilised to perform the required functions of a 2.048 MBit PCM receiver. The functional diagram of the MV1403 will now be as shown in Fig. 11.

The received pseudo-ternary HDB3 data is input to the HDB3 Decoder macrocell, which decodes this data and outputs it to the other three macrocells and external circuitry, as well as raising appropriate alarms as previously described for the individual receive mode.

The Timeslot Zero Receiver then synchronises itself to the Frame Alignment Signal present in this data stream and produces various timing outputs for use by the remaining two receiver macrocells and external circuitry. In addition this macrocell also raises appropriate alarms as required.

The data being output by the HDB3 decoder is used as the D input to the Timeslot 16 Receiver macrocell which also uses the Timeslot Zero Receiver's TSZ output as its FRS timing input. From this the macrocell determines the position of timeslot 16 and extracts the 8 bits of signalling data from this timeslot. This data is then converted into a continuous 64kbit output data stream.

The Cyclic Redundancy Checker macrocell uses the HDB3 Decoder's output data and the Timeslot Zero Receivers timing outputs TSZ and TZS as its D, FRS and TZS inputs respectively. From this information the macrocell synchronises itself to the CRC multiframe alignment signal and performs its CRC check procedure on the incoming data. Its two timing outputs, FRS13 and FRS15, are input to the Timeslot Zero Receiver to allow it to extract the international spare bits of the CRC multiframe.

In non CRC mode, the Cyclic Redundancy Checker's error outputs are disabled by the alarm gating circuitry. When in CRC mode, this circuitry will also disable the ER1 and ER2 alarms whilst the macrocell is out of multiframe alignment.

In addition to the required outputs, all the internal timing signals are also available as outputs from the MV1403, allowing the interaction of the macrocells to be observed.

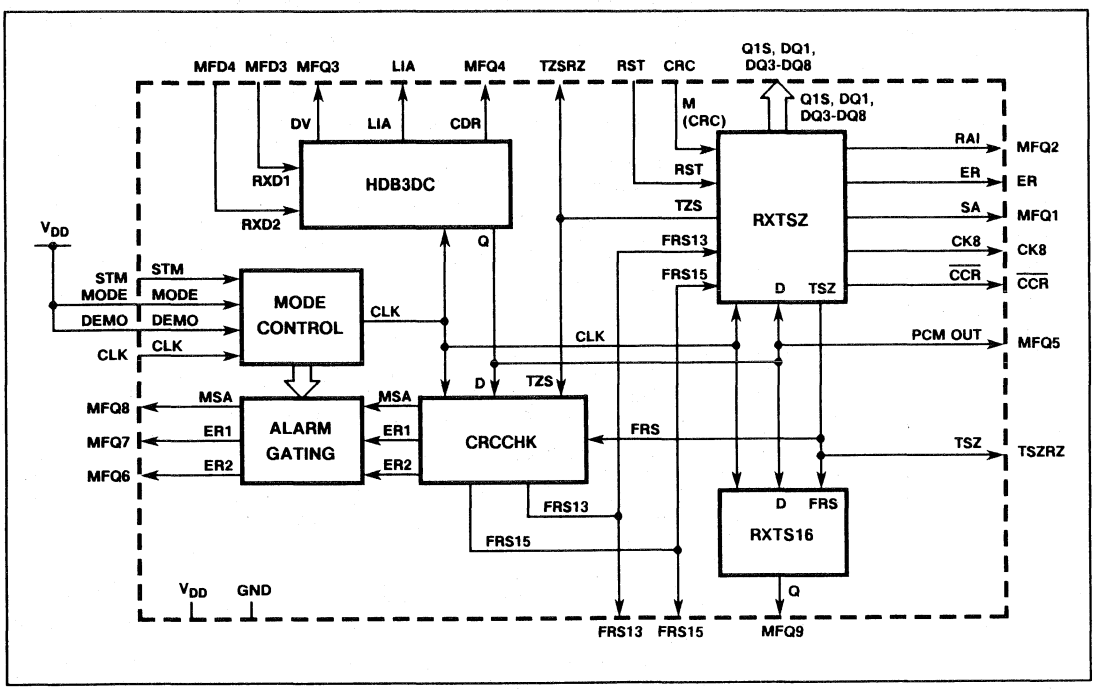


Fig. 11 RX2 receive demonstration mode functional diagram

PIN DESCRIPTIONS

Symbol	Pin no.		Mode name (see note 1)	Pin name and description
	DP48	HP44		
V_{DD1}	1	-	GLOBAL	Digital supply voltage. 5V (Note 2)
ER	2	2	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Sync Word Error Output (ER). This flag goes high for one frame immediately after detection of a bad timeslot zero sync word, whilst the macrocell is in sync. Three consecutive errors of this type will put the receiver out of sync. The last ER pulse of this sequence will be longer than 256 periods if a valid sync word is detected during the pulse.
MFQ1	3	3	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Synchronisation Alarm Output (SA). This error flag goes high when the macrocell is out of sync and only changes state at the end of a sync frame timeslot zero.
			TX	Timeslot Zero Transmitter (TXTSZ) Macrocell - Timeslot Zero Sync frame marker (TZS). This output is high during timeslot zero of sync frames and changes state at the beginning of timeslot one, bit 2 of every frame.
MFQ2	4	4	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Remote Alarm Indication Output (RAI). This is a persistence checked version of the Q3N output. When RXTSZ is in sync, this output goes high if the current and previous timeslot zero bit 3 of non-sync frames are both high. This output changes state at bit 1, timeslot 1 of non-sync frames. When the macrocell is out of sync this output is forced low in the non-sync frame following the last bad sync frame, and is held low until the macrocell comes back into sync.
			TX	Timeslot Zero Transmitter (TXTSZ) Macrocell - Data Output (Q). The sync word and signalling data word appear here in 8 bit bursts during timeslot zero. Bit 1 appears immediately after the rising edges of CLK and FRS. This output is low during all timeslots except timeslot zero.
DQ8 DQ7 DQ6 DQ5 DQ4 DQ3	5 6 7 8 9 10	5 6 7 8 9 10	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Data Outputs (Q8N-Q3N). These outputs are extracted from bits 8-3 of timeslot zero during non-sync frames respectively. These outputs change at the start of bit 1, timeslot 1 of non-sync frames.
			TX	Timeslot Zero Transmitter (TXTSZ) Macrocell Data Inputs (D8N-D3N). These data inputs are inserted into bits 8-3 of timeslot zero during non-sync frames respectively. This data must be set up prior to the rising edge of FRS.
DQ1	11	11	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Data Output (Q1N). With CRC = 0, this output latches data from bit 1, timeslot zero of non-sync frames. The output changes at the beginning of bit 1, timeslot 1 of non-sync frames. With CRC = 1, this output latches data from bit 1 of frame 15 of the CRC multiframe.
			TX1	Timeslot Zero Transmitter (TXTSZ) Macrocell - Data Input (D1). The data on this pin is inserted into the International spare bit (bit 1, timeslot zero of both sync and non-sync frames), and must be set up prior to the rising edge of FRS.
			TX2	This pin is unused since the D1 input of the Timeslot Zero Transmitter is connected internally to the Q output of the CRC Generator.
Q1S	12	12	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Data Output (Q1S). With CRC = 0, this output latches data from bit 1, timeslot zero of sync frames. The output changes at the beginning of bit 1, timeslot 1 of sync frames. With CRC = 1, this output latches data from bit 1 of frame 13 of the CRC multiframe.
V_{DD2}	13	-	GLOBAL	Digital supply voltage. 5V (Note 2)
GND1	14	13	GLOBAL	Digital ground. 0V (Note 2)
LIA	15	14	RX	HDB3 Decoder (HDB3DC) Macrocell - Loss of Input Alarm Output (LIA). This alarm output goes high after 11 consecutive zeros have been detected on the HDB3 inputs. It is reset on detection of a mark (1) on either HDB3 input.

PIN DESCRIPTIONS (continued)

Symbol	Pin no.		Mode name (see note 1)	Pin name and description
	DP48	HP44		
MFQ3	16	15	RX	HDB3 Decoder (HDB3DC) Macrocell - Double Violation Alarm Output (DV). This pin goes high one period after detection of a double violation on either of the HDB3 inputs.
			TX	HDB3 Encoder (HDB3EC) Macrocell - Data Output (Q). This output is a single period delayed version of this macrocells D input.
MFQ4	17	16	RX	HDB3 Decoder (HDB3DC) Macrocell - Clock Regeneration Output (CDR). This output is a logical 'OR' function of the two HDB3 inputs and may be used by external clock regeneration circuitry. This signal has a variable mark-to-space ratio.
			TX	HDB3 Encoder (HDB3EC) Macrocell - HDB3 Encoded Output 2 (TXD2). This output is always low during the high half cycle of clock and is only high the low half cycle if a mark is to be output.
MFQ5	18	17	RX	HDB3 Decoder (HDB3DC) Macrocell - HDB3 Decoded Output (Q). This output is the HDB3 inputs decoded back to NRZ form.
			TX	HDB3 Encoder (HDB3EC) Macrocell - HDB3 Encoded Output 1 (TXD1). As TXD2 (MFQ4).
FRS13RZ	19	18	RX1	Timeslot Zero Receiver (RXTSZ) Macrocell - Frame 13 Marker Input (FRS13). In CRC mode, this input should be high during bit 8, Frame 13 of the CRC multiframe and low during bit 8 of all other non-sync frames.
			RX2	This pin is unused since the FRS13 input of the Timeslot Zero Receiver is connected internally to the FRS13 output of the CRC Checker.
MFD1	20	19	RX1	Timeslot Zero Receiver (RXTSZ) Macrocell - Frame 15 Marker input (FRS15). In CRC mode, this input should be high during bit 8, Frame 15 of the CRC multiframe and low during bit 8 of all other non-sync frames.
			RX2	This pin is unused since the FRS15 input of the Timeslot Zero Receiver is connected internally to the FRS15 output of the CRC Checker.
			TX1	No Connection.
			TX2	PCM Voice Channel Input. In Transmit Demonstration mode this pin is used as the serial data input to the Transmission Multiplexer.
MFD2	21	20	RX1	Timeslot Zero Receiver (RXTSZ) Macrocell - Data Input (D). This pin is used to input the 2.048 Mbit data stream to this macrocell.
			RX2	This pin is unused since the D input of the Timeslot Zero Receiver is connected internally to the Q output of the HDB3 Decoder.
			TX	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Signalling Data Input (D1N). This pin is used to input the data to be inserted into bit 1 of non-sync frames (CRC = 0) or bit 1 of frame 15 of the CRC multiframe (CRC = 1).
MFD3	22	21	RX	HDB3 Decoder (HDB3DC) Macrocell - Data Input 1 (RXD1). This input latches the incoming HDB3 encoded data and is rising edge sensitive. The rising edge of this input should not occur within 50 ns of the rising edge of CLK.
			TX1	HDB3 Encoder (HDB3EC) Macrocell - Data Input (D). This pin is used to input NRZ data for conversion into pseudo ternary HDB3 format.
			TX2	This pin is unused since the D input of the HDB3 Encoder is connected internally to the Q output of the Transmission Multiplexer.
MFD4	23	22	RX	HDB3 Decoder (HDB3DC) Macrocell - Data Input 2 (RXD2). As RXD1 (MFD3)
			TX	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Signalling Data Input (D1S). This pin is used to input the data to be inserted into bit 1 of sync frames (CRC = 0) or bit 1 of frame 13 of CRC multiframe (CRC = 1).
V_{DD3} V_{DD}	24 -	- 23	GLOBAL	Digital supply voltage. 5V (Note 2)

Symbol	Pin no.		Mode name (see note 1)	Pin name and description
	DP48	HP44		
GND2	25	-	GLOBAL	Digital ground. 0V (Note 2)
DEMO	26	24	GLOBAL	Demonstration pin. A logic high on this pin puts the MV1403 into demonstration mode, RX2 or TX2 with all the transmit or receive macrocells connected together internally. A low on this pin allows access to the macrocells individually (ie. RX1 or TX1 mode).
MODE	27	25	GLOBAL	Transmit/Receive Mode pin. A logic high on this pin places the MV1403 in Receive mode RX1 or RX2. A low places it in Transmit mode TX1 or TX2.
CLK	28	26	GLOBAL	2.048MHz Master Clock input.
STM	29	27	GLOBAL	Scan Path Test Mode pin. A logic high on this pin places the MV1403 in scan test mode. For normal operation this pin should be tied low.
P	30	28	GLOBAL	Scan Test Data input. In Scan Path Test Mode, this pin is used as the input to the scan path.
CRC	31	29	GLOBAL	CRC Mode pin. This pin is used as the CRC mode input to the CRCGEN (EN input) or RXTSZ (M input) macrocells. A logic high on this pin will put the MV1403 into Cyclic Redundancy Check mode.
MFD5	32	30	RX1	Cyclic Redundancy Checker (CRCCHK) Macrocell - Data Input (D). This pin is used as the 2.048Mbit serial data input to this macrocell.
			RX2	This pin is unused since the D input of the CRC Checker is connected internally to the Q output of the HDB3 Decoder.
			TX1	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Data Input (D). This pin is the 2.048 Mbit data input to this macrocell.
			TX2	This pin is unused since the D input to the CRC Generator is connected internally to the Q output of the Transmission Multiplexer.
FRS	33	31	RX1	Frame Sync Input (FRS). This pin is the 8kHz timeslot zero frame marker input to the Timeslot Sixteen Receiver (RXTS16) and Cyclic Redundancy Checker (CRCCHK) macrocells. It is required to be high only during timeslot zero of each frame.
			RX2	This pin is unused since the FRS inputs to the CRC Checker and Timeslot 16 Receiver are connected internally to the TSZ output of the Timeslot Zero Receiver.
			TX	Frame Sync Input (FRS). This pin is the 8kHz timeslot zero frame marker input. It is required to be high only during timeslot zero of each frame.
TZS	34	32	RX1	Cyclic Redundancy Checker (CRCCHK) Macrocell - Timeslot Zero Sync Frame Marker Input (TZS). This 4KHz input is required to be high during timeslot zero of sync frames and change at the beginning of bit 2, timeslot 1 of every frame.
			RX2	This pin is unused since the TZS input of the CRC Checker is connected internally to the TZS output of the Timeslot Zero Receiver.
			TX1	Cyclic Redundancy Check Generator (CRCGEN) Macrocell Timeslot Zero Sync Frame Marker Input (TZS). This 4kHz input is required to be high during timeslot zero of sync frames and change at the beginning of bit 2, timeslot 1 of every frame.
MFD6	35	33	RX1	Timeslot Sixteen Receiver (RXTS16) Macrocell - 2.048Mbit Serial Data Input (D). The 8 bits of signalling data in timeslot 16 are extracted from this input during timeslot 16.
			RX2	This pin is unused since the D input of the Timeslot 16 Receiver is connected internally to the Q output of the HDB3 Decoder.
			TX	Timeslot Sixteen Transmitter (TXTS16) Macrocell - 64kbit Signalling Data Input (D). The continuous stream of data to be output as 8 bit bursts during timeslot 16 is input on this pin.
GND3	36	-	GLOBAL	Digital ground,0V. (Note 2)

PIN DESCRIPTIONS (continued)

Symbol	Pin no.		Mode name (see note 1)	Pin name and description
	DP48	HP44		
RST	37	34	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Reset Input (RST). A logic high on this pin will reset the state machine of this macrocell, forcing the macrocell out of frame alignment. Due to the 100kΩ pull-up resistors on all the inputs, this pin should be tied low when not in use.
MFQ6	38	35	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Sub-multiframe 2 Error Alarm Output (ER2). A logic high on this output indicates the detection of a CRC error in sub-multiframe 2.
			TX	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Data Output (Q). This pin is used to output the data to be inserted into bit 1, timeslot 0.
MFQ7	39	36	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Sub-multiframe 1 Error Alarm Output (ER1). A logic high on this output indicates the detection of a CRC error in sub-multiframe 1.
			TX	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Scan Test Data Output (STQ). In scan test mode, this pin is the scan path output of this macrocell.
MFQ8	40	37	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Multiframe Sync Alarm Output (MSA). A logic high on this output denotes that the macrocell is out of CRC multiframe alignment.
			TX	Timeslot Sixteen Transmitter (TXTS16) Macrocell - Timeslot 16 Marker Output (TS16). This output is high only during timeslot 16.
FRS15	41	38	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Frame 15 Marker Output (FRS15). When the macrocell is in CRC multiframe alignment, this output is high during frame 15 and low during all other non-sync frames.
FRS13	42	39	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Frame 13 Marker Output (FRS13). When the macrocell is in CRC multiframe alignment, this output is high during frame 13 and low during all other non-sync frames.
MFQ9	43	40	RX	Timeslot Sixteen Receiver (RXTS16) Macrocell - 64kbit Signalling Data Output (Q). This pin is used to output the 8 bits of signalling data extracted from timeslot 16 as a continuous 64kbit data stream.
			TX	Timeslot Sixteen Transmitter (TXTS16) Macrocell - Signalling Data Output (Q). The 8 bit data bursts produced by this macrocell are output at 2.048MHz on this pin during timeslot 16. This output is low at all other times.
TSZRZ	44	41	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Timeslot Zero Marker Output (TSZ). This output goes high for the 8 periods of timeslot zero and is low at all other times.
TZSRZ	45	42	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Timeslot Zero Sync Frame Marker Output (TZS). This output is high during timeslot zero of sync frames and changes state at the beginning of bit 2, timeslot 1 of every frame.
CK8	46	43	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - 8kHz Clock Output (CK8). This output goes low at the end of bit 7, timeslot zero and high at the end of bit 7, timeslot 16.
$\overline{CCR}$	47	44	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Channel Reset Output ($\overline{CCR}$). This output pulses low for a single period during bit 1, timeslot 1 of sync frames.
GND4 GND2	48	- 1	GLOBAL	Digital ground. 0V (Note 2).

NOTES

1. TX refers to TX1 and TX2 modes. RX refers to RX1 and RX2 modes. GLOBAL refers to all modes.
2. All the V_{DD} and GND pins of the 48-pin device, and two GND pins of the 44-pin device are connected together internally and as such there is no need to connect up all these supplies. However, it is recommended that all supply pins are connected to facilitate supply decoupling.
3. Since the device is intended as a demonstrator allowing access to the individual macrocells, 100kΩ pull-up resistors have been included on all the input pins to prevent any unconnected inputs from floating.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Supply Voltage V_{DD} = 5V ±0.5V, Ambient Temperature T_{amb} = 0 to 70°C.

STATIC CHARACTERISTICS

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Low level input voltage	V_{IL}	0		0.8	V	
High level input voltage	V_{IH}	2.0		V_{DD}	V	
Low level output voltage	V_{OL}	0		0.4	V	I_{SINK} = 10mA
High level output voltage	V_{OH}	2.4		V_{DD}	V	I_{SOURCE} = 5mA
Input leakage current	I_{IL}	-20		-200	µA	$V_{IN} = V_{SS}$
		-10		+10	µA	$V_{IN} = V_{DD}$
Supply current	I_{CC}		1.5	3.0	mA	All outputs unloaded
Input capacitance	C_{IN}		5		pF	
Output capacitance	C_{OUT}		5		pF	

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Clock						
Clock frequency	f_{CLK}		2.048		MHz	
Clock rise time	t_{CR}			20	ns	See Fig. 12
Clock high time	t_{CH}	150			ns	See Fig. 12
Clock fall time	t_{CF}			20	ns	See Fig. 12
Clock low time	t_{CL}	150			ns	See Fig. 12
Outputs						
Output propagation delay	t_{OPD}			50	ns	See Fig. 17, note 1
CDR propagation delay	t_{CDRPD}			50	ns	See Fig. 18
Frame synchronisation & related inputs						
FRS rising hold time	t_{FRH}	50			ns	See Fig. 13
FRS rising setup time	t_{FRS}	100			ns	See Fig. 13
FRS falling hold time	t_{FFH}	50			ns	See Fig. 13
FRS falling setup time	t_{FFS}	100			ns	See Fig. 13
TZS setup time	t_{SFS}	50			ns	See Fig. 13
TZS hold time	t_{SFH}	50			ns	See Fig. 13
User data setup time	t_{UDS}	50			ns	See Fig. 13
International data bits setup time	t_{IDS}	100			ns	See Fig. 13
Timeslot Zero data hold time	t_{TZDH}	100			ns	See Fig. 13
Data inputs						
Data setup time	t_{DS}	50			ns	See Fig. 14, note 2
Data hold time	t_{DH}	50			ns	See Fig. 14, note 2
Timeslot 16 transmitter data setup time	t_{T16DS}	50			ns	See Fig. 15, note 3
Timeslot 16 transmitter data hold time	t_{T16DH}	50			ns	See Fig. 15, note 3
HDB3 input data setup time	t_{RXDS}	50			ns	See Fig. 16
HDB3 input data pulse width	t_{RXDW}	50		488	ns	See Fig. 16

NOTES

1. The output propagation delay, t_{OPD}, is valid for all outputs except CDR (from the HDB3DC macrocell) and is specified with FRS rising before CLK. All output delays are measured with a 50pF load.
2. The data setup and hold parameters, t_{DS} and t_{DH}, apply to the following macrocell inputs: D (CRCGEN), D (HDB3EC), PCM DATA (TMUX), D (RXTSZ), FRS13/15 (RXTSZ), RST (RXTSZ), D (RXTS16), D (CRCCHK), P (GLOBAL)
3. Timeslot 16 transmitter data setup and hold times apply to the rising edge of clock cycles 24, 56, 88 etc. (see Fig. 4).

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings are limiting values above which opertaing life may be shortened or specified parameters may be degraded.

Positive supply voltage, V_{DD}	- 0.5 to + 7V
Inputs	V_{DD} + 0.3V to GND - 0.3V
Outputs	V_{DD} + 0.3V to GND - 0.3V

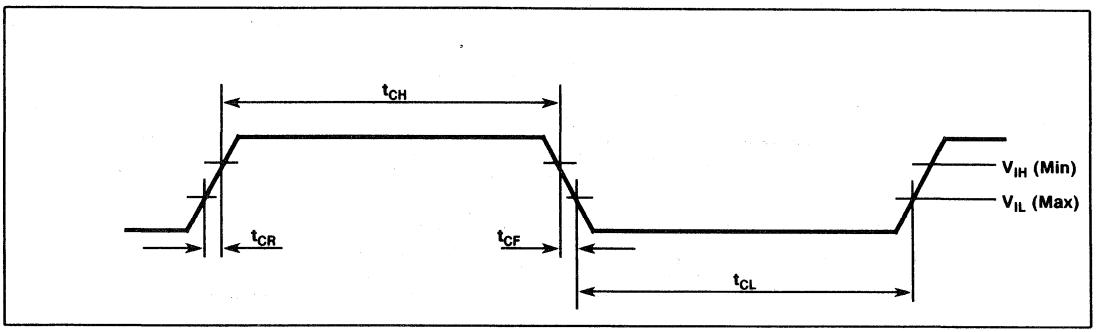


Fig. 12 Timing - clock inputs

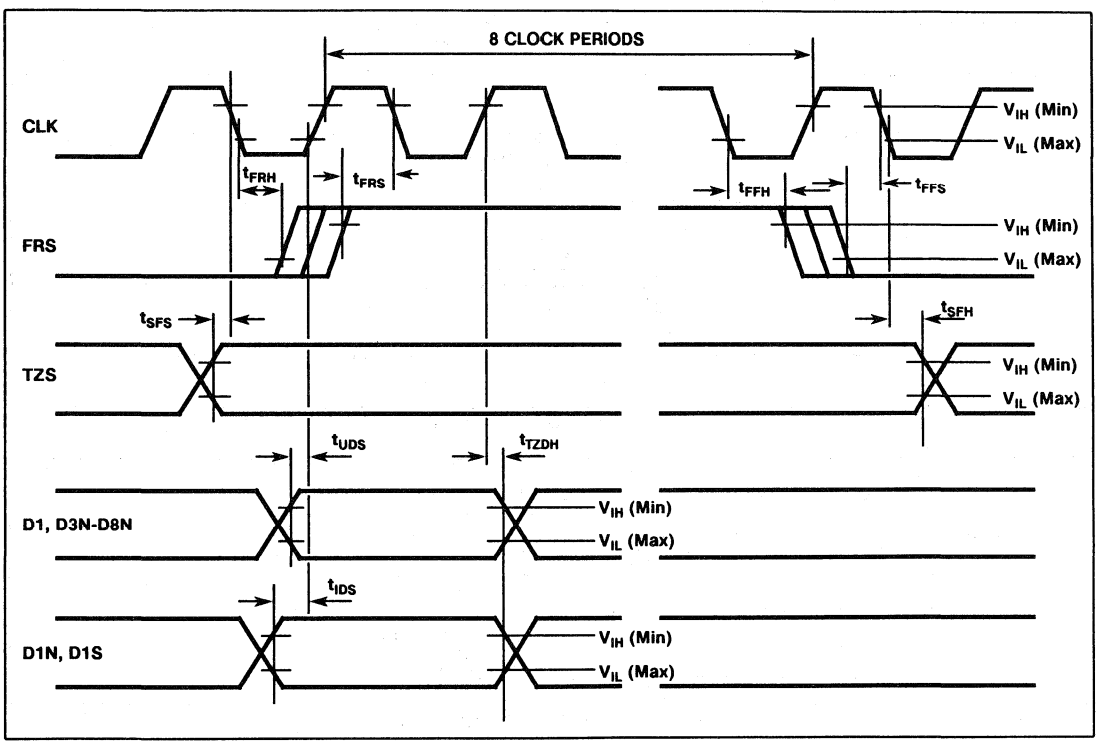


Fig. 13 Timing - FRS and related parameters

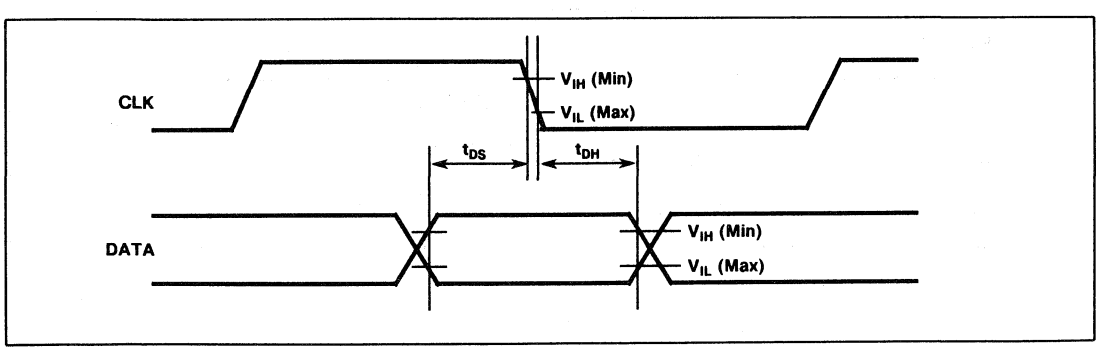


Fig. 14 Timing - data inputs

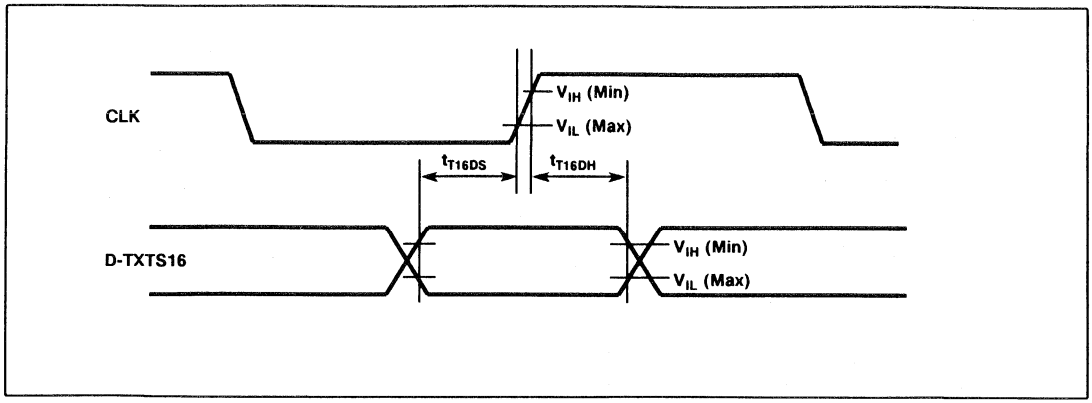


Fig. 15 Timing - Timeslot 16 transmitter data input

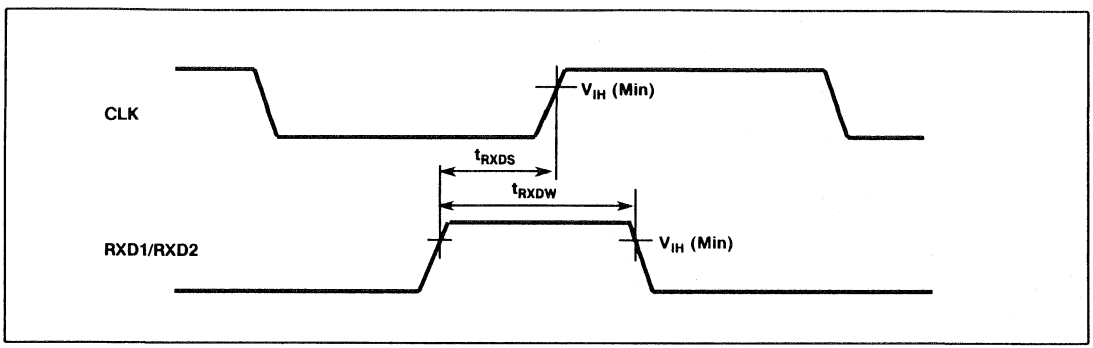


Fig. 16 Timing - RXD inputs

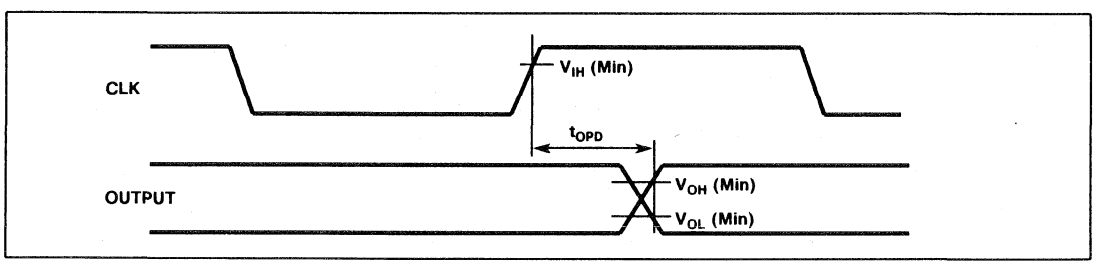


Fig. 17 Timing - output propagation delay

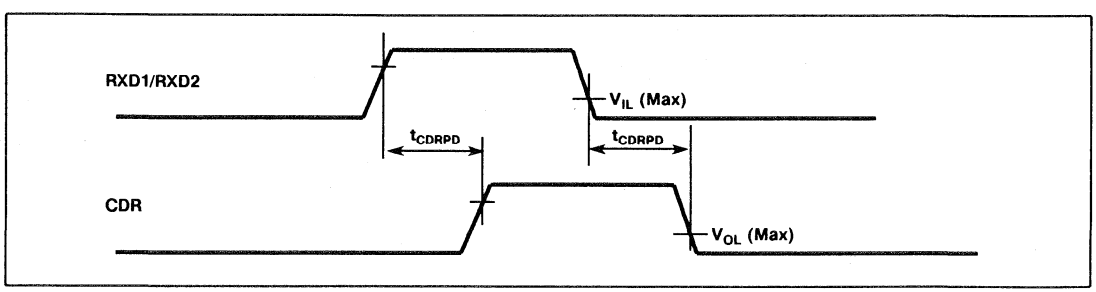


Fig. 18 Timing - CDR propagation delay

PCBAN93

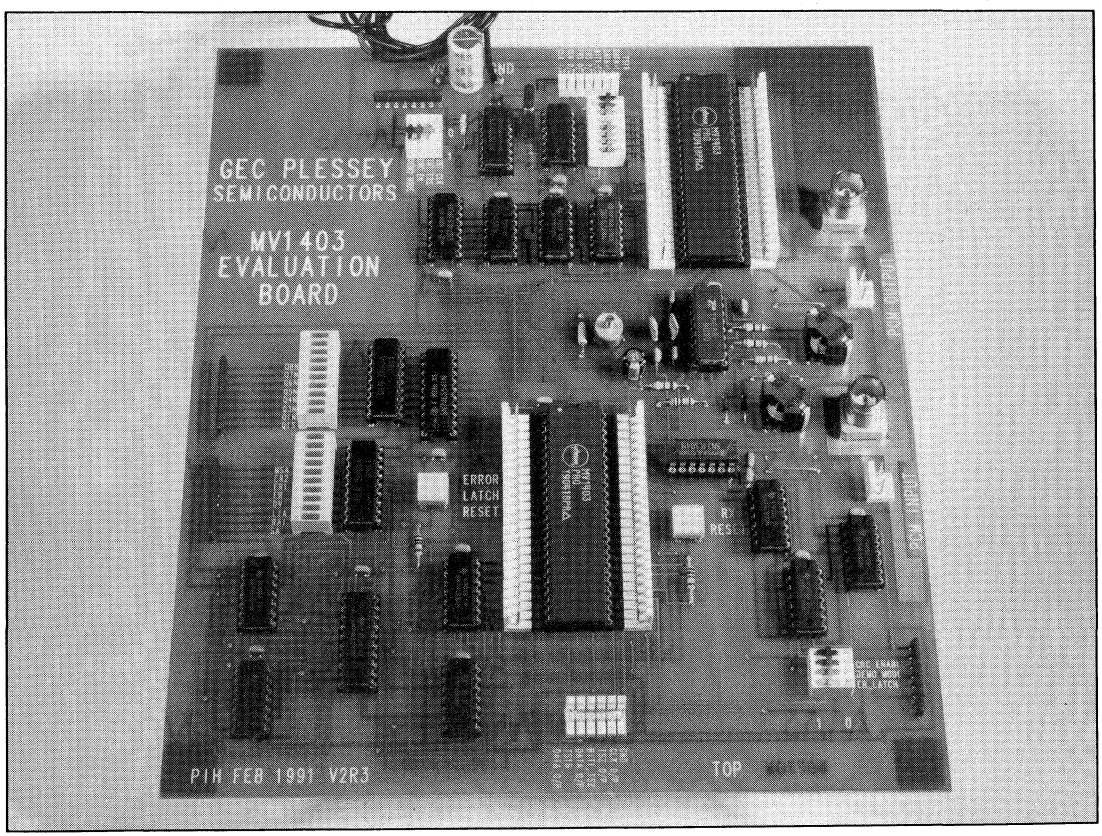
MV1403 PCM DEMONSTRATOR EVALUATION BOARD

Now available from GPS is an evaluation board for the MV1403 PCM Demonstrator chip. The board contains two MV1403 devices, one used for transmit and the second used for receive PCM functions. In addition, a line interface circuit is included to provide a complete demonstration of all the available Telecom PCM Macrocells within the MV1403.

For more details of the evaluation board, reference should be made to Application Note AN93. The MV1403 Data Sheet contains descriptions of the individual macrocells, whilst detailed design data is available in the CLA60000 Design Manual.

FEATURES

- Contains Two MV1403 PCM Demonstrator Devices, One For Transmit and One For Receive Directions.
- Transmit Mode Provides TS0 Transmit, TS16 Transmit, HDB3 Encode and CRC Generator Functions.
- Receive Mode Provides TS0 Receive, TS16 Receive, HDB3 Decode and CRC Checking Functions.
- 75Ω Coax or 120Ω Twisted Pair Line Driver and Receiver Circuitry With Clock Recovery Contained On Board.
- Single and 8 Periods of Clock Sync Signals Available for Synchronisation of External COMBO/SLAC Devices.
- Internal or External Transmit Clock and Frame Sync Options.
- Generates and Monitors Spare Time Slot Zero Data Bits.
- Displays Status of all Receive Error, Violation and Sync Alarm Outputs.
- Application Note AN93 fully Describes the Operation and Uses of the Evaluation Board.



The PCBAN93 evaluation board.

DS3162-1.1
Supersedes C48 Issue 2

MA808

FRAME ALIGNER WITH OPTIONAL TIME SLOT ZERO RECEIVER

The MA808 Frame Aligner chip has been primarily designed for use in equipment operating at the CCITT standard of 2048 kbit/s for 30 channel PCM data signals.

The basic function of the device is to accept a 2048 kbit/s data signal, whose frame structure conforms to CCITT recommendation G732 and frame synchronously align it to a local exchange/system clock.

The frame aligner operation is such that once a synchronisation sequence, as defined in CCITT recommendation G732, is received from a distant source synchronisation is established. Consequently the data stream is delayed such as to align it to the timing required at the local source. Once three successive sync. words are received containing errors, synchronisation is lost. The chip will remain out of sync. until the synchronising sequence is received.

The device can also, when configured in the 'enhanced mode' perform the additional function of time slot zero recovery.

A number of facilities are also provided to simplify the testing of the device and associated system.

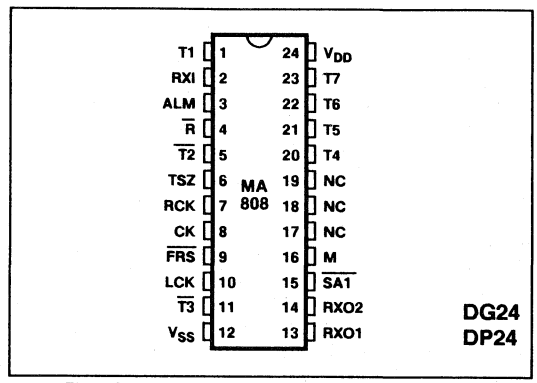


Fig.1 Basic Mode pin connections - top view. M tied to V_{SS}

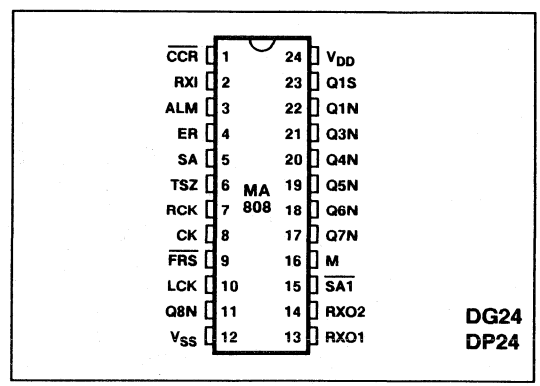


Fig.2 Enhanced Mode pin connections - top view. M tied to V_{DD}

FEATURES

- Fabricated in Low Power CMOS
- Optional Time Slot Zero Receiver
- Detection of Frame Alignment Signals for 30 Channel PCM Highways Operating at 2048 kbit/s in Accordance with CCITT Recommendations G732
- Delay Compensation and Clock Alignment between
- the Transmission Line system and the Exchange
- Compensation of Phase Jitter, Meeting the Requirements of CCITT
- Detection and Indication of Loss of Frame Alignment
- Provision of a Signal for Generation of AIS
- Slip Compensation
- Chip Functional Test Facilities
- TTL Compatible
- Operating Power Consumption 75mW max.
- Single +5V Supply
- High Latch-up Immunity
- 256 kHz Clock Output

APPLICATIONS

- Digital Multiplex Equipment
- Interfaces between PCM Line and Switching Systems
- Concentrators

OPERATION IN BASIC MODE ($M = V_{SS}$)

Frame Alignment

The remote non-return-to-zero (NRZ) binary PCM data stream (RXI) required to be aligned must be applied to the frame aligner along with a synchronous clock (RCK). A time slot zero impulse (TSZ) as shown in Fig. 5 is also required to define the start of the frame of input data.

A local clock (LCK) provides the timing from which the output data is clocked. Frame reset pulse ($\overline{FRS}$) is the data output timing pulse. The MA808 aligns the 16th bit of the incoming data to this pulse, as shown in Fig. 5, and the two NRZ binary outputs RXO1 and RXO2 are produced. RXO1 is purely a retimed version of the input data. RXO2 has the third bit of all time slot zero locations of the input data inverted, thereby deliberately corrupting the frame sync. and the frame sync. verification words. Once synchronisation has been established $\overline{FRS}$ may be removed. If synchronisation is lost, $\overline{FRS}$ must be reapplied in order to permit resynchronisation to be established.

Slip Compensation

Small differences in frequency between the local and remote clocks (LCK and RCK) are compensated for by the repetition of the previous frame, ('slipping in') or the omission of one complete frame of data ('slipping out').

Input Alarms

Two input alarms ($\overline{SA1}$ and ALM) are provided which will set data output(s) to an 'all ones' condition. ALM sets only RXO2 and $\overline{SA1}$ sets both RXO1 and RXO2 high (Fig. 6).

Test Features

The operation of the internal memory of the MA808 is continuously monitored by performing a check sum comparison of the input and output data signals RXI and RXO1. When an error is detected, the time slot zero words of RXO1 and RXO2 are set 'high'.

When a 'low' is applied to test input $\overline{T3}$, the outputs RXO1, RXO2 and CK are forced into a high impedance condition, thereby allowing associated circuitry to be tested independently of the MA808. Note that this facility is only available in the basic mode of operation.

OPERATION IN ENHANCED MODE ($M = V_{DD}$)

When configured in the enhanced mode the chip performs time slot zero (TS0) recovery in addition to the frame alignment function. TS0 recovery may also be performed independently.

Frame Alignment

The operation of frame alignment is essentially the same as the basic mode, except that the TSZ pulse is an output rather than an input, in accordance with the operation of the TS0 receiver, as shown in Fig. 7. The operation of the input alarms to set the output data 'high' is the same as described in the basic mode (Fig. 6).

Time Slot Zero Receiver

Two output signals (TSZ and $\overline{CCR}$) are provided so that the time slot zero receiver may be used independently of the frame alignment function. $\overline{CCR}$ is a channel reset pulse (as shown in Fig. 7) which goes 'low' for one RCK period following a sync. word (every alternate frame) when the device is in sync. When the device is out of sync. the reset pulse occurs after each time slot zero.

The TS0 receiver accesses information contained within time slot zeros and processes it to offer the facilities of synchronisation alarm (SA), error output (ER) and time slot zero spare bits (Q1S, Q1N, Q3N-Q8N).

Synchronisation Alarm (SA)

SA indicates loss of sync. as shown in Fig. 8. With the frame aligner operating in sync., SA will be 'low'. Following the receipt of 3 successive sync. words containing errors, SA will become active. SA will remain 'high' until the correct synchronising sequence as defined in CCITT recommendations G732 has been received.

Error Output (ER)

A logic signal, ER, indicating errors in sync. words, is provided as shown in Fig. 8, from which an AIS alarm may be generated. ER is activated at the beginning of the second bit of time slot 1 two frames after the receipt of a sync. word containing errors. If successive sync. words contain errors, the signal will remain active.

If synchronisation is lost, ER will remain active but will go 'low' for one period of the remote clock during the second bit of time slot 1, two frames after the receipt of the last valid sync. word, as long as synchronisation is not regained at this time.

If synchronisation is regained, ER will go 'low' for the two frames following the sync. word which caused synchronisation to be regained. The signal indicating an error in the sync. word two frames prior to synchronisation being regained will be delayed by one further sync. frame period. Consequently, it may be concluded that all errors in sync. words are accounted for in this signal, hence error monitoring in accordance with CCITT recommendation G732.3.1.6.1 may be performed.

Time Slot Zero Spare Bits

The spare bits contained in both time slot zero words are converted from serial to parallel format (Q1N, Q3N-Q8N inc. and Q1S) are shown in Fig. 9.

PIN DESCRIPTIONS - BASIC MODE

Pin	Def.	Function	Description
1	T1	Test input	Active high. To be tied to logic low during normal operation.
2	RXI	Data input	Recovered distant data input.
3	ALM	Alarm input	A logic high on this input sets RXO2 to an all 1s condition.
4	$\overline{R}$	Reset input	'Low' resets the device tied 'high' normally.
5	$\overline{T2}$	Test input	Active low. To be tied to logic high during normal operation.
6	TSZ	TSO input	Remote TS0 timing signal.
7	RCK	Clock input	Recovered distant clock in sync. with RXI.
8	CK	256kHz output	256kHz square wave clock output synchronous with LCK.
9	$\overline{FRS}$	Timing input	Data output timing pulse coincident with 16th bit of the local clock.
10	LCK	Clock input	Local clock input.
11	$\overline{T3}$	Test input	Active low. To be tied to logic high during normal operation.
12	V_{SS}	Negative supply	Nominally 0V.
13	RXO1	Data output	Retimed data output to LCK.
14	RXO2	Data output	As RXO1 except that bit 3 of each TS0 word is inverted.
15	$\overline{SA1}$	Set to all 1s input	A logic low sets RXO1 and RXO2 to an all 1s condition.
16	M	Mode input	Connected to V_{SS} for basic mode operation.
17	NC	No connection	To be left O/C during normal operation.
18	NC	No connection	To be left O/C during normal operation.
19	NC	No connection	To be left O/C during normal operation.
20	T4	Test input	Active when clocked by LCK (pin 10). To be tied to logic low during normal operation.
21	T5	Test input	Active when clocked by RCK (pin 7). To be tied to logic low during normal operation.
22	T6	Test output	To be left O/C during normal operation.
23	T7	Test output	To be left O/C during normal operation.
24	V_{DD}	Positive supply	Nominally +5V.

PIN DESCRIPTIONS - ENHANCED MODE

Pin	Def.	Function	Description
1	$\overline{CCR}$	Channel reset	An output used to reset other devices within the system.
2	RXI	Data input	Recovered distant data input.
3	ALM	Alarm input	A logic high on this input sets RXO2 to an all 1s condition.
4	ER	Error output	A TS0 word error is signalled when ER goes to logic high.
5	SA	Sync. alarm O/P	Loss of sync. is signalled when SA goes to logic high.
6	TSZ	TSO output	Remote TS0 output signal, (internally connected to the on-chip frame aligner).
7	RCK	Clock input	Recovered distant clock in sync. with RXI.
8	CK	256kHz output	256kHz square wave clock output synchronous with LCK.
9	$\overline{FRS}$	Timing input	Data output timing pulse coincident with 16th bit of the local clock.
10	LCK	Clock input	Local clock input.
11	Q8N	Output signal	Signal corresponding to bit 8 of the TS0 sync. verification word.
12	V_{SS}	Negative supply	Nominally 0V.
13	RXO1	Data output	Retimed data output to LCK.
14	RXO2	Data output	As RXO1 except that bit 3 of each TS0 word is inverted.
15	$\overline{SA1}$	Set to all 1s input	A logic low sets RXO1 and RXO2 to an all 1s condition.
16	M	Mode input	Connected to V_{DD} for enhanced mode operation.
17	Q7N	Output signal	Signal corresponding to bit 7 of the TS0 sync. verification word.
18	Q6N	Output signal	Signal corresponding to bit 6 of the TS0 sync. verification word.
19	Q5N	Output signal	Signal corresponding to bit 5 of the TS0 sync. verification word.
20	Q4N	Output signal	Signal corresponding to bit 4 of the TS0 sync. verification word.
21	Q3N	Output signal	Signal corresponding to bit 3 of the TS0 sync. verification word.
22	Q1N	Output signal	Signal corresponding to bit 1 of the TS0 sync. verification word.
23	Q1S	Output signal	Signal corresponding to bit 1 of the TS0 sync. word.
24	V_{DD}	Positive supply	Nominally +5V.

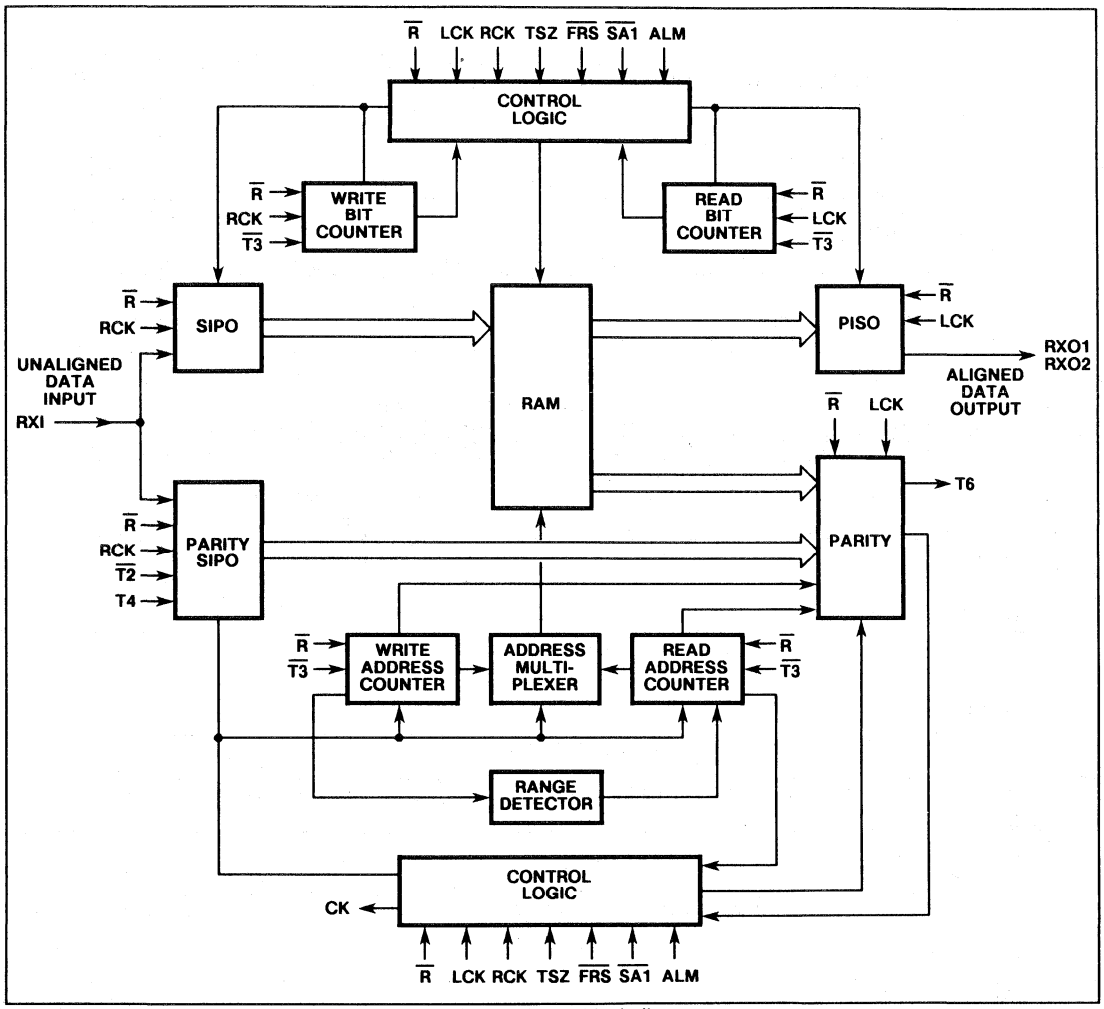


Fig.3 Frame aligner block diagram

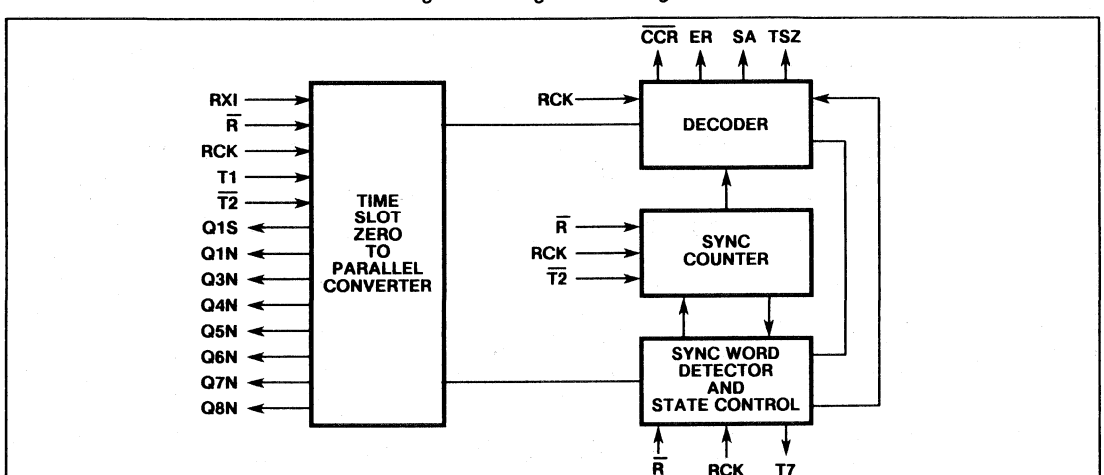


Fig.4 TS0 receiver block diagram

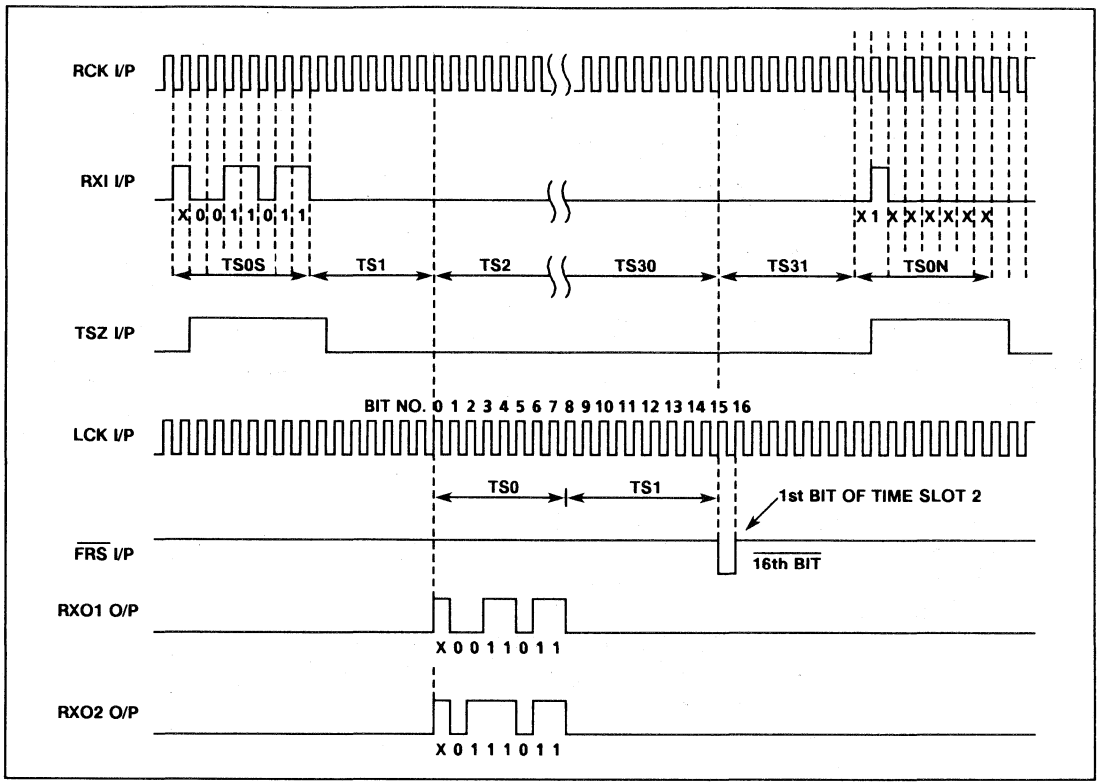


Fig.5 Timing diagram - basic mode: general operation of frame alignment

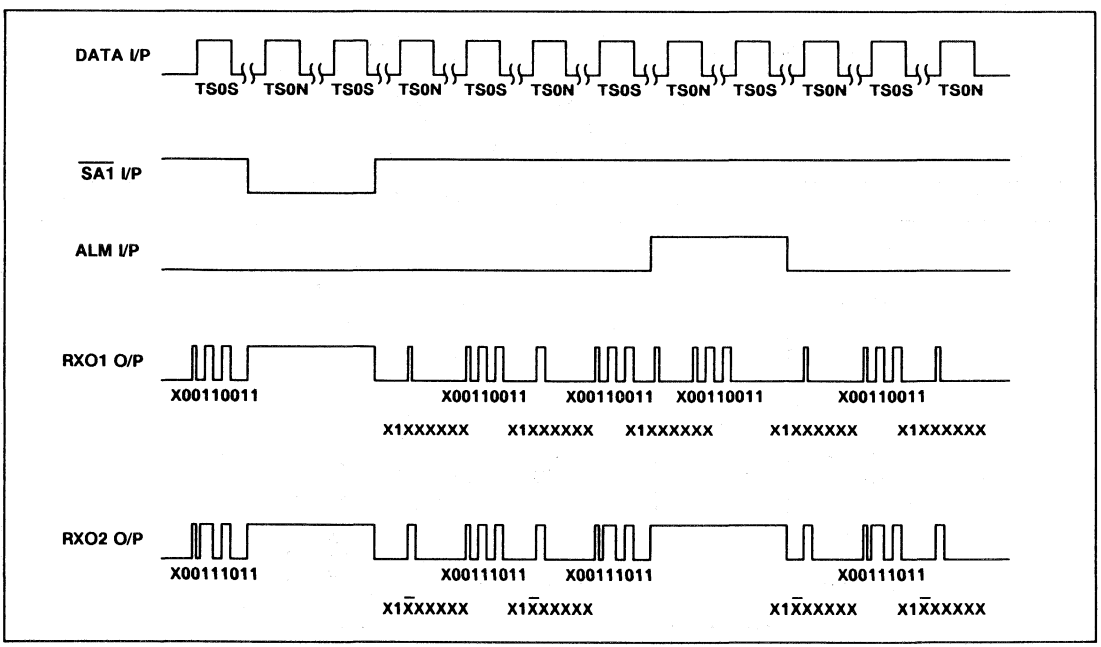


Fig.6 Timing diagram - basic mode: protocol timings of the alarm signals

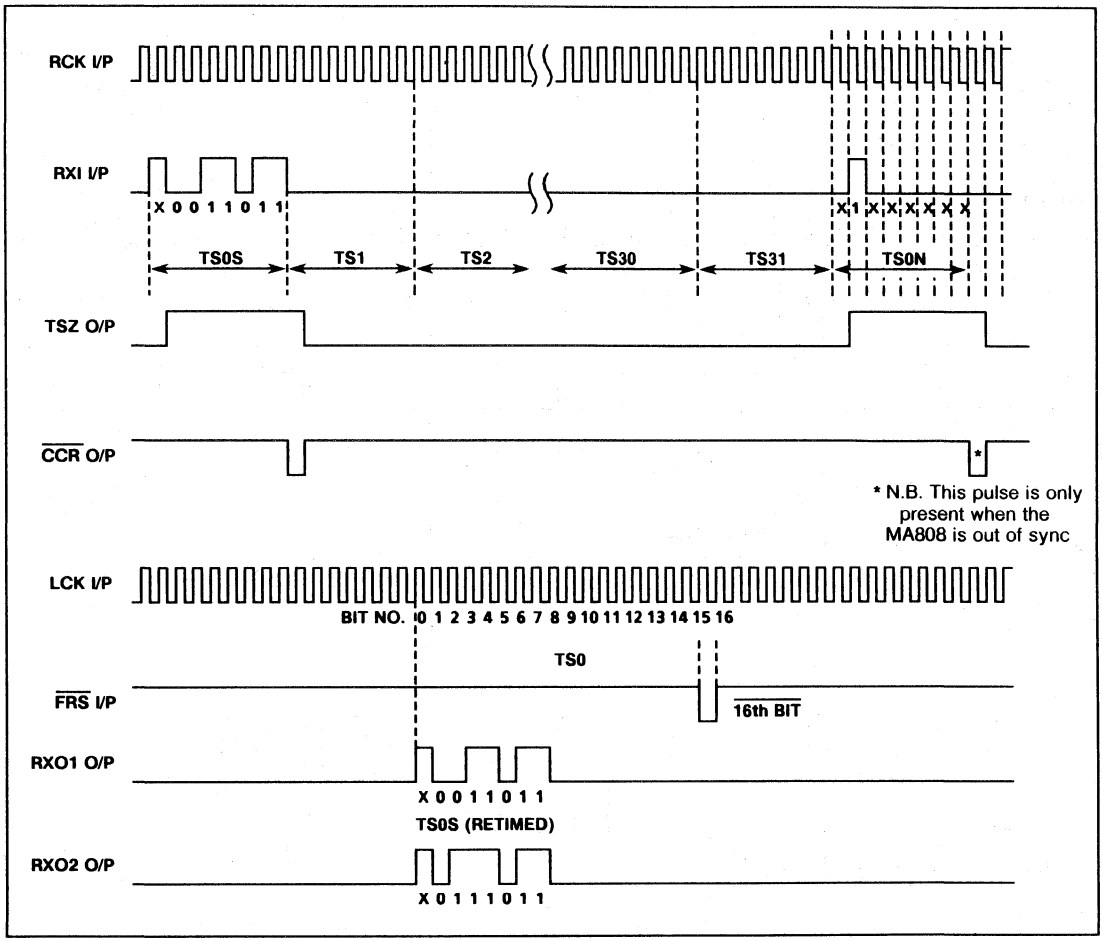


Fig.7 Timing diagram - enhanced mode: general operation of frame aligner

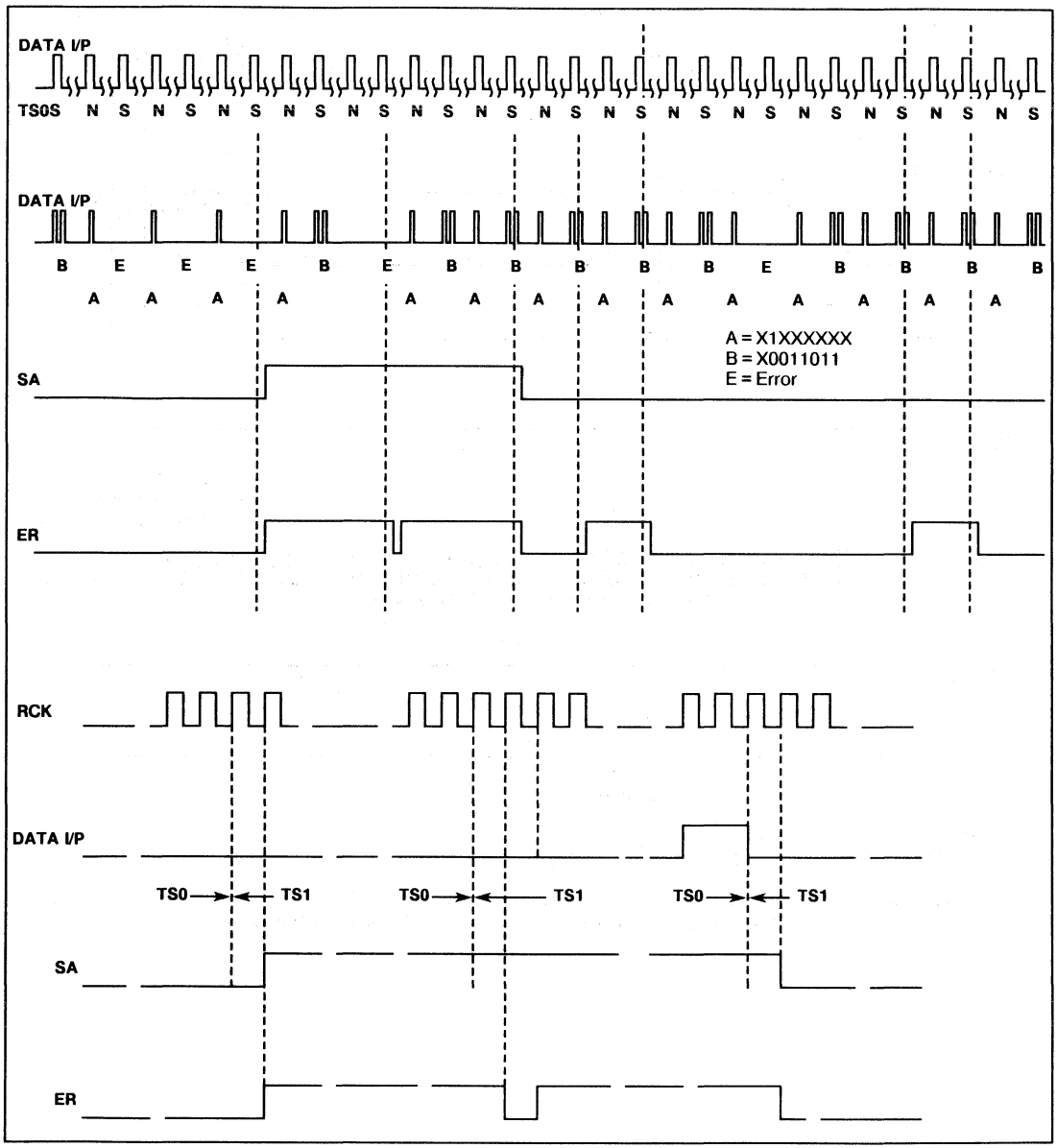


Fig.8 Timing diagram - enhanced mode: protocol timings of TS0 receiver alarms

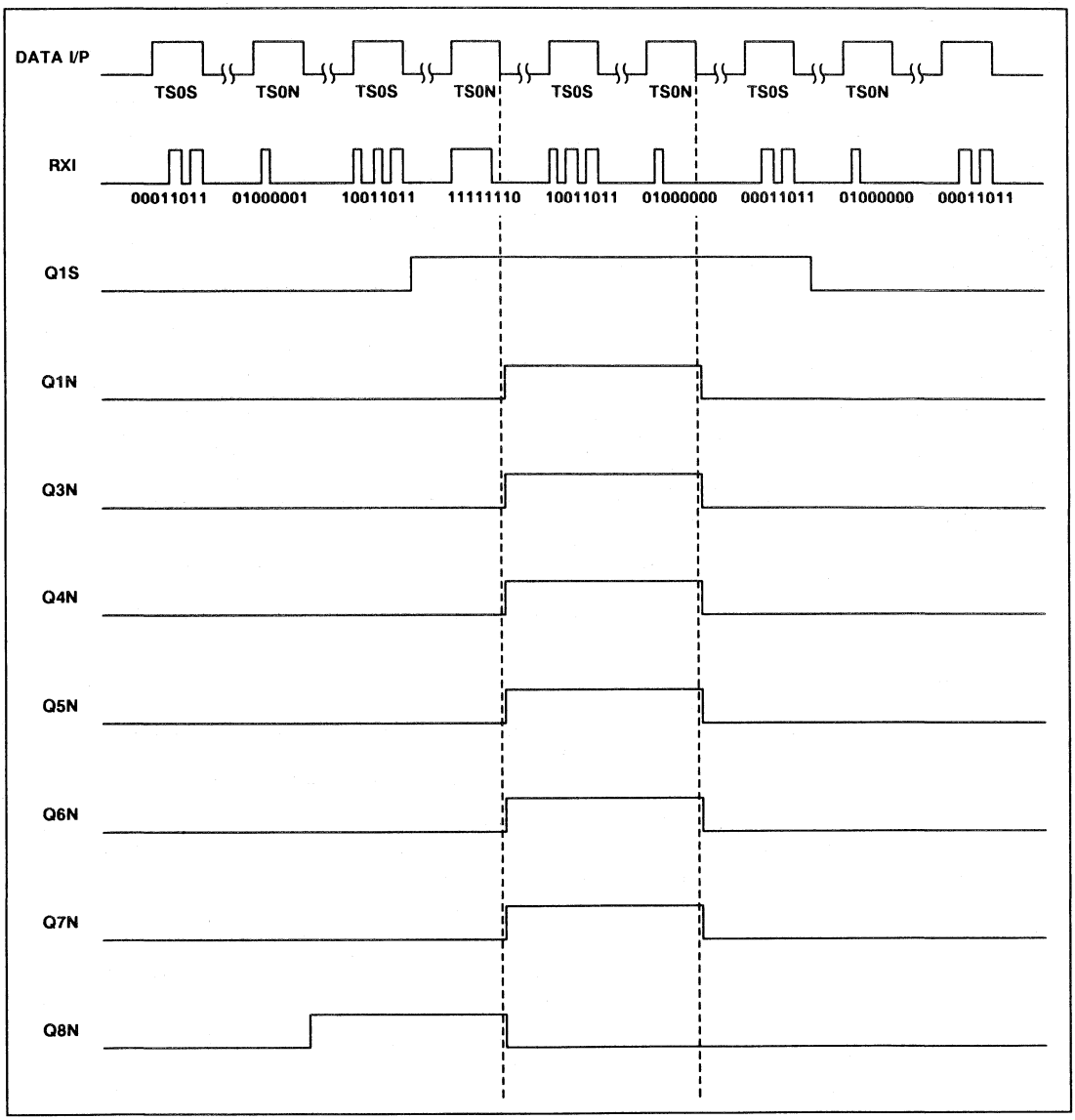


Fig.9 Timing diagram - enhanced mode: protocol timings of the signal lines

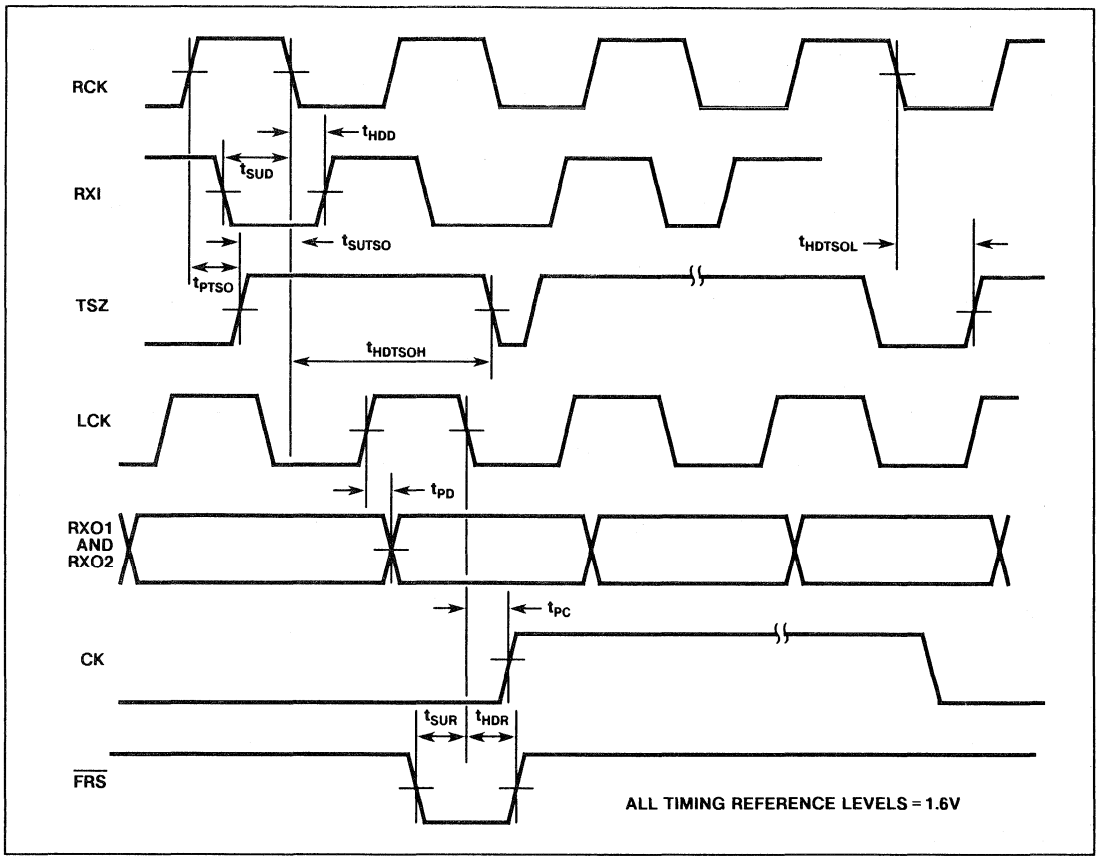


Fig.10 Timing diagram - basic and enhanced mode timing waveforms

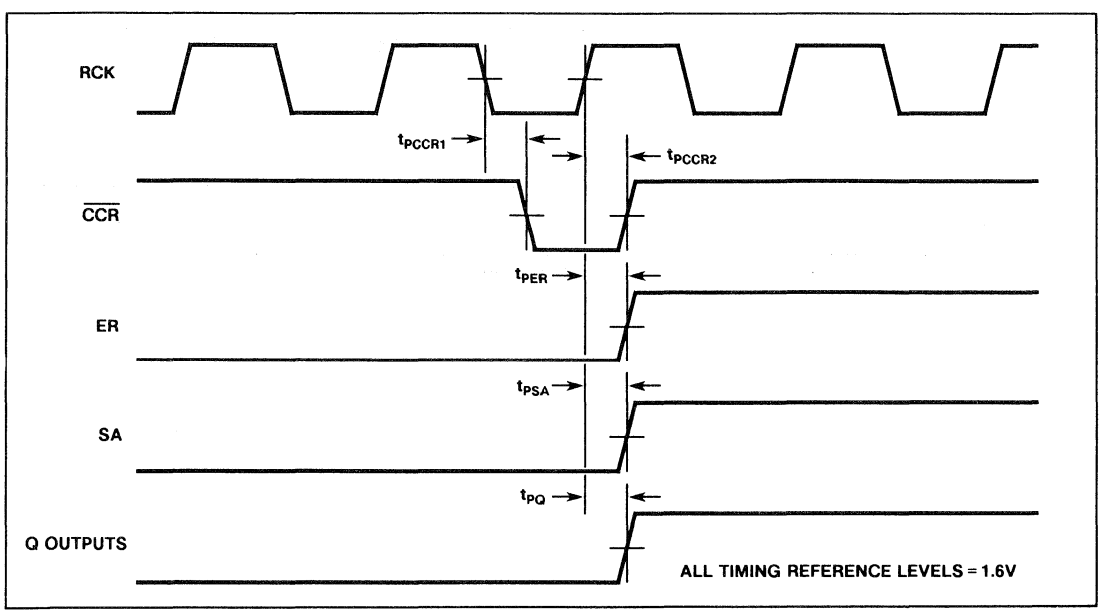


Fig.11 Timing diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{AMB} = +25°C

DC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Low level input voltage	V_{IL}			0.8	V	V_{DD} = 4.75V
High level input voltage	V_{IH}	2.4			V	V_{DD} = 5.25V
Low level input current	I_{IL}			10	μA	$V_{IN} = V_{SS}$, V_{DD} = 5.25V
High level input current	I_{IH}			10	μA	$V_{IN} = V_{DD}$ = 5.25V
Low level output voltage	V_{OL}			0.5	V	I_{OL} = 2mA, V_{DD} = 4.75V
High level output voltage	V_{OH}	2.8			V	I_{OH} = 0.2mA. V_{DD} = 4.75V
Output leakage current	I_{OL}			±10	μA	$V_{SS} < V_{OUT} < V_{DD}$, V_{DD} = 5.25V
Dynamic supply current	I_{DDD}			15	mA	
Static supply current	I_{DDS}			1	mA	

AC Timing Characteristics (Refer to Figs. 10 and 11)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Set up time RXI to RCK (H→L)	t_{SUD}	25			ns	
Set up time TSZ to RCK (H→L)	t_{SUTSO}	20			ns	
Set up time $\overline{FRS}$ to LCK (H→L)	t_{SUR}	150			ns	
Data hold time wrt RCK (H→L)	t_{HDD}	100			ns	
TSZ (L) hold time wrt RCK (H→L)	t_{HDTSOL}	50			ns	
TSZ (H) hold time wrt RCK (H→L)	t_{HDTSOH}	100			ns	
$\overline{FRS}$ hold time wrt LCK (H→L)	t_{HDR}	150			ns	
Nominal frequency	f		2.048		MHz	
Propagation delay, LCK to RXO1 and RXO2	t_{PD}	30		150	ns	Outputs loaded to 10pF, f_{CLOCK} = 2.048MHz
Propagation delay, LCK (H→L) to CK	t_{PC}	0		175	ns	
Propagation delay, RCK (H→L) to $\overline{CCR}$ (H→L)	t_{PCCR1}	0		150	ns	
Propagation delay, RCK (L→H) to $\overline{CCR}$ (L→H)	t_{PCCR2}	0		200	ns	
Propagation delay, RCK (L→H) to TSZ	t_{PTSO}	20		200	ns	
Propagation delay, RCK (L→H) to ER	t_{PER}	20		200	ns	
Propagation delay, RCK (L→H) to SA	t_{PSA}	20		200	ns	
Propagation delay, RCK (L→H) to Q8N–Q3N, Q1N and Q1S	t_{PQ}	20		200	ns	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}–V_{SS}	–0.3 to +7.0V
Voltage on any pin (V_{IN}) (See note 1)	V_{SS} – 0.3V to V_{DD} + 0.3V
Current through any pin (See note 1)	±20mA
Storage temperature	–55°C to +125°C
Operating temperature range	–10°C to +55°C

NOTES

1. Guaranteed no latch-up conditions.
2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DS3163-1.0
Supersedes C1080FDS Issue 2

MA8112

DIGITAL SWITCH MODULE (DSM)

The MA8112 is a CMOS device providing digital switching for up to 256 8-bit channels as used in PCM or data systems. 8-bit words are received and transmitted at 2.048 Mb/s on each of eight input and eight output lines respectively either in a parallel format with 256 consecutive channels or in serial format with 32 channels multiplexed on to each of the eight lines.

The device operates unidirectionally and allows 8-bit words from any incoming channel to be switched to any outgoing channel, under the control of an on-chip connection memory, which may be updated or interrogated via an external control interface. The control interface and addressing facilities are designed to allow easy expansion to provide greater switching capacity.

Applications include PCM switching systems in which up to 32 x 64 Kb/s speech/data channels are time division multiplexed on to a single line in accordance with CCITT Recommendation G732 2.048Mb/s format.

Alternatively, the device can be used as a high speed data switch at data rates up to 2.048 Mb/s and can be used to convert 8-bit channels from serial to parallel format or vice-versa.

The MA8112 is pin-compatible with the MS2002.

FEATURES

- Single 5V Supply
- Low Power CMOS Design
- Inputs and Outputs TTL Compatible
- Compatible with CCITT 32-Channel 2.048 Mb/s Format (Rec. G732)
- 256 Input/256 Output Channels
- Inputs and Outputs can be Serial or Parallel
- Variable Input/Output Frame Delay
- Designed to allow Easy Expansion into Larger Switches Matrices

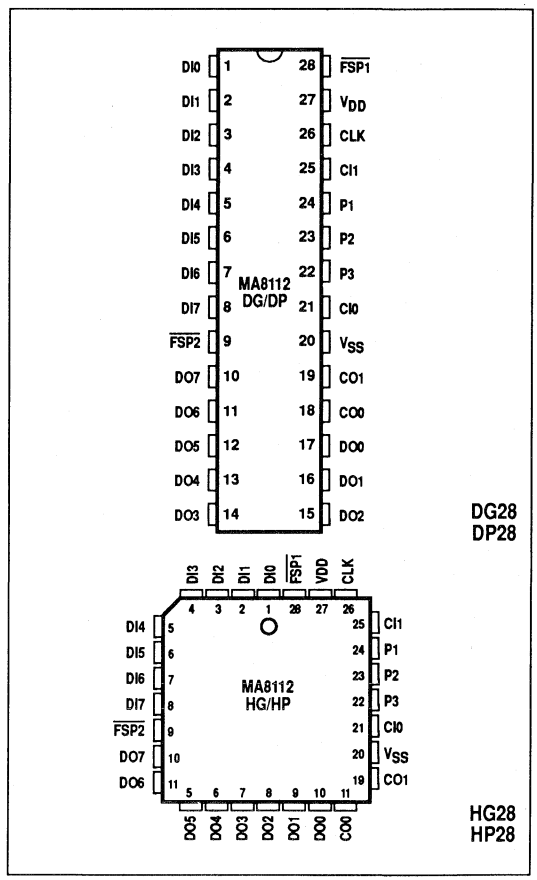


Fig.1 Pin connections - top view

FUNCTIONAL DESCRIPTION

The MA8112 Digital Switch Module is designed to provide switching for 256 x 8-bit PCM encoded speech or data channels operating at rates up to 2.048 Mb/s. The input and output data is handled in frames containing 256 8-bit channels in either serial or parallel format and repeating at a rate of up to 8 kHz. The format of these frames is shown in Fig. 3. When operating at 2.048 Mb/s in serial input/output mode, 32 channels each operating at a rate of 64 kb/s are multiplexed on to each line according to CCITT specifications for PCM transmission (Recommmendation G732).

The input frame to output frame delay is variable (up to one frame period) with the input channel data stored on-chip until being sent to the appropriate output channel. The switching of any input channel is independent of any other channel and once set up, the connection between an input channel and an output channel is maintained until a new connection is specified via the control interface.

Switching is achieved as follows:

The MA8112 contains two read/write memories- the SPEECH (i.e. PCM) memory and the CONNECTION memory.

In the speech memory, there is one 8-bit location dedicated to each of the 256 8-bit PCM (speech) input channels. In each frame of incoming data, each 8-bit PCM word will be written to a location in the speech memory according to its input channel. This operation is repeated in successive frames.

In the connection memory, there is one location dedicated to each of the 256 PCM output channels. Each of these locations contains an 8-bit word which is used to address one of the 256 locations in the speech memory (and hence one of the 256 input channels). The PCM word contained in this location is then sent to the output channel concerned. Thus switching of an 8-bit word between an input channel and an output channel is achieved.

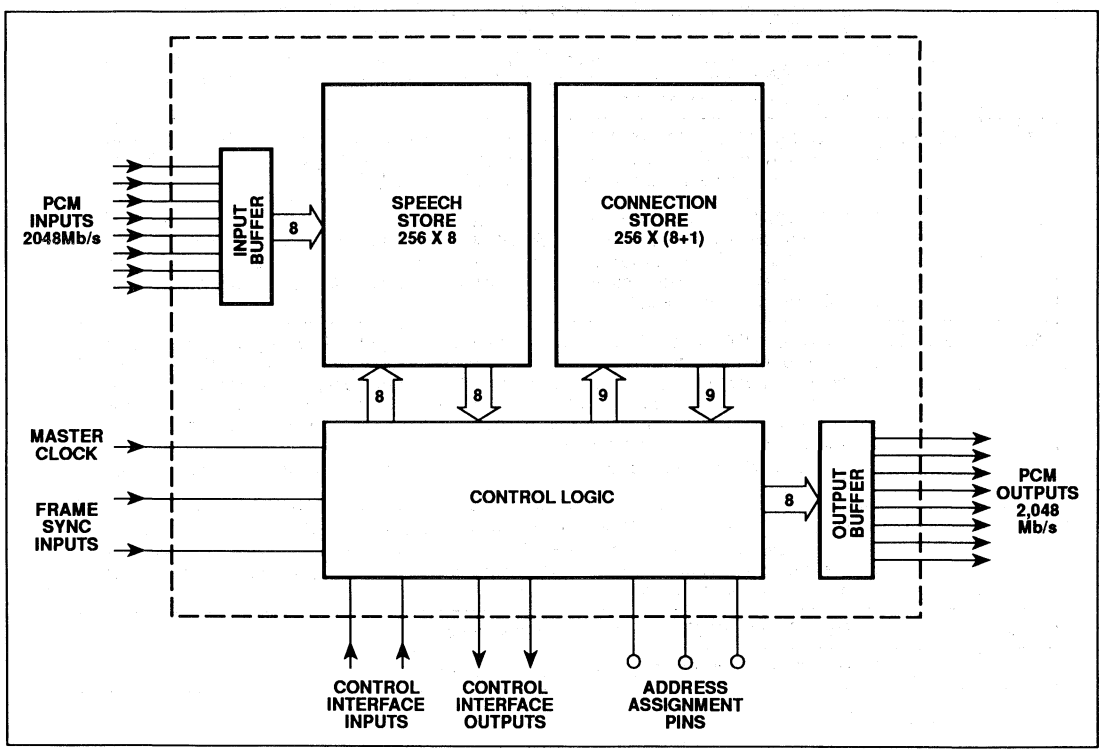
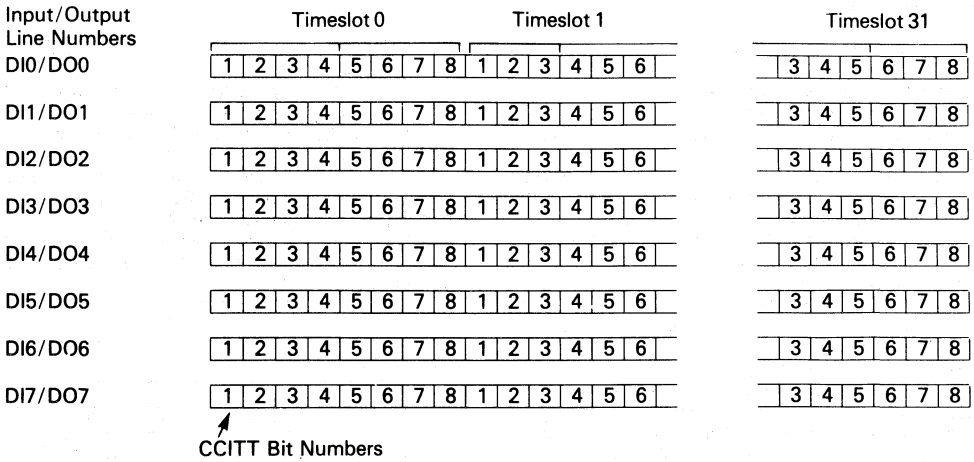


Fig.2 MA8112 block diagram

PIN DESCRIPTION

No.	Name	Function and Description
1 - 8	DI0 - DI7	SPEECH DATA INPUTS. These inputs carry the 256 8-bit channels (containing PCM encoded speech or data) in either serial or parallel format for switching. All eight input lines must be bit and timeslot synchronous. The start and format (i.e. serial or parallel) of an input frame is determined by the input frame synchronisation pulse on Pin 28 ($\overline{FSP1}$). Input and output channels are formatted and numbered as shown in Fig. 3 and the input channel timing is shown in Fig. 4.
10 - 17	DO7 - DO0	SPEECH DATA OUTPUTS. These outputs carry the 256 8-bit channels (containing PCM encoded speech or data) in either serial or parallel format after switching. All eight output lines are bit and timeslot synchronous. The timing of the output frame relative to the input frame is determined by the input to Pin 9 (FSP2). These outputs are open-drain type and should be tied externally to V_{DD} using 1Kohm resistors.
9 28	$\overline{FSP2}$ $\overline{FSP1}$	FRAME SYNC PULSE INPUTS. A frame sync pulse input on $\overline{FSP1}$ provides a frame datum for the incoming data (on both the speech and control inputs) and indicates the active edges of the system clock. In addition the duration of the sync pulse low period determines the speech data input and output formats (i.e. serial or parallel) as shown in Table 1. The $\overline{FSP2}$ input is used to define the start of the output frame. If no frame sync pulse is provided on $\overline{FSP2}$, the output frame will automatically start 21 bits after $\overline{FSP1}$ (mode 1), and will be timed by the negative clock edges alternate to those used for clocking the input frame.
22 - 24	P3 - P1	ADDRESS ASSIGNMENT PINS. These pins are each hardwired to V_{DD} or V_{SS} in order to assign a unique address for up to eight DSMs in a matrix. This allows several DSMs to share the same control interface lines (CI0, CI1 and CO0, CO1).
21, 25	CI0, CI1	CONTROL INTERFACE INPUTS. These are serial control inputs into which all instructions and data regarding the addressing of the DSM, routing of the PCM inputs and outputs and channel insertion and extraction are entered. CI1 is the control instruction input. 8-bit words entered on CI1 correspond to, and control the 8-bit words entered synchronously on CI0, the control data input.
18, 19	CO0, CO1	CONTROL INTERFACE OUTPUTS. These are serial outputs which respond to the words received on the control interface inputs. There is a fixed response time of 21 bit periods between a control interface input word and the corresponding control interface output word. The control instruction output CO1 carries 8-bit words which refer to the words carried on the control data output CI0. These outputs are used to extract data from either the speech or connection memories. CO0 and CO1 are open drain outputs and should be tied high externally using 1Kohm resistors.
26	CLK	MASTER CLOCK INPUT. This input requires a 4.096 MHz TTL level clock. All input signals are strobed on alternate falling clock edges (the active edge is assigned by the position of the input frame sync pulse $\overline{FSP1}$). All output data is clocked out on the opposite alternate negative edges of the clock.
20	V_{SS}	NEGATIVE POWER SUPPLY PIN. Connect to 0v.
27	V_{DD}	POSITIVE POWER SUPPLY PIN. Connect to +5v.

SERIAL DATA FORMAT



PARALLEL DATA FORMAT

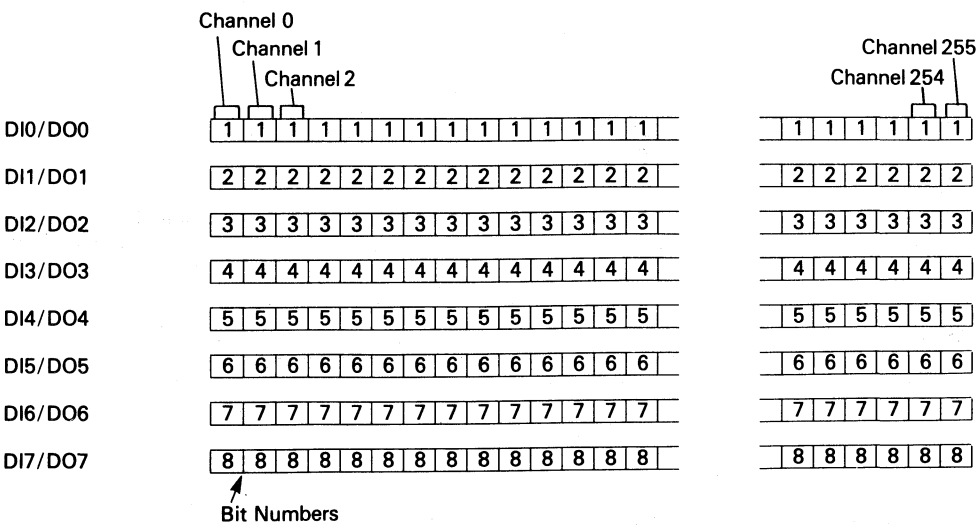


Fig.3 Input and output data formats

INTERFACE DESCRIPTION

TIMING INTERFACE

The following timing information signals must be provided to the MA8112:
(a) A 4.096 MHz master clock on CLK (Pin 26).
(b) An input frame synchronisation pulse on $\overline{FSP1}$ (Pin 28). This pulse must repeat every 125μs (i.e. every 512 master clock periods).
(c) (Optional). An output frame synchronisation pulse on $\overline{FSP2}$ (Pin 9) which repeats every 125μs (512 master clock periods). If this is not provided, the MA8112 will default to assuming a start time for the output frame 21 bit periods after $\overline{FSP1}$.

The master clock is used to strobe all data into and out of the DSM. Data is clocked in on the speech data inputs (DI0-7) and the control interface inputs (CI0, CI1) on alternate falling edges of the master clock. The first active edge of the master clock in each frame is assigned by the timing of the input frame sync pulse $\overline{FSP1}$, as shown in Fig. 4.

$\overline{FSP1}$ also indicates a frame datum for the speech data inputs and control interface inputs, thereby allowing an input channel to be identified by its input line and/or input timeslot (Fig.4). The length of the frame sync pulse low period is used to determine the format of the data on the speech data inputs and outputs.

The input and output formats are explained in the Data Interface description.

The input frame sync pulse must repeat every 512 master clock periods to denote the start of each input frame.

The output frame sync allows the start of each output frame to be denoted in the same way as the input frames. If no pulse is provided on $\overline{FSP2}$, then the output frame starts 21 bits after the $\overline{FSP1}$ automatically. As $\overline{FSP2}$ is internally tied high by a resistor, it may be left open circuit.

Zero frame delay is achieved by tying $\overline{FSP2}$ to $\overline{FSP1}$.

The length of the pulse on $\overline{FSP2}$ has no relevance to the operation of the MA8112.

Length of $\overline{FSP1}$ low period (clock periods)	Format
1	Serial In, Serial Out (SISO)
2	Serial In, Parallel Out (SIPO)
3	Parallel In, Serial Out (PISO)
4	Parallel In, Parallel Out (PIPO)

Table 1

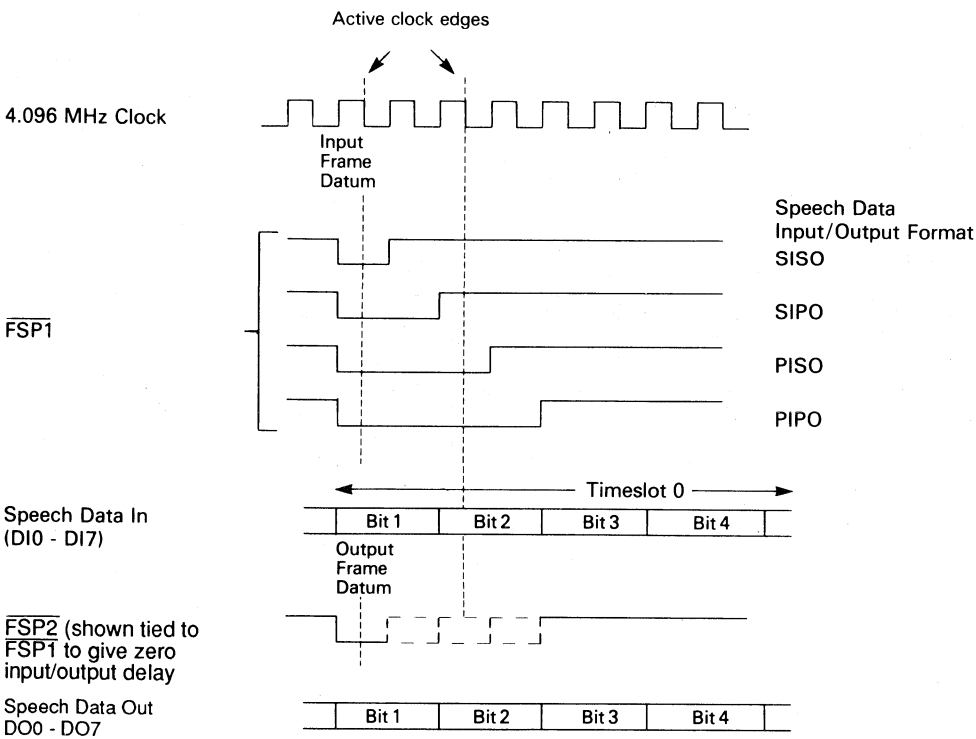


Fig.4(a) DSM timing diagram

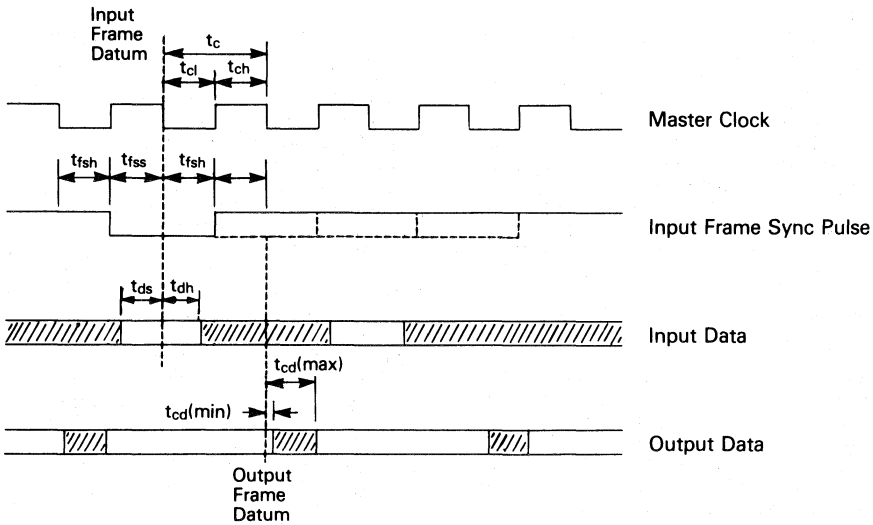


Fig.4(b) Timing information

DATA INTERFACE

The data interface consists of eight input lines DI0-7 and eight output lines DO0-7. Input and output lines carry data at a rate of 2.048Mb/s. This allows 256 8-bit PCM or data channels repeating at a rate of 8 kHz to be switched from the input lines to the output lines.

The data on both the input and output lines is in frames arranged either as 32 serial 8-bit channels on each of the eight input or output lines or, as 256 consecutive 8-bit parallel words on the eight input or output lines. These formats and the numbering scheme for the channels are shown in Fig. 3. Any combination of parallel or serial input or output formats is possible and may be selected by the length of the input frame sync pulse on $\overline{FSP1}$ as explained in the timing interface description.

The input frames are clocked in by alternate negative edges of the master clock. All input lines must be both bit and channel synchronous with each other. The output frames are clocked on the other alternate negative edges to the input frames.

Outputs are open drain type and should be connected via a 1kohm resistor to V_{DD}. This allows several DSMs to be wire-ORed on to the same PCM lines in a matrix configuration.

CONTROL INTERFACE

The control interface consists of two input lines (CI0 and CI1) and two output lines (CO0 and CO1). The operation of the control interface is summarised in Table 2.

Control Interface Inputs

The two input lines receive data in the form of serial 8-bit words at the same rate, and synchronised with the data input lines DI0-DI7. Thus, 32 8-bit words are received per frame.

Each 8-bit control instruction word received on CI1 corresponds to and controls the processing of the 8-bit control data word received in the same timeslot on CI0.

(a) Control Instruction word

The control instruction word format is shown in Fig. 5. Each control instruction word refers to a specific connection memory location (and hence, also to a specific output channel). The connection memory location is addressed by a combination of the timeslot number in which the word is received and the three bits $\overline{A0}$, $\overline{A1}$, $\overline{A2}$ within the control instruction word.

Bits S3, S2 and S1 are used to identify a particular DSM in an array. These bits are compared to the hardwired address assignment pins, P3, P2 and P1. If they match, the control instruction word is intended for this particualr DSM and the DSM will respond accordingly (this is the normal mode in an application using only one DSM).

However, if P3 and S3 match, but either or both S2 and S1 do not match P2 and P1, the DSM will recognise that the message is intended for another DSM which shares the same control interface and speech data lines within a matrix (see Application note). This does not mean that the message is completely ignored. If the message specifies a write operation to a location in another DSM's connection memory, then this DSM will fill its corresponding location with all 1s (including B_{INT}) in order that its speech data output will go open drain on the same output line and timeslot as that of the addressed DSM. This facility allows a DSM matrix to operate particularly efficiently, as several DSMs can be wire-ORed on to the same control lines and when a new connection on to an output channel is made, previous connections from other DSMs are automatically removed.

In the case of a mismatch between S3 and P3, the control instruction word and the control data word are completely ignored as it is assumed that the message is for a DSM with outputs connected to other lines.

The R/$\overline{W}$ bit is the read/write bit. If R/$\overline{W}$ = 0 the operation is a write operation then (subject to an address match on S3, S2 and S1) new data will be written to the appropriate connection memory location. This new data will consist of the 8-bit control data word loaded synchronously on CI0 and the external busy bit, B_{EXT} from the control instruction word. B_{EXT} then becomes the internal busy bit B_{INT}, a ninth bit attached to the eight data bits in each connection memory location. If B_{INT} = 0, then an input channel to output channel connection is made, the location of the word in the connection memory indicating the output channel and the 8 bits at that location (loaded on CI0) indicating the input channel to be switched to the output channel. If B_{INT} = 1, the 8 bits in the connection memory are switched directly to the output channel. This facility allows an idle code to be inserted via the control interface when an output channel is unused.

(b) Control data word

Fig. 5 shows the three possible formats for the control data word loaded synchronously with the control instruction word. If R/$\overline{W}$= 0 and B_{EXT}= 0 in the CIW, one of the first two formats should be used (depending upon whether the speech data format is serial or parallel). If B_{EXT} = 1, the third format should be used, as this is data to be sent to an output channel.

If R/$\overline{W}$ = 1 in the corresponding control instruction word, then the operation is a read and the data on CO0 is irrelevant.

Control Interface Outputs

The two control interface output lines, CO1 and CO0 (Pins 19 and 18) transmit data in the form of serial 8-bit words in response to messages received on the control instruction input CI1. The outputs operate at the same data rate as the inputs (i.e. 32 8-bit words per frame) and are synchronous with each other, each control instruction ouput word transmitted on CO1 corresponding to the accompanying control data output word on CO0.

The delay time from input messages on CI0 and CI1 to the response messages on CO0 and CO1 is 21 bit periods (the outputs are clocked on the other alternate falling edges of the master clock to the inputs). This is a fixed delay and does not vary with the input/output frame delay.

(a) Control instruction output word

The format of the control instruction output word is shown in Fig.6. The information carried on CO1 relates to the data on CO0. As explained earlier, each pair of control interface words on CI0 and CI1 refer to a specific connection memory location, therefore, the control interface output words which form a response will also refer to the same connection memory location.

If the S3 bit in the control instruction word input on CI1 does not match P3, then the input message is ignored and the control interface outputs, CO1 and CO0 will go open-drain (i.e. all 1s) during the response timeslot.

When S3 = P3 on CI1, then the response word on CO1 will always contain a reflection of the connection memory addressing bits $\overline{A0}$, $\overline{A1}$ and $\overline{A2}$ and the R/$\overline{W}$ (read/write) bit on CI1. This information, together with the timeslot during which the output words are transmitted, provides the information on whether the input message was a read or write operation and which connection memory location (and, therefore, output channel) is being referred to. The remaining bits of the control instruction output word and the data contained in the corresponding word on CO0 will depend upon the operation being performed and the contents of the connection memory.

When R/$\overline{W}$ = 0 on CI1 (i.e. a write operation), then the corresponding control data output word on CO0 will reflect the new connection memory contents at the specified location and B_{INT} will, similarly, be reflected on CO1. If the new contents of the connection memory location is all 1s, including B_{INT} (because either the input message was addressed to another DSM in a matrix or because all 1s were specifically written to this location in this DSM) this will be reflected by the control data output CO0 going open-drain during the relevant timeslot. Also the S1, S2 and S3 bits on CO1 will be set to one. If the word on CI1 was specifically addressed to this DSM and the connection memory location contents is not all 1s, then S1, S2 and S3 will reflect the address of this DSM (i.e. P1, P2 and P3). As only one DSM in a matrix can have anything other than all 1s in corresponding connection memory locations (because only one device can be active in a PCM output channel at a time) this arrangement ensures that only this DSM responds with the address in the relevant timeslot.

When R/$\overline{W}$ = 1 on the control instruction word on CI1 (i.e. a read operation) the data input on CI0 is irrelevant. It is not necessary to specify which DSM is to be read from by matching S1 and S2 to P1 and P2 because when used on a matrix, only one of the DSMs with output lines wired together will contain any data other than all 1s in the connection memory location which is to be read. Therefore, only one DSM will respond to the read instruction by transmitting data on CO0 and a reflection of its address on CO1 - other DSMs will go open-drain at the appropriate time. The status of the B_{EXT} bit in the control insruction input word determines whether the read operation refers to reading the word in the connection memory location or reading the PCM output channel associated with this location. If B_{EXT} = 0, the connection memory is read. If B_{EXT} = 1, the output channel word is read - this may be the word from the speech memory addressed by the contents of the connection memory or the word from the connection memory itself, depending upon the status of B_{INT} appended to this location.

(b) Control data output word

The four possible control data output word formats are shown in Fig. 6. Which format is applicable is determined by the information requested, and the format in which this data is stored on chip.

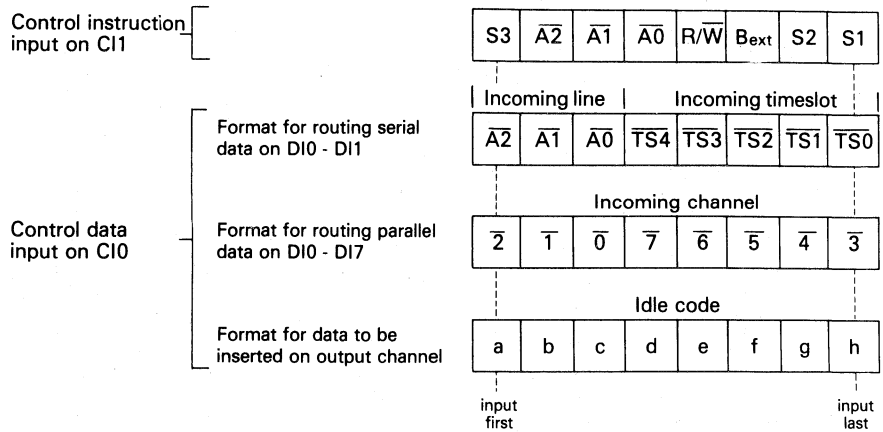


Fig.5 Control interface input message formats

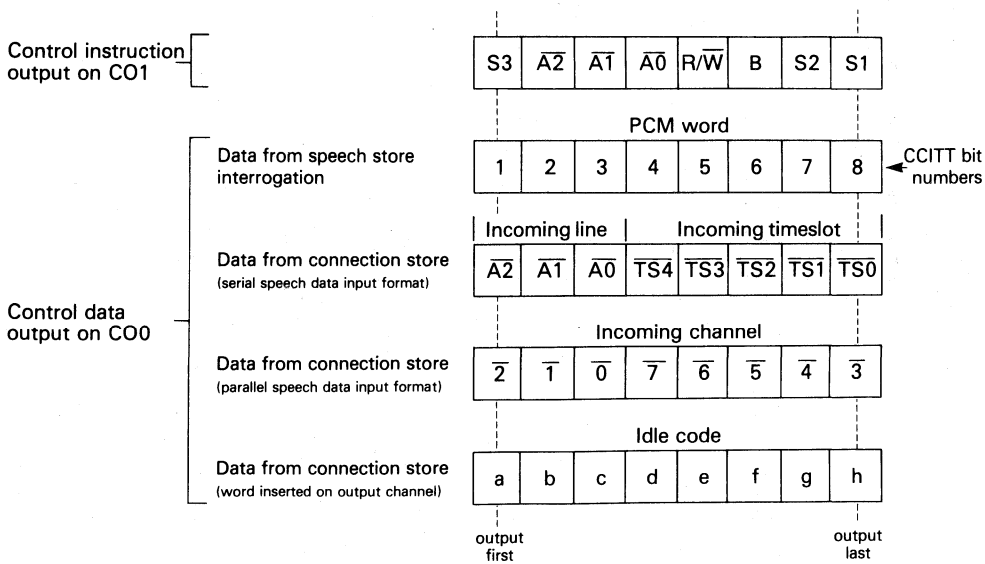


Fig.6 Control interface output message formats

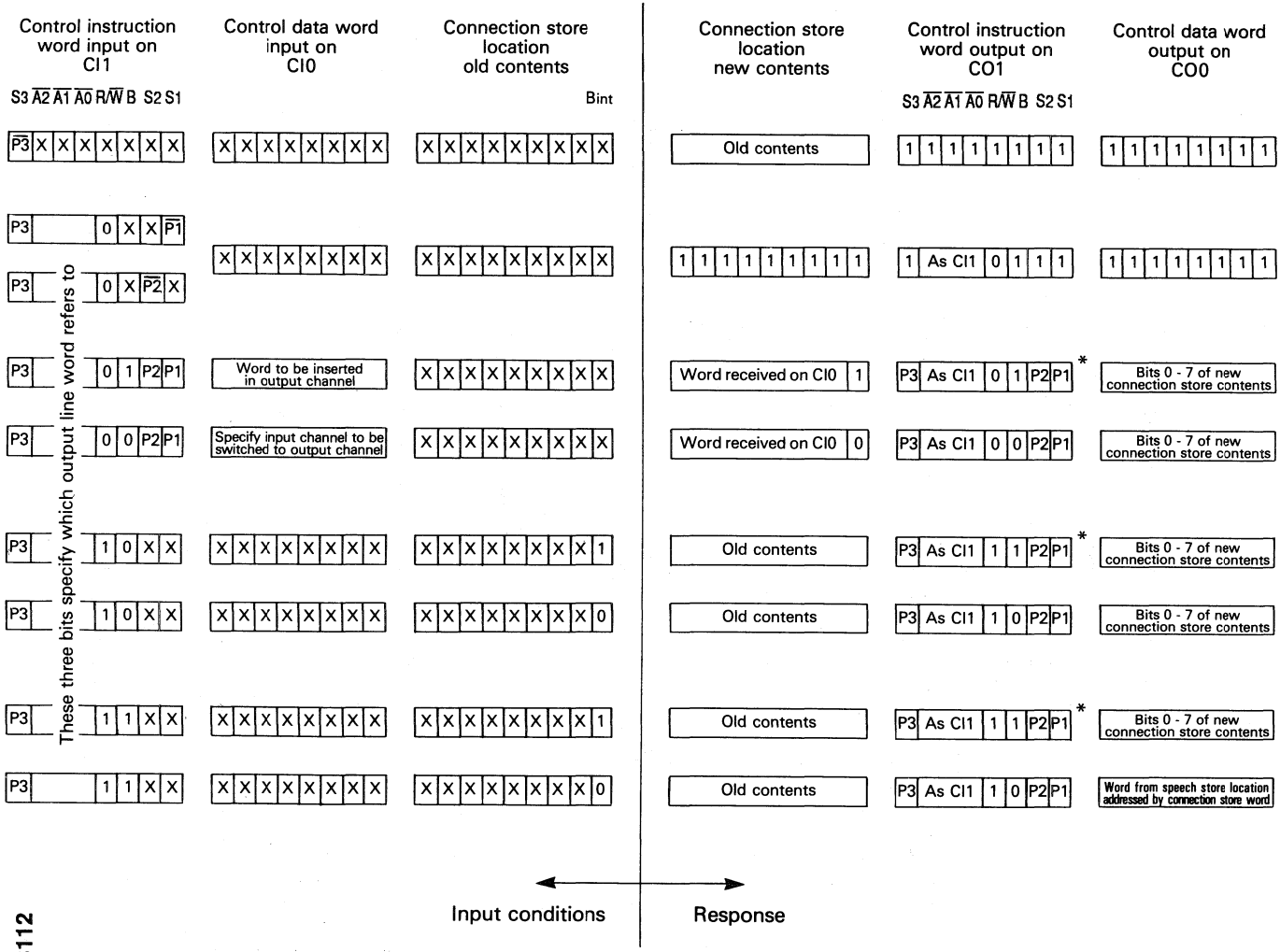


Table 2 Control interface operation

* Except when addressed connection store location contains all 1s. In this case S1, S2, S3 = 1

X = Don't Care

ADDITIONAL NOTES

Channel Numbering

When the DSM is operated in a mixed input/output format mode , i.e. Serial In, Parallel Out, or Parallel In, Serial Out, it is necessary to be able to equate channel numbers.

MSB							LSB
TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0

In serial mode, a channel number is identified by taking the line number and timeslot number and assembling them as follows:

MSB						LSB
TS4	TS3	TS2	TS1	TS0	A2	A0	A1

DSM Internal Delays

There is a fixed minimum internal delay through the DSM for PCM words which is that produced by format conversion and the memory read/write cycle within the DSM. This delay is 21 bit periods (i.e. 42 master clock periods) and is the shortest period in which an input word can be sent to an output channel.

If the $\overline{FSP2}$ input is left open circuit, then the fixed delay will be 21 bit periods, but if an output frame sync pulse is provided, the fixed delay will be up to 255 bit periods longer, dependent upon the timing of the $\overline{FSP2}$ relative to $\overline{FSP1}$.

The total delay for any particular channel is equal to this fixed delay plus a variable delay determined by the time spent in the speech memory waiting for the relevant output timeslot.

The overall delay is given by the following relation:

PIPO format:

$$D = F + (N - M) \text{ for } N \geqslant M$$

$$D = F + 256 + (N - M) \text{ for } N < M$$

SISO format:

$$D = F + \left(\text{INT}\frac{N}{8} - \text{INT}\frac{M}{8}\right) \times 8 \text{ for } N \geqslant M$$

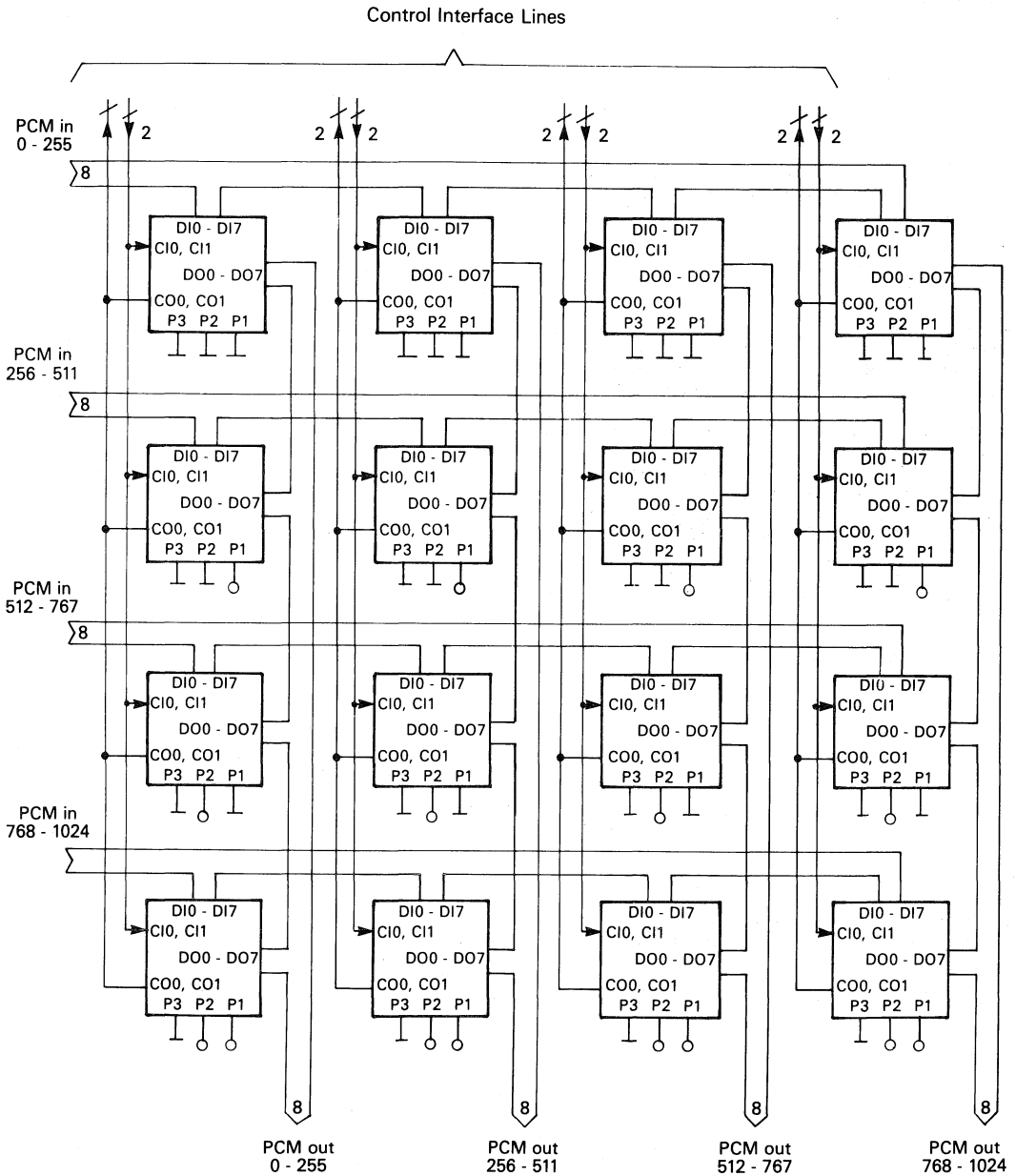
$$D = F + 256 + \left(\text{INT}\frac{N}{8} - \text{INT}\frac{M}{8}\right) \times 8 \text{ for } N < M$$

where

D = total delay in bit periods (488ns)
F = fixed delay in bit periods (21 bits or specified by FSP2)
M = Incoming channel number
N = Outgoing channel number

APPLICATIONS INFORMATION

Fig. 7 shows how a 1024-channel DSM matrix can be constructed, providing four times the switching capacity of a single DSM. Note that the control interface allows DSMs connected to the same PCM output lines to be wire-ORed to common interface lines without additional logic.



ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
Supply voltage V_{DD}	−0.3	6.5	V
Voltage on any pin	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Operating temperature	0	70	°C
Storage temperature	−55	+125	°C

* Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

D C ELECTRICAL CHARACTERISTICS at V_{DD} = 5v ±%, Ambient temperature = 25°C

	Symbol	Min	Typ	Max	Units	Conditions
High level input voltage	V_{IH}	2.0			V	
Low level input voltage	V_{IL}	−0.3		0.8	V	
Supply current			<5	10	mA	CLK = 4.096 MHz
Input current	I_{IH}			10	μA	$V_{IH} = V_{DD} + 0.3v$
	I_{IL}			10	μA	−0.3v V_{IL} 0.8v except Pin 9
				100	μA	−0.3v V_{IL} 0.8v Pin 9
Low level output voltage	V_{OL}			0.4	V	Rpu = 1Kohm
High level output voltage	V_{OH}	2.8			V	Rpu = 1Kohm
Input capacitance	C_i			5	pF	
Output capacitance	C_o			5	pF	

A C ELECTRICAL CHARACTERISTICS† at V_{DD} = 5v ±5%, Ambient temperature 0 to +70°C

	Symbol	Min	Typ	Max	Units	Conditions
Master clock period	t_c	240	244	2400	nS	
Master clock low period	t_{cl}	80			nS	
Master clock high period	t_{ch}	80			nS	
Frame sync period	t_f	512		512		Master clock periods
Frame sync set up time	t_{fss}	50			nS	
Frame sync hold time	t_{fsh}	50			nS	
Input data set up time	t_{ds}	50			nS	
Input data hold time	t_{dh}	50			nS	
Master clock to output delay	t_{cd}	5		150	nS	

† See Fig. 4(b)

DS3132-1.0

MS2002

DIGITAL SWITCH MODULE (DSM)

The MS2002 is an N-channel MOS LSI integrated circuit providing digital switching for 256 channels in PCM systems. The device is unidirectional in operation and is capable of switching data from any incoming channel to any outgoing channel. Input data can be either serial or parallel. The DSM is designed to be easily expandable to provide a greater switching capacity.

FEATURES

- Single 5V Supply
- TTL Compatible
- Interfaces Directly with European Standard CCITT 32 Channel Format
- 256 Input/256 Output Channels
- Serial or Parallel Inputs and Outputs
- Open Drain Outputs for Easy Expansion
- One System Clock and One Frame Synchronisation Pulse

APPLICATION

- Circuit Switched PCM or Data Systems

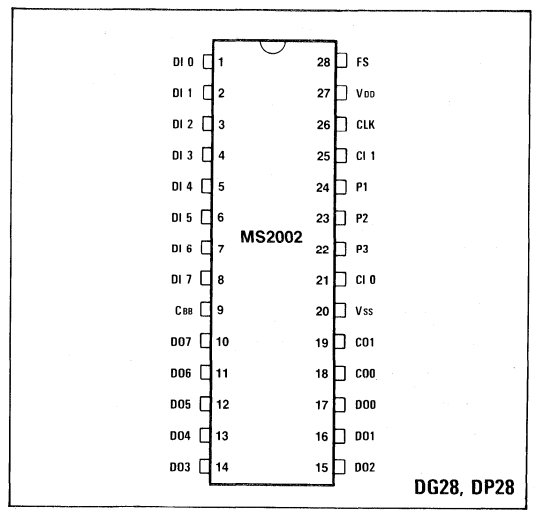


Fig.1 Pin connections - top view

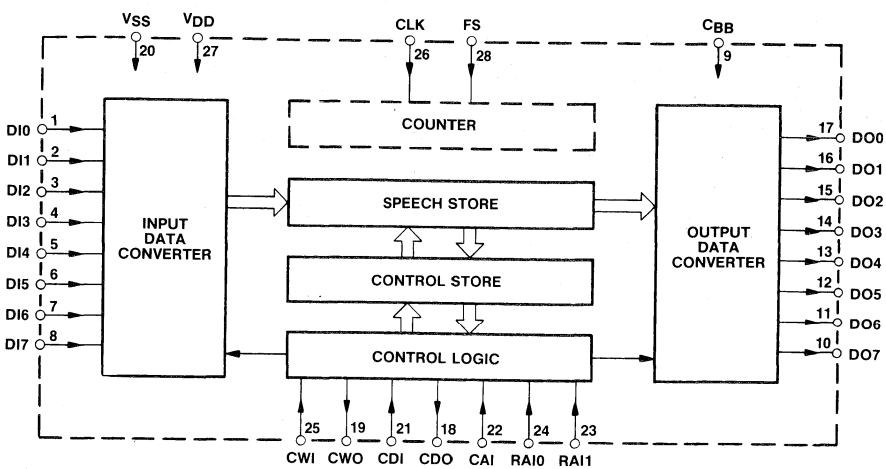


Fig.2 Functional block diagram

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
DI0-DI7	1-8	**Data In 0 to 7 (Digital Inputs).** These are the inputs for the 256 incoming channels. The data presented at these pins is latched on the alternate negative edges of the CLK clock to those used by DO0-7. Frame synchronisation for these pins is established by the FS pulse.
C_{BB}	9	**Bias Decoupling Capacitor (Decoupling Node).** A bias decoupling capacitor of 1000pF should be connected between this pin and V_{SS}.
DO7-DO0	10-17	**Data Out 0 to 7 (Digital Pull-down Outputs).** These are the output pins for the 256 outgoing channels. Data is output at these pins on the alternate negative edges of the CLK clock to those used by DI0-7. Frame synchronisation for these pins is established by the FS pulse.
CDO	18	**Control Data Out (Digital Pull-down Output).** This pin outputs control data bytes. Bit synchronisation and frame synchronisation are stablished by the CLK and FS signal in a similar way as on the DO0-7 pins. It is high impedance for time slots which are not in use for control instructions. It is also high impedance for time slots corresponding to the 'write all ones' instruction. During time slots corresponding to other control instructions this pin outputs either the inverse of the 8 least significant bits at a control store location or the data at the speech store location selected by these 8 bits.
CWO	19	**Control Word Out (Digital Pull-down Output).** This pin outputs control word bytes. Bit synchronisation and frame synchronisation are established by the CLK and FS signals in a similar way as on the DO0-7 pins. It is high impedance for time slots which are not in use for control instructions and for time slots corresponding to the instruction 'write all ones'. During time slots corresponding to other instructions this pin outputs 4 bits which are the same as on CWI and 4 bits which indicate to the status of the chip.
V_{SS}	20	**Negative Supply Voltage (Power Input).** 0V.
CDI	21	**Control Data In (Digital Input).** The control data bytes are latched into the chip at this pin. Bit synchronisation and frame synchronisation are established by the CLK and FS signals in a similar way as on the DI0-7 pins. The bits in the input control data byte are inverted and written into the control store by the instruction 'write CWM bit and CI bits'.
CAI	22	**Column Address In (Digital Input).** This pin defines the column position of a chip in the control array.
RAI 1,0	23, 24	**Row Address In 1, 0 (Digital Inputs).** These pins defined the row position of a chip in the control array.
CWI	25	**Control Word In (Digital Input).** Control word bytes are latched into the chip at this pin. Bit synchronisation and frame synchronisation are established by the CLK and FS in a similar way as on the DI0-7 pins. The bits in the input control word byte control whether reads or writes occur, allow different chips in a control array to be addressed, and control whether connections are busy or free.
CLK	26	**Clock (Digital Input).** The system clock, nominally 4.096MHz, is input at this pin. It is used with the pulse on FS to establish bit synchronisation on the data and control inputs and outputs.
V_{DD}	27	**Positive Supply Voltage (Power Input).** 5V.
FS	28	**Frame Synchronisation (Digital Input).** The negative pulse input at this pin is used with the CLK clock to establish the frame synchronisation on the data and control inputs and outputs. The duration of the pulse determines the modes of the data input and output converters.

Duration (clock periods)	Data Inputs	Data Outputs
1	Serial	Serial
2	Serial	Parallel
3	Parallel	Serial
4	Parallel	Parallel

FUNCTIONAL DESCRIPTION

The MS2002 is a 256 channel non-blocking digital switch capable of connecting all 256 incoming channels to all 256 outgoing channels in any desired order. Alternatively, selected input channels may be broadcast to any number of output channels. Each output channel may, however, receive from only one input channel at a time.

Speech data is input to the device via 8 lines (DI0-7) that can accept 8 bit data in either serial or parallel format at a 2.048Mb/s rate. Speech data is output is via a further 8 lines which may be set independently of the input lines to give serial or parallel format data.

Call routings are held in an on-chip control store in the form of a nine bit word for each outgoing speech channel, bit nine (CM) indicating the busy status of the channel (0 = busy). In the case of a busy outgoing channel the remaining eight bits denote the number of the input channel to be connected to that outgoing channel.

The contents of the control store can be modified, and the speech or control store interrogated, via control messages received over the control inputs (CWI, CDI). Data generated by interrogation of either the control or speech store appears on the two control outputs (CWO, CDO).

Frame Formats

Serial inputs and outputs on the DSM are numbered in the same way as the CCITT 2048kbit/s PCM link (see Fig.3). This applies to both data and control information.

If the DSM is configured for parallel data on the data inputs or outputs then the Parallel Channels are numbered from 0 to 255 (see Fig.4).

These are different frame alignments for inputs and outputs (see Fig.5) The outgoing alignment is delayed by 21 bit periods with respect to the incoming alignment.

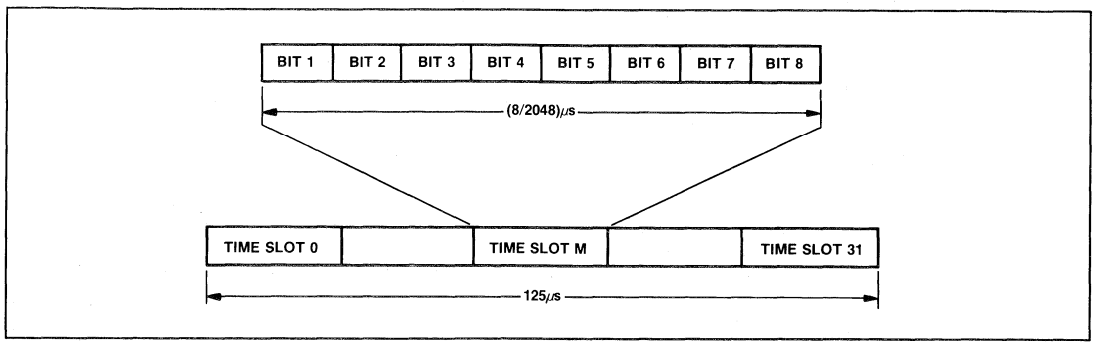


Fig.3 Serial format

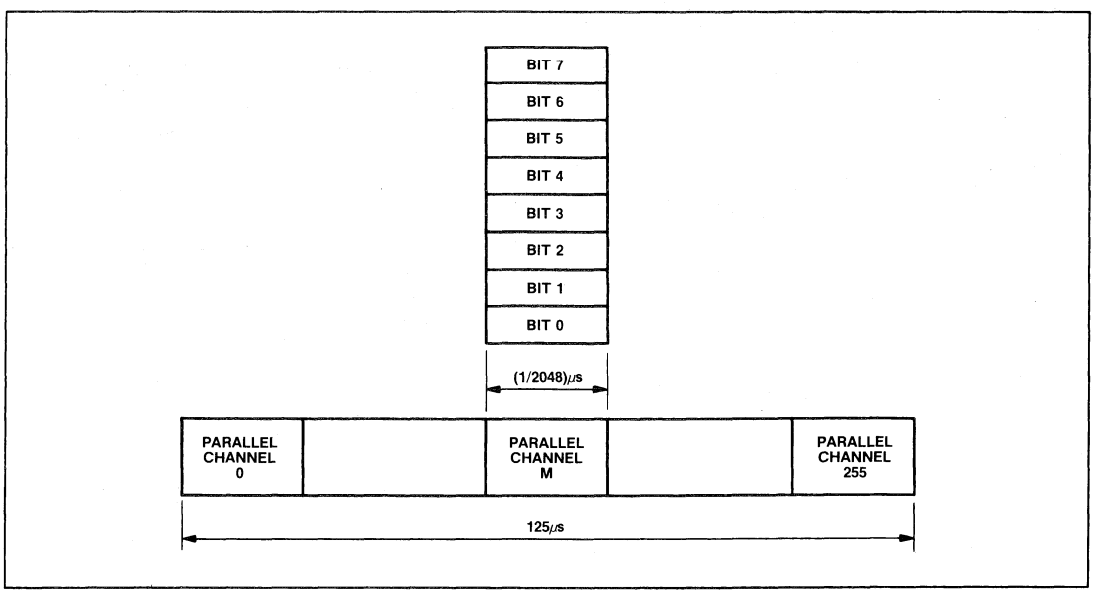


Fig.4 Parallel format

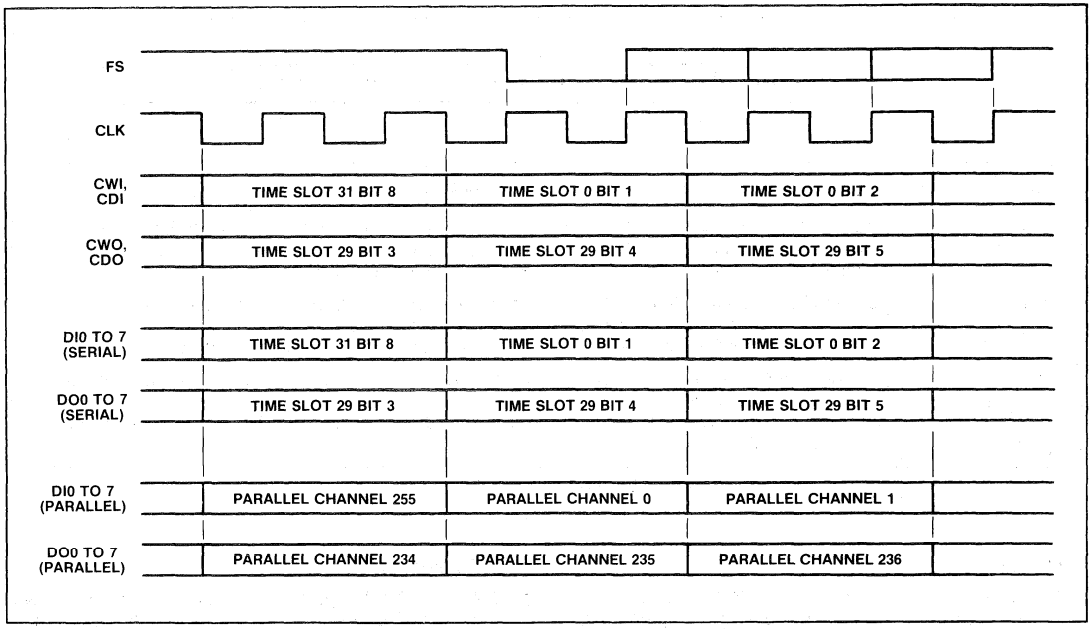


Fig.5 Timing - nominal

Speech Store

The Speech Store has 256 addresses each containing 8 bits. These addresses are associated with the Data In pins. If the DSM is configured for serial input then these addresses are organised by input pin and Time Slot (see Fig.6). If the MS2002 is configured for parallel input then these addresses correspond to the input Parallel Channels.

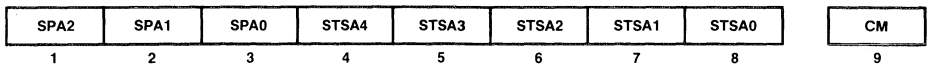
Control Store

The Control Store has 256 addresses each containing 9 bits. These addresses are associated with the Data Out pins in the same way that the Speech Store is associated with the Data In pins (see Fig.6).

Fig.7 shows how the 9 bits at each Control Store address are organised.

Store Address (Speech or Control)	Serial Time Slot Address (Input or Output)	Serial Pin Address (Input or Outut)	Parallel Channel (Input or Output)
0	0	0	0
1	0	1	1
2	0	2	2
3	0	3	3
4	0	4	4
5	0	5	5
6	0	6	6
7	0	7	7
8	1	0	8
9	1	1	9
.	.	.	.
.	.	.	.
.	.	.	.
254	31	6	254
255	31	7	255

Fig.6 Relationship between inputs, outputs and stores



Bit	Name	Description
1-3	SPA2-0	**Speech Pin Address 2 to 0.** These bits are the Serial Pin Address in the Speech Store (see Fig.6). When used with the Speech Time Slot Address bits a unique Speech Store address is specified. This address corresponds to a Parallel Channel if parallel input is used.
4-8	STSA4-0	**Speech Time Slot Address 4 to 0.** These bits are the Serial Time Slot Address in the Speech Store (see Fig.6). When used with the Speech Pin Address bits a unique Speech Store address is specified. This address corresponds to a Parallel Channel if parallel input is used.
9	CM	**Connection Mode.** This bit determines whether the connection is busy or free and also helps to control reads from the DSM. If this bit is 0 then the connection is busy. If it is 1 then the connection is free. Fig.10 shows how this bit affects reads.

Fig.7 Bits at each control store address

Switching Delay

The switching function of the MS2002 is achieved by storing the incoming speech channels sequentially in the 256 x 8 speech store (after conversion to parallel format) and then sending them to the output channels in the order specified by the control store.

The delay encountered by each channel consists of a fixed delay, determined by the format conversion circuitry and the memory read/write cycle time, and a variable delay. The fixed delay is the 21 bits shown in Fig.5.

The variable delay is controlled by the sequence of writing to the speech store and reading from it under the direction of the control store. Input data is written to the speech store addresses in turn (see Fig.6). Output data is obtained by reading the control store addresses in turn and then reading the output data from the specified speech store address.

This means that when an input serial time slot is switched to the same output serial time slot then the delay is 21 bits if the Data In number is less than or equal to the Data Out number. The delay is 21 bits plus one frame if the Data In number is greater than the Data Out number.

The Control Array

The MS2002 is designed to be controlled in an array of two columns and four rows (see Fig.8). This control array need not be fully implemented. For example, a 512 channel switch can be constructed from two columns and two rows. If a large switch is required then control arrays can be arranged in a variety of architectures.

Each MS2002 in the Control Array uses the same control signals. These contain 32 Time Slots of 8 bits each.

The Time Slot used by an instruction is the Time Slot Address in the Control Store (see Fig.6). The format of the bits used for control, which is the same for both input and output, is shown in Figs. 9 and 10.

Instructions to the array are decoded according to the column in the array. The column whose Column Address pin matches the Column Address Bit on Control Word In responds to the instruction.

The write instruction can set up a connection from any one of the 1024 addresses in the Speech Stores of the 4 MS2002s in a row of the control array. The read instructions allow busy connections to be identified and monitored.

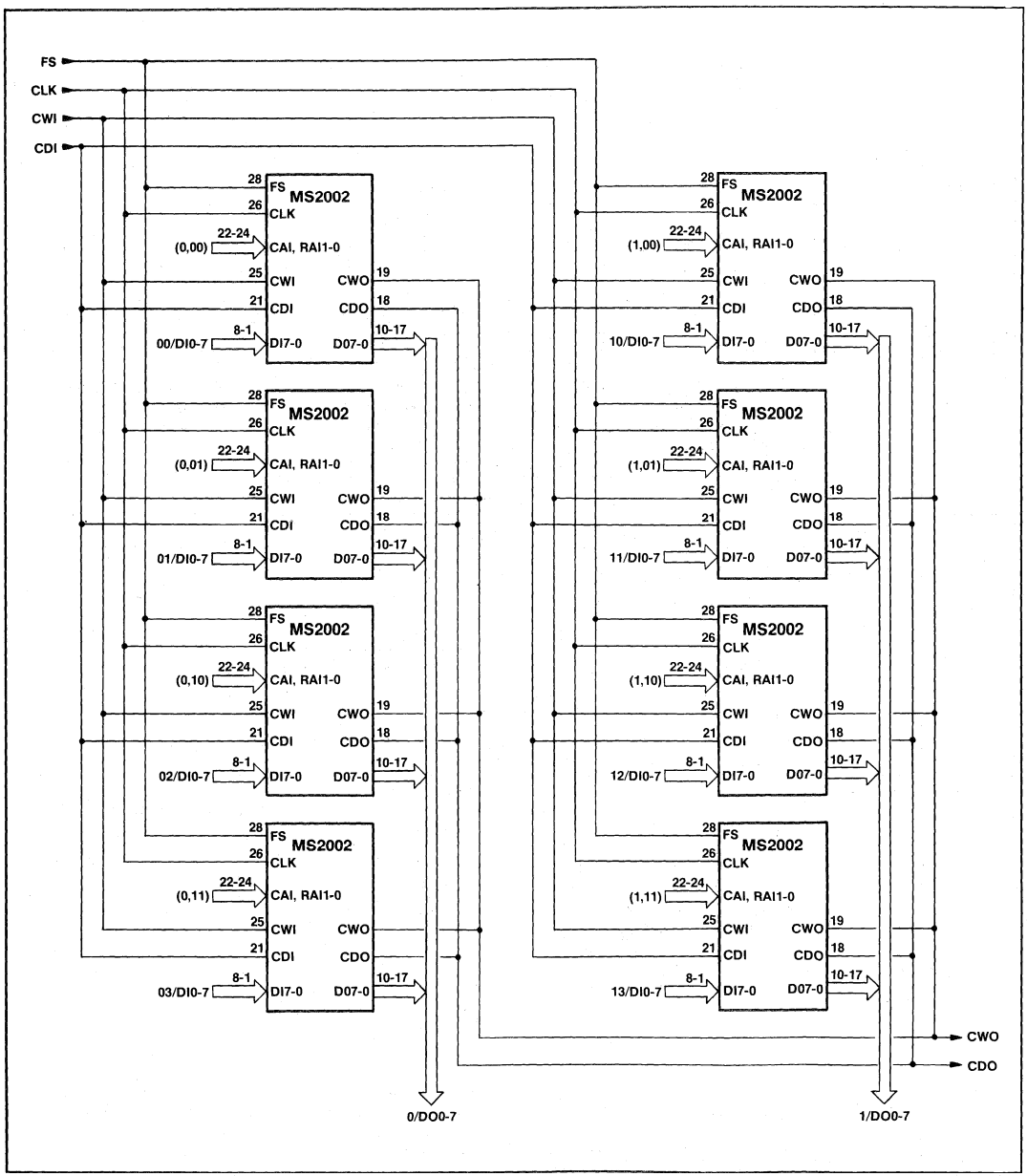
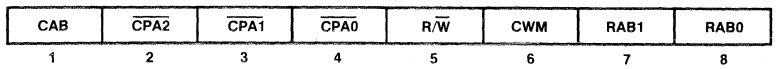


Fig.8 The control array



Bit	Name		Description
1	CAB		**Column Address Bit**
		In	If this bit matches the Column Address pin then the device will be written to or read from. If it does not match then Control Word Out and Control Data Out are high impedance during the output Time Slot.
		Out	This bit is set to the Column Address after a read from the Speech Store or after a write to the Control Store other than all 1's. It goes high impedance in all other cases.
2-4	$\overline{CPA2\text{-}0}$		**Control Pin Address 2 to 0**
		In	These bits are the Serial Pin Address at the Control Store (see Fig.6). The Time Slot Address is determined by the Time Slot on the Control Word In pin (see Fig.3). The Serial Pin and Time Slot Addresses define a unique address in the Control Store which corresponds to a Parallel channel if parallel output is used (Fig.6).
		Out	These bits are the same as those on the Time Slot on Control Word In if the Column Addresses match. They are high impedance otherwise.
5	R/$\overline{W}$		**Read or Write**
		In	This bit has no effect unless the Column Addresses match. If they do match then a read or write occurs depending whether it is 1 or 0 6 (see Fig.10).
		Out	This bit is the same as on the Time Slot on Control Word In if the Column Addresses match. It is high impedance otherwise.
6	CWM		**Control Word Mode**
		In	This bit has no effect unless the Column Addresses match. It can replace the Connection Mode bit at the Control Store address during writes or it can help to direct reads if the Column Addresses do match (see Fig.10).
		Out	This bit is the same as the Connection Mode bit at the Control Store address if the Column Addresses match. It is high impedance otherwise.
7-8	RAB1-0		**Row Address Bit 1 and 0**
		In	These bits have no effect unless the Column Addresses match. They help to control writes if the Column Addresses do match (see Fig.10). The Row Address Bits ensure that only one of the four MS2002s in a row of the Control Array can be active on the Data Out pins at any time.
		Out	These bits are set to the Row Address after certain operations and are high impedance otherwise. See Fig.11 for details.

Fig.9 Control word bits (both input and output) **NB** *The Control Word Out bits are open-drain pulldown outputs. This means that output high is the same as output high impedance.*

Writing

The R/$\overline{W}$ bit of the instruction on Control Word In must be low for a write (see Fig.9). This causes a write to all MS2002s in the selected column. This write is to the same address in the Control Store of each MS2002. The Time Slot part of the address is the same as the Time Slot used by the instruction on Control Word In and Control Data In. The Pin part of the address is selected by the Control Pin Address bits in the Control Word (see Figs. 6 and 9).

The MS2002s in the selected column whose Row Address pins do not match the Row Address Bits in the Control Word have 1s written to the 9 bits at the address in the Control Store. This ensures that none of these MS2002s are in conflict with the remaining MS2002 on the Data Out pins. They also go high impedance during the control Time Slot on Control Word Out and Control Data Out (except for the $\overline{CPA2\text{-}0}$ and R/$\overline{W}$ bits which are the same for all MS2002s - see Fig.11).

The MS2002 whose Row Address matches responds differently to the instruction. The Control Word Mode bit and the Control Data bits are written into the address in the Control Store. This allows a connection to be established onto the Data Out pins. This MS2002 also responds differently on the control outputs unless the 9 bits written to the Control Store are all 1s. Fig.11 shows how the MS2002 acknowledges the instruction.

Reading

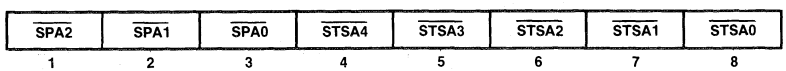
A read is performed automatically to acknowledge a write as mentioned in the previous section. It is also possible to read from the array independently of writing. The column selected by the Column Address Bit of the instruction will be read when the R/$\overline{W}$ bit is high. Reads are associated with an address in the Control Store. Either the bits at that address or the bits in the Speech Store selected by them will be read. This provides information about calls in progress or about the status of a connection.

The Row Address Bits in the instruction are ignored during reads. Each MS2002 which has one or more 0s at the selected address in its Control Store will respond to a read instruction. To avoid possible confusion about which MS2002 in a row is being read the array should be initialised by writing to it.

Two types of read are possible, depending on the input Control Word Mode bit. If this bit is 0 then a Type-0 Read occurs. Type-0 Reads are always from the Control Store. If the Control Word Mode bit is 1 then a Type-1 Read occurs. Type-1 Reads are from the Control Store or from the Speech Store depending on whether the Connection Mode bit at the Control Store address is 1 or 0 (free or busy). Fig.11 shows how the reads affect the control outputs.

Type-0 Reads indicate whether or not the connection through the array to the Data Out pins is busy or free. If it is busy then it identifies the MS2002 and Speech Store Address in it which sources the connection.

Type-1 Reads tap a connection to the Data Out pins if it is busy. They also indicate the MS2002 which sources the connection but cannot specify the origin within the MS2002. If there is no busy connection assocaited with the Control Store address the a Type-1 Read indicates the presence of 0s at the Control Store address.



Bit	Name	Description	
1-3	$\overline{\text{SPA2-0}}$	**Speech Pin Address 2 to 0**	
		In	These bits replace the Speech Pin Address bits at the Control Store address during a write if the Row Addresses match (see Fig.10). **NB** These bits are inverted with respect to those at the Control Store address, i.e. if these are all 0 then they refer to Speech Pin Address 7 (see Fig.6).
		Out	These bits are high impedance unless a read or write occurs. During a read these bits can contain the Speech Pin Address bits at the Control Store address or bits 1 to 3 of the Speech Store location addressed by the bits at the Control Store address (see Fig.11). **NB** These bits are inverted with respect to the contents of the Control Store but not with respect to the contents of the Speech Store.
4-8	$\overline{\text{STSA4-0}}$	**Speech Time Slot Address 4 to 0**	
		In	These bits replace the Speech Time Slot Address bits at the Control Store address during a write if the Row Addresses match (see Fig.11). **NB** These bits are inverted with respect to those at the Control Store address, i.e. if these are all 0 then they refer to Speech Time Slot Address 31 (see Fig.6).
		Out	These bits are high impedance unless a read or write occurs. During a read these bits can contain the Speech Time Slot Address bits at the Control Store address or bits 4 to 8 of the Speech Store location addressed by the bits at the Control Store address (see Fig.11). **NB** These bits are inverted with respect to the contents of the Control Store but not with respect to the contents of the Speech Store.

Fig.10 Control data bits (both input and output) **NB** *The Control Data Out bits are open-drain pulldown outputs. This means that output high is the same as output high impedance.*

Control Word In			CM Bit at Control Store Address	Instruction	Control Word Out			Control Data Out
R/W Bit	CWM Bit	Row Address			CAB Bit	CWM Bit	RAB1-0 Bits	
0	X	Matches	X	Write CWM bit + CDI bits	CAP Pin *†	Control Store Bit 9 (CM)†	RAP1-0 Pins *†	Control Store Bits 1-8†
0	X	Does Not Match	X	Write all 1s	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	X	Read Type 0	CAP Pin *†	Control Store Bit 9 (CM)	RAP1-0 Pins *	Control Store Bits 1-8
1	1	X	1	Read Type 1	High Impedance	Control Store Bit 9 (CM) = 1	High Impedance	Control Store Bits 1-8
1	1	X	0		CAP Pin†	Control Store Bit 9 (CM) = 0	RAP1-0 Pins	Speech Store Bits 1-8

Fig.11 The control operations

NB It is assumed that the Column Address matches, in which case $\overline{CPA2\text{-}0}$ and R/$\overline{W}$ are the same as on the control Time Slot on Control Word In. The control outputs are high impedance during the control Time Slot if the Column Address does not match.
* High Impedance if data at Control Store Address is all 1's.
† Should be identical to the data on the control inputs.

ELECTRICAL CHARACTERISTICS

Test Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Characteristic	Symbol	Value			Units
		Min.	Typ.(1)	Max.	
Positive supply voltage	V_{DD}	4.75	5.0	5.25	V
Ambient temperature	T_{amb}	0		70	°C
Input low voltage	V_{IL}	0	0.4	0.8	V
Input high voltage	V_{IH}	2.0	2.4	V_{CC}	V
Output pullup resistor	R_{OP}	1000			Ω
Output load capacitor	C_{OP}	50			pF
Bias decoupling capacitor	C_{BB}	900	1000	1100	pF

Digital Static Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Supply current	I_{DD}		40	60	mA	Unloaded
Input leakage current	I_{LI}			50	μA	$0 < V < V_{CC}$
Output low voltage	V_{OL}	0		0.4	V	I_{OL} (Sink) = 2mA
Output low voltage	V_{OL}	0		2.0	V	I_{OL} (Sink) = 8mA
Output leakage current	I_{LO}			50	μA	$0 < V < V_{CC}$

Analog Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Pin capacitance	C_P		8	10	nF	Unloaded

Digital Switching Characteristics - Clock (see Fig.12)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Clock period	t_{CP}	225	244	275	ns	
Clock rise time	t_{CR}		50		ns	
Clock high period	t_{CH}	82			ns	
Clock fall time	t_{CF}		50		ns	
Clock low period	t_{CL}	82			ns	

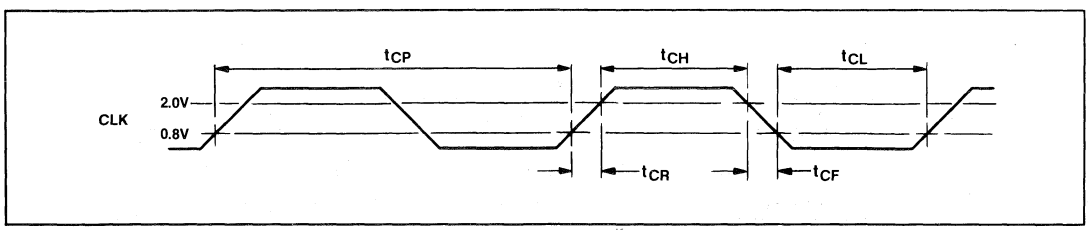


Fig.12 Timing - clock

Digital Switching Characteristics - Frame Synchronisation (see Figs.5 and 13)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Frame Synchronisation falling hold time	t_{FFH}	90	122		ns	
Frame synchronisation falling setup time	t_{FFS}	60	122		ns	
Frame synchronsiation rising hold time	t_{FRH}	90	122		ns	
Frame synchronisation rising setup time	t_{FFS}	60	122		ns	

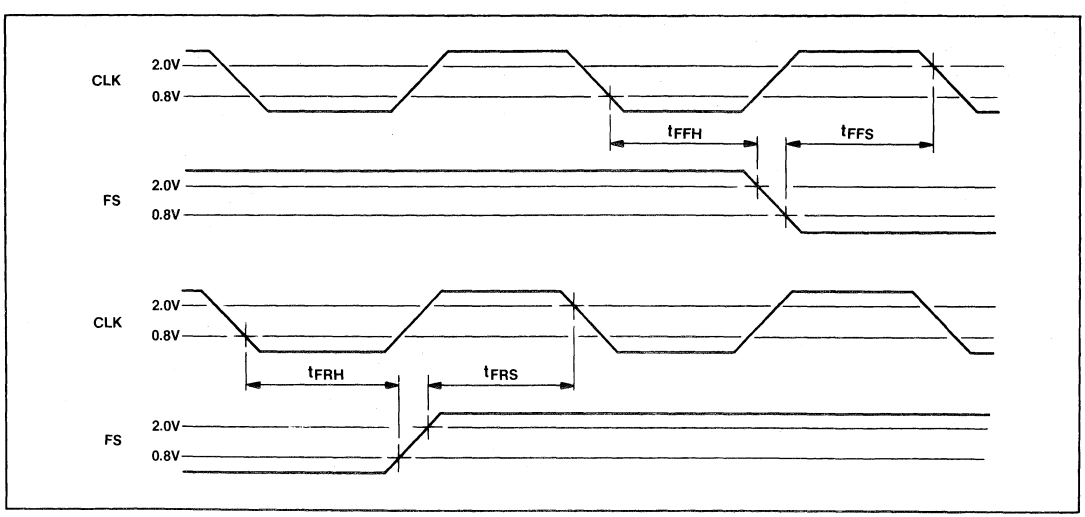


Fig.13 Timing - falling and rising edges of frame synchronisation

Digital Switching Characteristics - Data and Control Inputs and Outputs (see Figs.5 and 14)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Input setup time	t_{IS}	60	244		ns	
Input hold time	t_{IH}	90	244		ns	
Output hold time	t_{OH}	5			ns	
Output delay	t_{OD}			150	ns	

NOTE
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

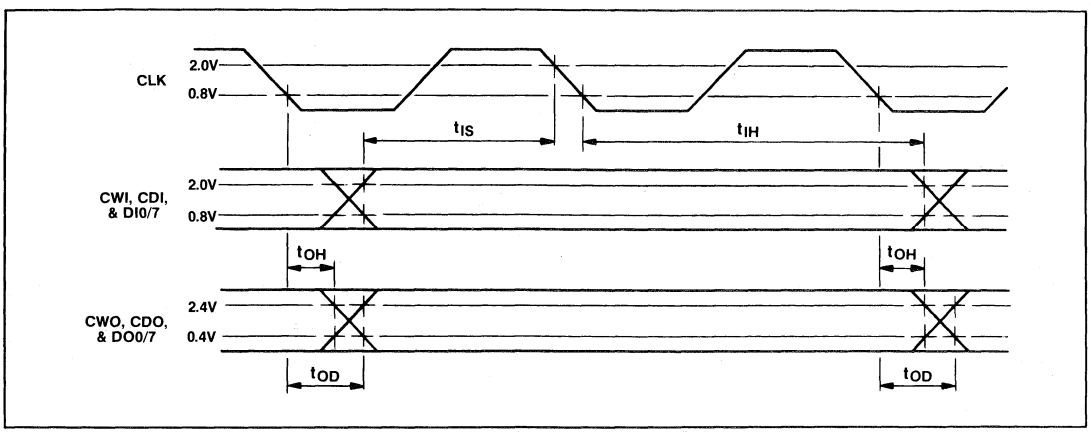


Fig.14 Timing - data and control inputs and outputs

ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Positive supply voltage, V_{DD}	-0.5V to +7V
Storage tempertaure, T_{ST}	-65°C to +150°C
Digital input voltage, V_{ID}	-0.3V to V_{DD} +0.3V
Clamp current (Sink or Source), I_C	50mA
Package power dissipation, P_P	800mW

DS3133-1.0

MV3506 A-LAW FILTER/CODEC
MV3507 μ-LAW FILTER/CODEC
MV3507A μ-LAW FILTER/CODEC WITH A/B SIGNALLING
MV3508 A-LAW FILTER/CODEC WITH OPTIONAL SQUELCH
MV3509 μ-LAW FILTER/CODEC WITH OPTIONAL SQUELCH

These devices are silicon gate CMOS Companding Encoder/Decoder integrated circuits designed to implement the per channel voice frequency Codecs used in PCM systems. They contain the band-limiting filters and the analog to digital conversion circuits that conform to the desired transfer characteristic. The MV3506 and MV3508 provide the European A-Law companding and the MV3507, MV3507A and MV3509 provide the North American μ-Law companding characteristic. The MV3508 and MV3509 have programmable squelch circuitry to reduce idle channel noise. The MV3507A provides for A/B bit signalling.

These circuits provide the interface between the analog signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of ±5V.

FEATURES

- Low Power CMOS 80mW (Operating) 10mW (Standby)
- Meets or Exceeds AT & T3, and CCITT G.711, G.712 and G.733 Specifications
- Input Analog Filter Eliminates Need for External Anti-aliasing Prefilter
- Uncommitted Input and Output Op. Amps for Programming Gain
- Output Op. Amp Provides ±3.1V into a 1200 Ohms Load or can be Switched Off for Reduced Power (70mW)
- Encoder has Dual-speed Auto-zero Loop for Fast Acquisition on Power-up
- Low Absolute Group Delay = 410 microseconds at 1kHz

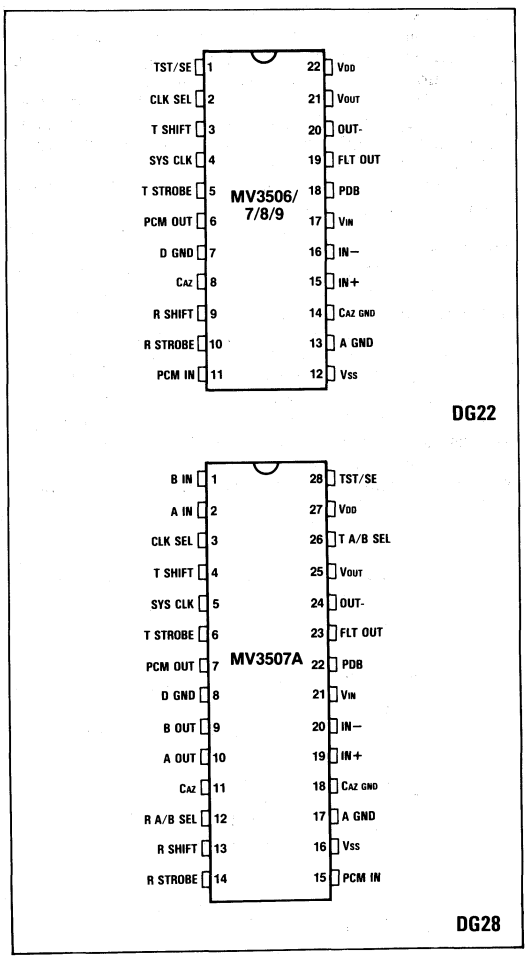


Fig.1 Pin connections - top view

FUNCTIONAL DESCRIPTION

Fig.2 shows the simplified block diagram of the devices. They contain independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps.

Transmit Section

Input analog signals first enter the chip at the uncommitted op.amp. terminals (IN + and IN- pins). This allows for the gain in the system to be trimmed. From the V_{IN} pin the signal enters a second-order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 34dB (typically) at 256kHz and 44dB (typically) at 512kHz.

The signal next enters the transmit filter, which is a fifth-order low-pass filter clocked at 256kHz, followed by a third-order high-pass filter clocked at 64kHz. The resulting bandpass characteristics meet the CCITT specifications G.711, G.712 and G.733. Some representative attenuations are better than 26dB from 0 to 60Hz and better than 35dB from 4.6kHz to 100kHz.

The output of the transmit filter is sampled at the analog to digital encoder by a capacitor array at the sampling rate of 8kHz. The successive approximation conversion process requires about 72μsec.

The 8-bit PCM data is clocked out by the transmit shift clock which can vary from 64kHz to 2.048MHz in 8kHz steps (see Figs. 3 and 4). A switched capacitor dual-speed, auto-zero loop using a small non-critical external capacitor (0.1μF) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

Included in the circuitry of the MV3507 is 'All Zero' code suppression so that negative input signal values between decision values numbers 127 and 128 are encoded as 00000010. This prevents loss of repeater synchronisation by DS1 (T1) line clock recovery circuitry as there are never more than 15 consecutive zeros.

An additional feature of the MV3506/7 and 7A is a special circuit to eliminate any transmitted idle channel noise during quiet periods. When the input of these chips is such that for 250ms the only code words generated were +0, -0, +1 or -1, the output word will be a +0. The steady +0 state prevents alternating sign bits or LSB from toggling and thus results in a quieter signal at the decoder. Upon detection of a different value, the output resumes normal operation resetting the 250ms timer. This feature is a form of idle Channel Noise 'Squelch' or 'Crosstalk Suppression'. It is of particular importance in the MV3506 A-Law version because the A-Law transfer characteristic has 'mid-riser' bias which enhances low level signals from crosstalk.

Receive Section

A receive shift clock, variable between the frequencies of 64kHz and 2.048MHz clocks the PCM data into the input buffer register once every sampling period (see Figs.5 and 6). A charge proportional to the received PCM data word appears on the decoder capacitor array of the digital to analog converter. A sample and hold circuit, initialised to zro by a narrow pulse at the beginning of each sampling period, integrates the charge and holds it for the rest of the sampling period.

The receive filter, consisting of a switched-capacitor fifth-order low-pass filter clocked at 256kHz, smooths the sampled and held signal. It also performs the loss equalisation to compensate for the sin(x)/x distortion due to the sampling.

The filter output (FLT OUT pin) is available for driving electronic hybrids directly as long as the impedance is greater than 20kΩ. When used in this fashion the low impedance output amp can be switched off for a considerable saving in power consumption. When it is required to drive a 600Ω load the output amp allows gain trimming as well as impedance matching.

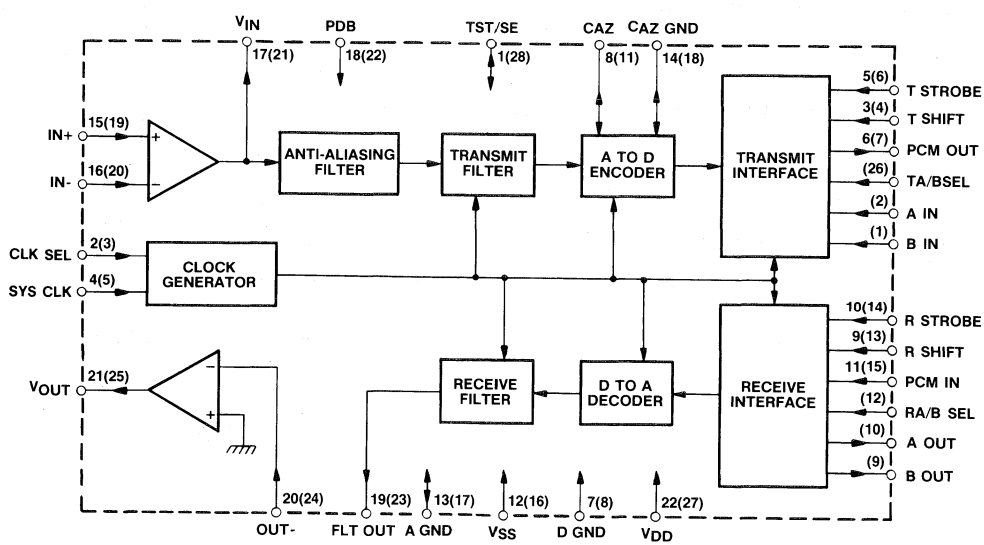


Fig.2 Functional block diagram (pin numbers for the MV3507A are in brackets)

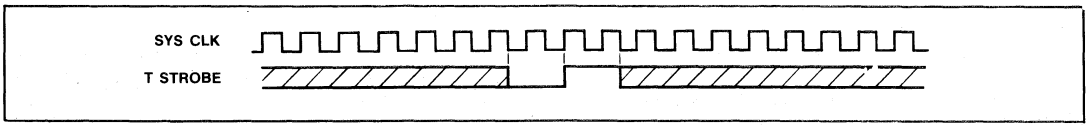


Fig.3 Transmit strobe alignment

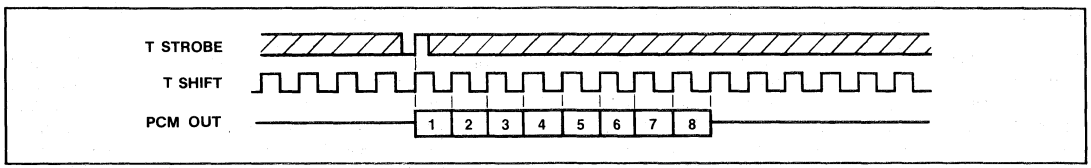


Fig.4 Transmit alignment

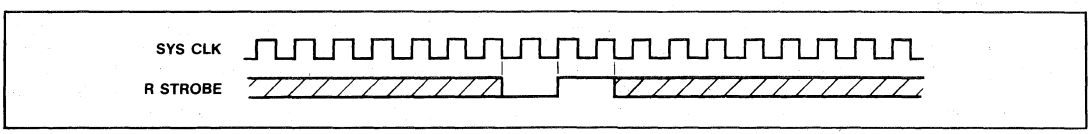


Fig.5 Receive strobe alignment

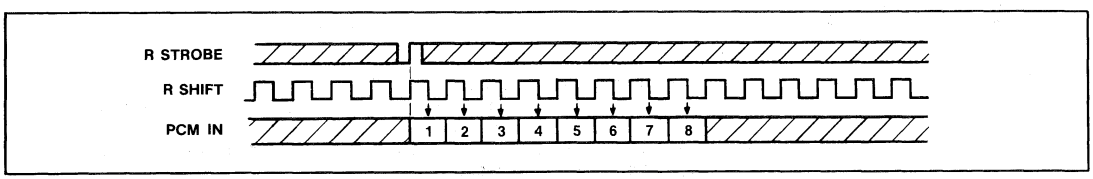


Fig.6 Receive alignment

Timing Requirements

The internal design of the devices paid careful attention to the timing requirements of various systems. In North America, central office and channel bank designs often follow the American Telephone and Telegraph Company's T1 (DS1) Carrier PCM format to multiplex 24 voice channels at a data rate of 1.544Mb/s. PABX designs, on the other hand, may use their own multiplexing formats with different data rates. Nevertheless, in digital telephone designs, Codecs may be used in a non-multiplexed form with data rate as low as 64kbit/s. The μ-Law Codecs fulfil these requirements.

In Europe, telephone exchange and channel bank designs often follow the CCITT carrier PCM format to multiplex 30 telephony channels at a data rate of 2.048Mbit/s. The A-Law Codecs are designed for this market and will also handle PABX and digital telephone applications.

The timing format chosen for the devices allows operation in both multiplexed or non-multiplexed form with data rates variable from 64kbit/s to 2.048Mbit/s. Use of separate internal clocks for filters and for shifting of PCM input/output data allows for this variation.

The devices do not require that the 8kHz transmit and receive sampling strobes be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+ve) edges of the strobe, forcing the PCM output into its high impedance state after the 8th bit is shifted out. This allows the width of the strobe signal to vary as long as its repetition rate is 8kHz and the transmit and receive shift clocks are synchronised to it.

System Clock

The basic timing is provided by the system clock which is divided down internally to provide the various filter clocks and the timing for the conversions. The transmit and receive strobes and clocks must be locked to this clock so that the PCM data matches the sample rates.

Signalling in 7-Law Systems

In μ-Law systems there is a requirement for signalling information to be carried in the bit stream with the coded analog data. This coding scheme is sometimes called 7$\frac{1}{2}$ bit rather than 8 bit because the LSB in every 6th frame is replaced by a signalling bit. This is referred to as A/B signalling and if a signalling frame carries the 'A' bit, then 6 frames later the LSB will carry the 'B' bit. To meet this requirement, the MV3507A is available in a 28-pin package.

Signalling Interface

In the AT&T T1 carrier PCM format (DS1) an A/B signalling method conveys channel information. It might include the on-or-off hook status of the channel, dial pulsing (10 or 20 pulses per second), loop closure, ring ground etc, depending on the application. Two signalling conditions (A and B) per channel, giving four possible signalling states per channel are repeated every 12 frames (1.5msec). The A signalling condition is sent on bit 8 of all 24 channels in frame 6 and the B signalling condition is sent in frame 12. In each frame, the 193rd bit (the S bit) performs the terminal framing function and serves to identify frames 6 and 12.

The MV3507A in a 28-pin package is designed to simplify the signalling interface. For example, the A/B select input pins are transition sensitive. The transmit A/B select pin selects the A signal input on a positive transition and the B signal input on the negative transition. Internally, the device synchronises the A/B select input with the strobe signal. As a result, a common A/B select signal can be used for all 24 transmit channels in the channel bank. The A and B signalling bits are sent in the frame following the frame in which the A/B select input makes the transition. Therefore the A/B select input must go positive in the beginning of frame 5 and negative in the beginning of frame 11.

The decoder uses a similar scheme for receiving the A and B signalling bits, with one difference. They are latched to the respective outputs in the same frame in which A/B select input makes a transition. Therefore, the receive A/B select input must go high at the beginning of frame 6 and go low at the beginning of frame 12. In the T1 (DS1) carrier system, 24 voice channels are multiplexed to form the transmit and receive PCM highway, 8 data bits from each channel plus a framing bit called the S bit form a 193 bit frame. Since each channel is sampled 8000 times per second, the resultant data rate is 1.544Mbit/s. Within the channel bank the transmit and receive channels of a Codec can occupy the same time slot for synchronous operation or they can be independent of each other for asynchronous operation. Asynchronous operation helps minimise switching delays through the system. Since the timing interface for the coder and decoder sections are independent of each other in the MV3507A, it can be operated in either manner.

In the CCITT carrier system 30 voice channels and 2 framing and signalling channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel. Since each channel is sampled 8000 times per second, the resultant data rate is 2.048Mbit/s.

PIN DESCRIPTIONS

Symbol	Pin No.		Pin name and description
	3506/7/8/9	3507A	
TST/SE	1	28	**Test/Squelch Enable (Internal Connection/Digital Input).** This pin is an internal test connection on the MV3506, MV3507 and MV3507A, and it is the squelch enable input on the MV3508 and MV3509. On the MV3506/7/7A it should be left unconnected or connected to the A GND pin via a capacitor for normal operation. On the MV3508/9 it should be tied high to enable the squelch feature and it should be left unconnected otherwise.
CLK SEL	2	3	**Clock Select (Three Level Input).** This pin selects the proper divide ratios for a 256kHz, 1.544MHz or 2.048MHz system clock. The pin is tied to V_{DD} (+5V) for 2.048MHz operation, to D GND (0V) for 256kHz operation, and to V_{SS} (-5V) for 1.544MHz operation.
T SHIFT	3	4	**Transmit Shift Clock (Digital Input).** This TTL compatible input shifts PCM data out of the coder on the positive going edges after receiving a positive edge on the T STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
SYS CLK	4	5	**System Clock (Digital Input).** This pin is a TTL compatible input for either a 256kHz, 1.544MHz or a 2.048MHz clock that is divided down to provide the filter clocks. The status of the CLK SEL pin must correspond to the provided clock frequency.
T STROBE	5	6	**Transmit Strobe (Digital Input with Pull-up).** This TTL compatible pulse input (typically 8kHz) is used for analog sampling and initiating the PCM output from the coder. It must be synchronised with the T SHIFT and SYS CLK clocks with its positive going edges occurring after the falling edges of these clocks. The width of this signal is not critical. An internal bit counter generates the necessary timing for PCM output.
PCM OUT	6	7	**PCM Out (Pull-down Output).** This is a LS TTL compatible open-drain output. It is active only during transmission of PCM output for 8-bit periods of the T SHIFT clock signal following positive edge on the T STROBE input. Data is clocked out by the positive edge on the T SHIFT clock into one 510Ω pull-up per system plus 2 LS TTL inputs.
D GND	7	8	**Digital Ground (Power Input).** 0V.
C_{AZ}	8	11	**Auto Zero Capacitor (Reference Node).** A capacitor of 0.1μF (±20%) should be connected between this pin and $C_{AZ\,GND}$ for coder auto zero operation. The sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
R SHIFT	9	13	**Receive Shift Clock (Digital Input).** This TTL compatible input shifts PCM data into the decoder on the negative going edges after receiving a positive edge on the R STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.

PIN DESCRIPTIONS (continued)

Symbol	Pin No.		Pin name and description
	3506/7/8/9	3507A	
R STROBE	10	14	**Receive Strobe (Digital Input with Pull-up).** This TTL compatible pulse input (typically 8kHz) initiates clocking of PCM input data into the decoder. It must be synchronised with the R SHIFT and SYS CLK clocks with its positive going edges occurring after the falling edges of these clocks. The width of the signal is not critical. An internal bit counter generates necessary timing for PCM input.
PCM IN	11	15	**PCM In (Digital Input).** This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of the R SHIFT clock.
V_{SS}	12	16	**Negative Supply (Power Input).** -5V.
A GND	13	17	**Analog Ground (Reference Node).** This is the ground reference node for analog signals.
$C_{AZ\ GND}$	14	18	**Auto Zero Capacitor Ground (Reference Node).** A capacitor of 0.1μF ($\pm$20%) should be connected between this pin and C_{AZ} for coder auto zero operation. The sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
IN +, IN-	15,16	19,20	**In Positive and Negative (Analog Voltage Inputs).** These are the differential inputs of a high input impedance op amp whose output is connected to the V_{IN} pin. These three pins allow the user complete control over the input stage so that it can be connected as a fixed gain amplifier, as an amplifier with adjustable gain, or as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel.
V_{IN}	17	21	**Input Voltage (Analog High-impedance Voltage Output).** This is the output of a high input impedance op amp whose differential inputs are the IN + and IN- pins. This node feeds the rest of the analog input section.
PDB	18	22	**Power Down Bar (Digital Input with Pull-up).** This TTL compatible input, when held low, puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.
FLT OUT	19	23	**Filter Out (Analog High-impedance Voltage Output).** This is the output of the low pass filter which represents the recreated analog signal from the received PCM data words. The filter sample frequency of 256kHz is down 37dB at this point. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance. It should not be loaded by less than 20kΩ.
OUT-	20	24	**Out Negative (Analog Voltage Input).** This is the inverting input of the uncommitted output amplifier stage, which has its non-inverting input connected internally to ground and its output connected to V_{OUT}. The signal at the FLT OUT pin can be connected to this pin to realise a low output impedance with unity, increased or reduced gain. This allows easy calibration of the receive channel. If OUT- is connected directly to V_{SS} then the op amp will be powered down, reducing power consumption by 10mW typically.
V_{OUT}	21	25	**Output Voltage (Analog Voltage Output).** This is the output of the uncommitted output amplifier stage, which has its inverting input connected to the OUT- pin and its non-inverting input connected internally to ground. The signal at the FLT OUT pin can be connected to OUT- to realise a low output impedance with unity, increased or reduced gain. This allows easy calibration of the receive channel. The V_{OUT} pin has the capability of driving 0dBm into a 600Ω load (see Fig.4).
V_{DD}	22	27	**Positive Supply (Power Input).** 5V.
B IN, A IN	-	1,2	**B IN and A IN (Digital Inputs with Pull-ups).** These are the TTL compatible inputs for the A and B signalling bits for transmission. The signalling bits are sent in the bit 8 position of the PCM word in the frame following the frame in which the T-A/B SEL input makes a transition.
B OUT,A OUT	-	9,10	**B OUT and A OUT (Digital CMOS Outputs).** These are the outputs for the received A and B signalling bits. The signalling bits received in the PCM input word are latched to the respective outputs in the same frame in which the Receive A/B select (R-A/B SEL) input makes a transition. A-bits are latched on a positive transition and B-bits are latched on a negative transition.

PIN DESCRIPTIONS (continued)

Symbol	Pin No.		Pin name and description
	3506/7/8/9	3507A	
R-A/B SEL	-	12	**Receive A or B Select (Digital Input with Pull-up).** This is the TTL compatible input which causes A and B signalling bits to b at the A OUT and B OUT pins. The signalling bits received in the PCM input word are latched to the respective outputs in the same frame in which this input makes a transition. A-bits are latched on a positive transition and B-bits are latched on a negative transition. A common select input can be used for all channels in a multiplex operation.
T-A/B SEL	-	26	**Transmit A or B Select (Digital Input with Pull-up).** This is the TTL compatible input which causes the transmission of A and B signalling bits input at the A IN and B IN pins. The signalling bits are sent in the bit 8 position of the PCM word in the frame following the frame in which the T-A/B SEL input makes a transition. A common A/B select input can be used for all channels in a multiplex operation, since it is synchronised to the T STROBE input in each device.

ELECTRICAL CHARACTERISTICS

Test conditions - Voltages are with respect to digital ground (V_{DGND})

Characteristic	Symbol	Value			Units
		Min.	Typ.(1)	Max.	
Digital supply voltage	V_{DD}	4.75	5	5.25	V
Negative supply voltage	V_{SS}	-5.25	-5	-4.75	V
Analog ground voltage	V_{AGND}	-0.1	0	0.1	V
Ambient temperature	V_{AMB}	0		70	°C
Input low voltage - digital inputs	V_{IL}	0	0.4	0.8	V
Input high voltage - digital inputs	V_{IH}	2.0	2.4	V_{DD}	V
System clock frequency					
CLK SEL tied to V_{DD}	f_S	2047.90	2048	2048.10	kHz
CLK SEL tied to D GND		255.99	256	256.01	
CLK SEL tied to V_{SS}		1549.92	1544	1544.08	
Capacitive loading - digital outputs	C_{LD}	0		100	pF
Pull-up resistance for PCM OUT pin	R_{PU}	510			Ω
Analog input voltage	V_{IA}	V_{AGND} -3.1		V_{AGND} +3.1	V
Capacitive loading - analog outputs	C_{LA}			50	pF
Resistive loading - V_{OUT} pin	R_{VOUT}	1200			Ω
Resistive loading - V_{IN} pin	R_{VIN}	10			kΩ
Resistive loading - FLT OUT pin	$R_{RLT\ OUT}$	20			kΩ

Power Supply Requirements - V_{DD} = 5V, V_{SS} = -5V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Power dissipation - normal	P_N		80	110	mW	Unloaded
Power dissipation - without output amp.	P_{WA}		70		mW	Unloaded
Power dissipation - standby	P_S		10	20	mW	Unloaded

Static Characteristics - Voltages are with respect to digital ground (V_{DGND})

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Pin capacitance	C_{PIN}		7	15	pF	
Input leakage current	I_{IL}			1	μA	$0 < V < V_{DD}$
Input source current - inputs with pull-ups	I_{IS}			600	μA	$0 < V < V_{DD}$
Output high voltage	V_{OH}	2.4		V_{DD}	V	I_{OH} (Source) = 40μA
Output low voltage	V_{OL}	0		0.4	V	I_{OL} (Sink) = 1.6mA
Output leakage current	I_{OL}			10	μA	$0 < V < V_{DD}$
Analog input resistance	R_{IA}	100			kΩ	
Analog output voltage	V_{OA}	V_{AGND} -3.1		V_{AGND} +3.1	V	

Digital Switching Characteristics - System Clock (see Fig.7)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
System clock rise time	t_{SR}		50		ns	
System clock high period	t_{SH}	0.4/f_S		0.6/f_S	s	
System clock fall time	t_{SF}		50		ns	
System clock low period	t_{SL}	0.4/f_S		0.6/f_S	s	

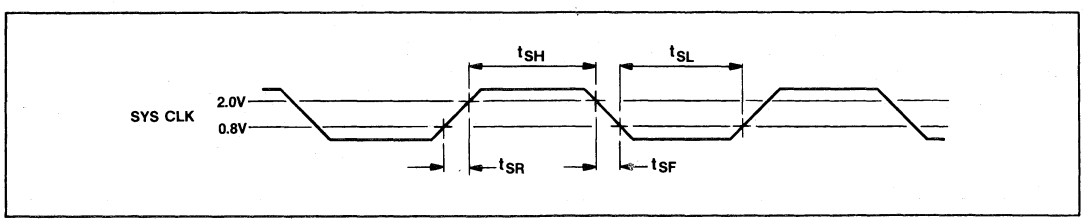


Fig.7 Timing - system clock

Digital Switching Characteristics - Receive Strobe and Clock (see Figs. 8 and 9)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Receive strobe frequency	f_{RS}	7.99996	8	8.00004	kHz	Phase-locked with system clock
Receive strobe falling set-up time	t_{RSFS}	120			ns	
Receive strobe early jitter	t_{RSEJ}			200	ns	
Receive strobe late jitter	t_{RSLJ}			100	ns	
Receive strobe falling hold time	t_{RSFH}	220			ns	
Receive clock frequency	f_{RC}	63.9997		2048.01	kHz	Phase-locked with receive strobe
Receive clock rise time	t_{RCR}			100	ns	
Receive clock high period	t_{RCH}	0.4/f_{RC}		0.6/f_{RC}	s	
Receive clock fall time	t_{RCF}			100	ns	
Receive clock low period	t_{RCL}	0.4/f_{RC}		0.6/f_{RC}	s	
Receive clock early jitter	t_{RCEJ}			200	ns	
Receive clock late jitter	t_{RSLJ}			100	ns	

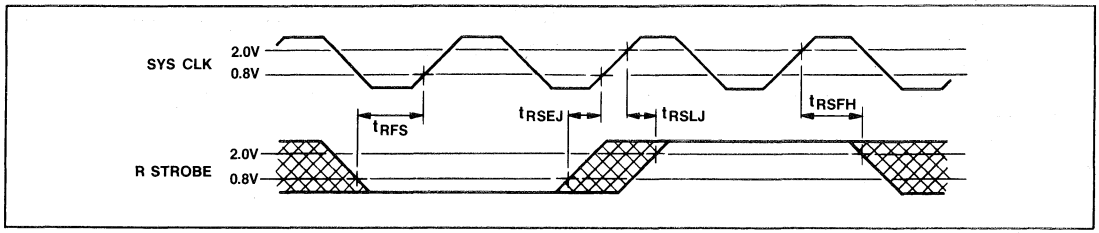


Fig.8 Timing - receive strobe

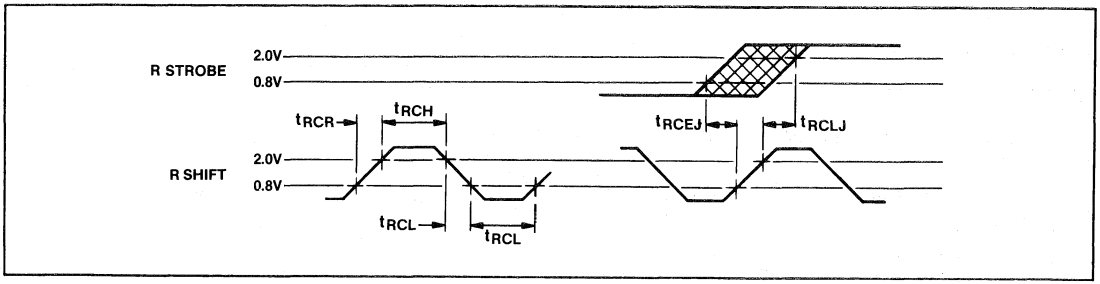


Fig.9 Timing - receive clock

Digital Switching Characteristics - Receive Data (see Fig.10)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
PCM input set-up time	t_{PIS}	60			ns	
PCM input hold time	t_{PIH}	60			ns	

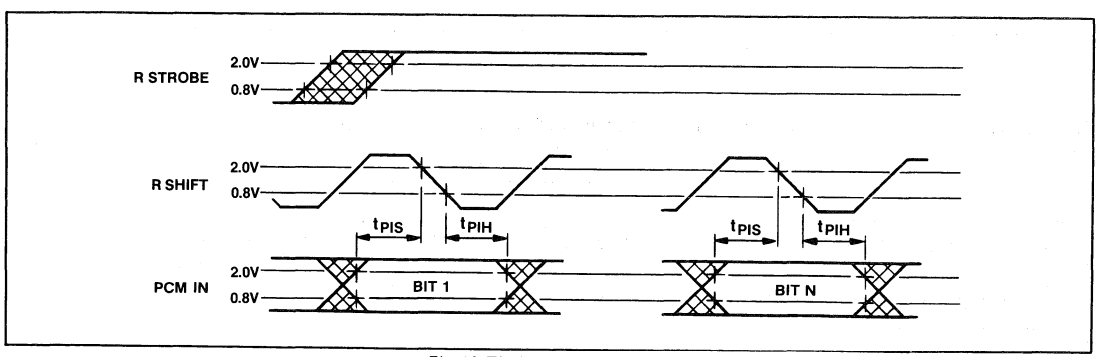


Fig.10 Timing - receive data

Digital Switching Characteristics - Transmit Strobe and Clock (see Figs.11 and 12)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Transmit strobe frequency	f_{TS}	7.99996	8	8.00004	kHz	Phase-locked with system clock
Transmit strobe falling set-up time	t_{TSFS}	120			ns	
Transmit strobe early jitter	t_{TSEJ}			200	ns	
Transmit strobe late jitter	t_{TSLJ}			100	ns	
Transmit strobe falling hold time	t_{TSFH}	220			ns	
Transmit clock frequency	f_{TC}	63.9997		2048.01	kHz	Phase-locked with transmit strobe
Transmit clock rise time	t_{TCR}			100	ns	
Transmit clock high period	t_{TCH}	$0.4/f_{TC}$		$0.6/f_{TC}$	s	
Transmit clock fall time	t_{TCF}			100	ns	
Transmit clock low period	t_{TCL}	$0.4/f_{TC}$		$0.6/f_{TC}$	s	
Transmit clock early jitter	t_{TCEJ}			200	ns	
Transmit clock late jitter	t_{TCLJ}			100	ns	

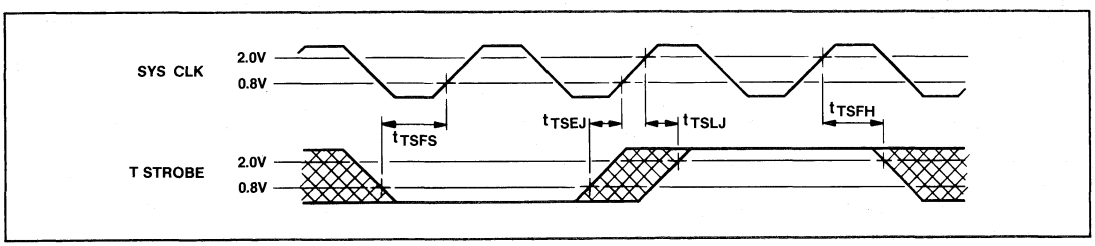


Fig.11 Timing - receive strobe

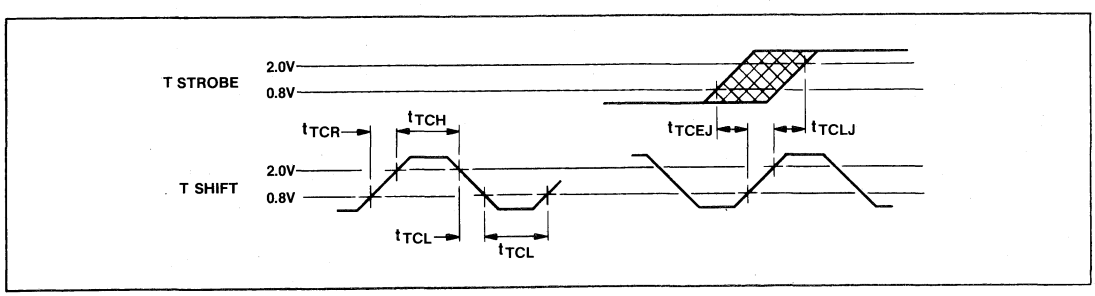


Fig.12 Timing - receive clock

Digital Switching Characteristics - Transmit Data (see Fig.13)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
PCM output holt time	t_{POH}	0	50		ns	
PCM output delay	t_{POD}		100	150	ns	

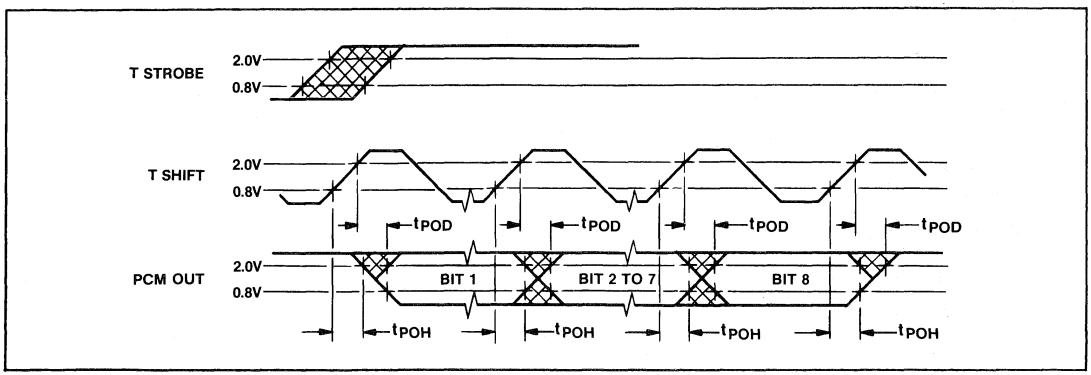


Fig.13 Timing - transmit data

Analog Channel Characteristics - Filter Delays

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
Transmit filter delay	t_{TFD}			182	μs	1kHz
Receive filter delay	t_{RFD}			110	μs	1kHz

Analog Channel Characteristics - A-Law

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
0dBm0 level (see Note 2)	0dBm0	5.3	5.8	6.3	dBm	±5V, 25°C
Variation in 0dBm0 level	Δ_{0dBm0}	-0.3	0	0.3	dB	Over test conditions
Weighted idle channel noise	ICN_W		-85	-73	dBm0p	CCITT G.712, §5.1 (see Note 3)
Single frequency idle channel noise	ICN_{SF}			-60	dBm0	CCITT G.712, §5.2
Weighted receive idle channel noise	ICN_{WR}			-78	dBm0p	CCITT G.712, §5.3
Spurious out-band noise	N_{SOB}			-30	dBm0	CCITT G.712, §7.1
Spurious in-band noise	N_{SIB}			-40	dBm0	CCITT G.712, §10
Two tone interdemodulation	IMD_{2T}			-35	dBm0	CCITT G.712, §8.1
Tone + power inter-demodulation	IMD_{TP}			-49	dBm0	CCITT G.712, §8.2
Crosstalk attenuation between V_{IN} and V_{OUT}	A_X	75	80		dB	CCITT G.712, §12

Analog Channel Characteristics - μ-Law

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.(1)	Max.		
0dBm0 level (see Note 2)	0dBm0	5.3	5.8	6.3	dBm	±5V, 25°C
Variation in 0dBm0 level	Δ_{dBm0}	-0.3	0	0.3	dB	Over test conditions
Weighted idle channel noise	ICN_W		5	17	dBrnc0	AT&T D3 (see Note 3)
Single frequency idle channel noise	ICN_{SF}			-60	dBm0	AT&T D3
Weighted receive idle channel noise	ICN_{WR}			15	dBrnc0	AT&T D3
Spurious out-band noise	N_{SOB}			-28	dBm0	AT&T D3
Spurious in-band noise	N_{SIB}			-40	dBm0	AT&T D3
Two tone interdemodulation	IMD_{2T}			-35	dBm0	AT&T D3
Tone + power inter-demodulation	IMD_{TP}			-49	dBm0	AT&T D3
Crosstalk attenuation between V_{IN} and V_{OUT}	A_X	75	80		dB	AT&T D3

NOTES
1. Typical figures are for design aid only. They are not guaranteed and not subject to production testing.
2. The typical 0dBm0 level of 5.8dBm corresponds to an RMS voltage of 1.51V and a maximum coding level of 3.1V.
3. The maximum value reduces to -68dBm0p without squelch (MV3508 with TST/SE pin unconnected).
4. The maximum value reduces to 22dBrnc0 without squelch (MV3509 with TST/SE pin unconnected).

ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage.
Functional operation under these conditions is not implied.

Positive supply voltage V_{DD}	-0.5V to +6.0V	Voltage at digital or analog pins V_P	V_{SS} -0.3V to V_{DD} +0.3V
Analog ground V_{AGND}	-0.1V to +0.1V	Package power dissipation P	1000mW
Negative supply voltage V_{SS}	-6.0V to +0.5V		
Storage temperature T_S	-65°C to +150°C		

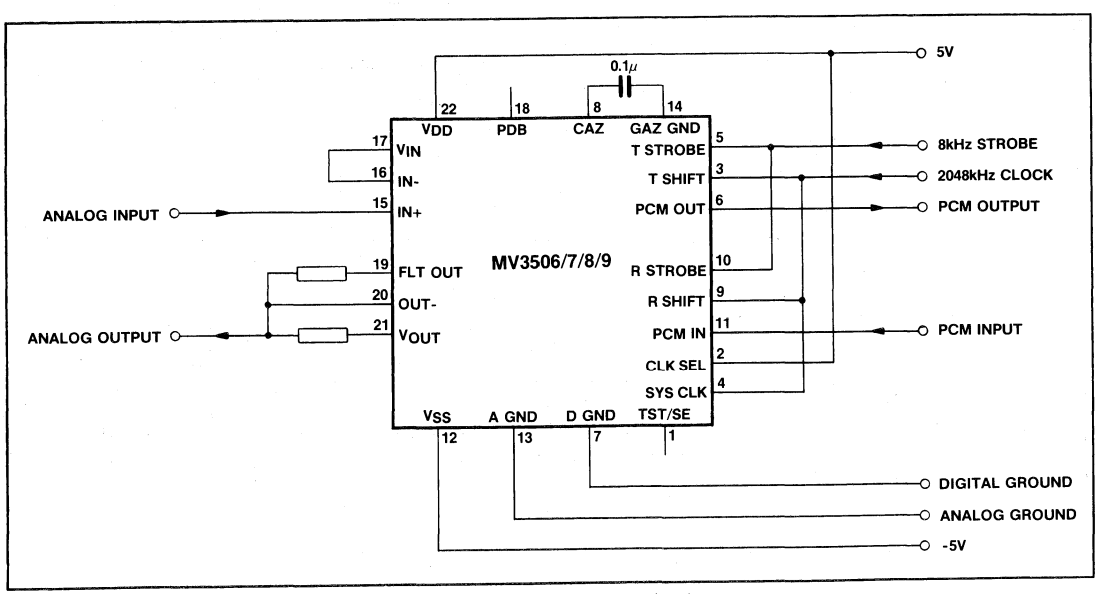


Fig.14 Simple application circuit

DS3134-1.0

SP1450B(B) & SP1455B(B)

PCM SIGNAL MONITOR CIRCUITS

The SP1450B and SP1455B are bipolar integrated circuits designed to monitor errors in three-level digital signals modulated by a three-alphabet 4B3T code such as MS43. They can also indicate the failure of positive or negative pulses in the signal. The high frequency capability allows operation in PCM systems up to 34M bit/s (SP1450) and 140M bit/s (SP1455). Facilities are provided to adjust input thresholds independently on each polarity of input and the error output can be interfaced with low speed CMOS circuitry or high speed ECL.

The SP1450B(B) and SP1455B(B) are similar to the SP1450B and SP1455B but are screened to MIL-STD-883, Method 5004, Class B.

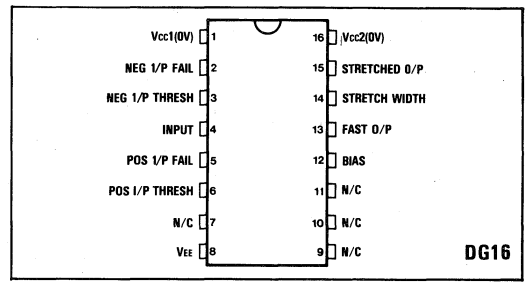


Fig.1 Pin connections (top view)

FEATURES

- Suitable for 34, 120 and 140M bit/s PCM
- Positive and Negative Input Signal Fail Outputs
- High Speed Error Output
- Low Speed 'Stretched' Output
- Low Power Consumption

APPLICATIONS

- PCM Telephone Transmission Terminal Equipment
- PCM Repeaters
- Error Checking Test Equipment

QUICK REFERENCE DATA

- Supply Voltage -4.4V to -5.25V
- Operating Temperature Range -10°C to +70°C
- Power Consumption 100mW typ
- Input Voltage Range ±450mV to ±1100mV (SP1450)
  ±450mV to ±600mV (SP1455)
- Thermal Resistance θj-a 100°C/W

ABSOLUTE MAXIMUM RATINGS

Supply voltage -8V
Reverse input current (pin 4) 5mA (continuous) 20mA (10us max)
Forward input current (pin 4) 20mA (10us max)
Storage temperature -55°C to +150°C
Operating temperature -10°C to +70°C
Junction temperature 150°C

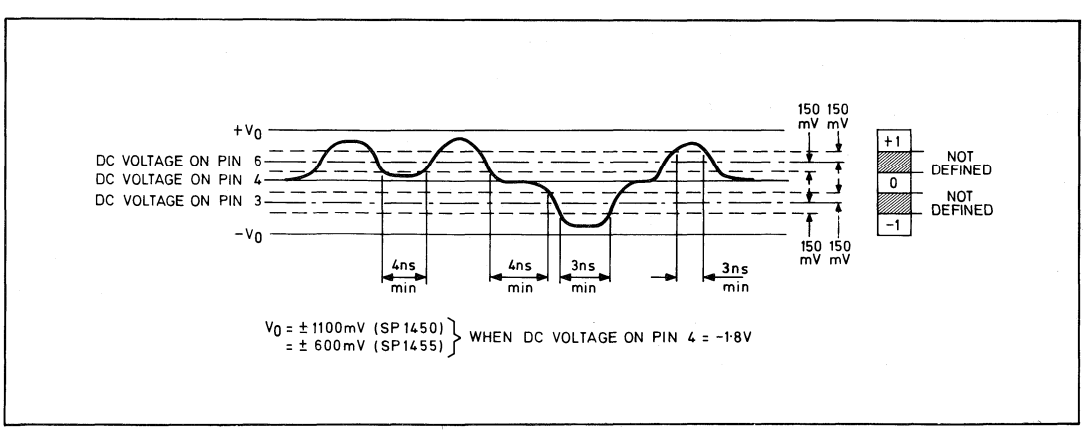


Fig.2 Input pulse wave form

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = Pins 1-16 = 0V, V_{EE} = Pin 8 = -5.0V, T_{amb} = +25°C, Input voltage range (pins 3,4,6) = -0.9V to -3.1V

DC CHARACTERISTICS

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Output low, current	2	0.9	1.2	1.9	mA	Pin 2 = OV Pin 3 = —1.7V Pin 4 = —2.0V
Output low, current	2	0.7	—	—	mA	Pin 2 = OV Pin 3 = —1.95V Pin 4 = —2.0V
Output high, current	2	—	—	1	µA	Pin 2 = OV Pin 3 = —2.3V Pin 4 = —2.0V
Output high, current	2	—	—	0.4	mA	Pin 2 = OV Pin 3 = —2.05V Pin 4 = —2.0V
Output low, current	5	0.9	1.2	1.9	mA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —2.3V
Output low, current	5	0.7	—	—	mA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —2.05V
Output high, current	5	—	—	1	µA	Pin 5 = OV Pin 4 = —2.0V Pin 6 = —1.7V
Output high, current	5	—	—	0.4	mA	Pin 5 = OV Pin 4 = —2.0V Pin 6 = —1.95V
Output low, current	13	6.0	7.0	9.0	mA	Pin 13,15 = OV Pin 3 = —1.7V Pin 4 = —2.0V Pin 6 = —2.3V Pins 2,5 = OV 470 Ω pin 12 to —5V 27 kΩ pin 14 to —5V Six pos. or neg. pulses on pin 4
Output high, current	15	—	—	1	µA	
Output high, current	13	—	—	1	µA	Pin 13, 15 = OV Pin 3 = —2.3V Pin 4 = —2.0V Pin 6 = —1.7V Pins 2,5 = OV 470 Ω pin 12 to —5V 27 kΩ pin 14 to —5V
Output low, current	15	0.5	0.75	—	mA	
Current consumption	1,16	—	20	25	mA	(Pins 2,5,13,15 = OV (Pins 3,6 = —2.3V (Pin 4 = —2.0V (27 kΩ resistor between (Pin 14 and —5V (Pin 12 open
Input bias current	3	—	—	40	µA	Pin 2 = OV Pin 3 = —1.7V Pin 4 = —2V
Input bias current	6	—	—	40	µA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —1.7V
Input bias current	4	—	—	80	µA	Pins 2,5 = OV Pins 3,6 = —2.3V Pin 4 = —2.0V

AC CHARACTERISTICS

Circuit reference: Fig.3, Input signal: Fig.2, T_{amb} = -10°C to +70°C, V_{EE} = -4.4V to -5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Input Frequency						
SP1450	13		—	25.5	M band/s	See note 1 below
SP1455	13		—	105	M band/s	See note 1 below
Stretched output pulse width	15	0.5	0.7	2	µS	C_1 = 390 pF R_1 = 27 kΩ using circuit of Fig. 7 (see note 2 below)
Error pulse width SP1455	13	4.25	—	5.25	nS	Input freq. 105 M band/s
Error pulse amplitude	13	300	—	—	mV	At max input frequency
Spurious pulse amplitude	13	—	—	50	mV	At max. input frequency

NOTE 1: These figures are the max.input symbol rates. For 4B3T codes, the effective bit rate is 4/3 x (input frequency).

NOTE 2: Resistor and capacitor values quoted are absolute values; temperature coefficients and tolerances have not been taken into account.

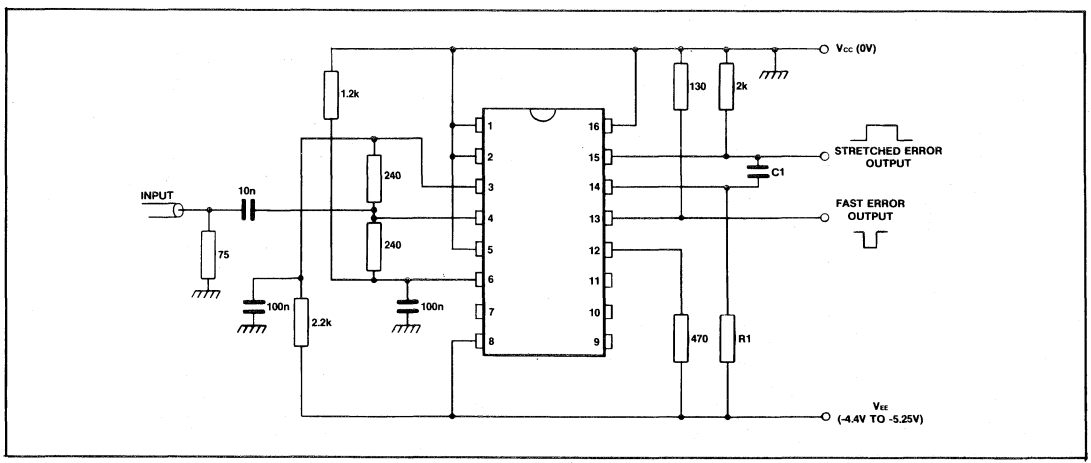


Fig.3 Functional test circuit

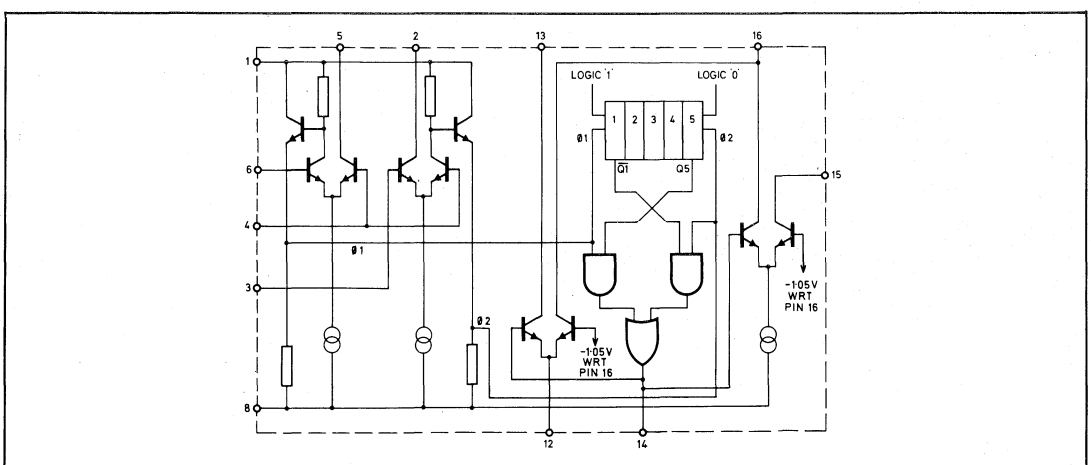


Fig.4 Circuit diagram of SP1450/SP1455

APPLICATIONS

The circuit shown in Fig.3 is designed to accept a three level (ternary) input signal as shown in Fig.2. The input is applied to pin 4 whilst fixed bias levels are maintained on pins 3 and 6. When a positive input pulse is applied at a level more positive than the bias on pin 6 the positive comparator output o 1 goes from '0' (V_{EE}) to '1' (V_{CC}). The 1-0 edge of this pulse clocks the five bit shift register one place to the right. Repeated operation will cause a pattern of logic '1's to be propagated along the shift register. When bit 5 is at logic '1' and the input is also positive an 'error' will occur at pins 13 and 15.

A negative input pulse at a level more negative than the voltage on bias pin 3 causes the negative comparator output o 2 to clock the shift register one place to the left. Repeated operation causes a pattern of logic '0's to be propagated along the shift register. When bit 1 is at logic '0' and the input is also negative an 'error' output will again occur at pins 13 and 15.

During normal operation the shift register can assume one of only six possible states as shown in Fig.5.

State	1	2	3	4	5
A	0	0	0	0	0
B	1	0	0	0	0
C	1	1	0	0	0
D	1	1	1	0	0
E	1	1	1	1	0
F	1	1	1	1	1

Fig.5 Shift register states

When power is initially connected other states may occur.

Two 'error' outputs are available. The fast output at pin 13 is negative going; the peak current is defined by a resistor connected between pin 12 and V_{EE} according to the formula:

$$I = \frac{3.3}{R} \text{ (e.g. 820 ohms; 4mA)}$$

A pullup resistor must then be connected between pin 13 and V_{CC} to give a suitable voltage swing. A suitable ECL interface is shown in Fig.6.

If, as in a repeater application, a fast output is not required, pin 12 should be left open and pin 13 connected to V_{CC} (pin 16).

A stretched output is available from pin 15 by connection of a capacitor between pins 14 and 15. A suitable circuit is shown in Fig.7.

Facilities are available at pins 2 and 5 to detect the absence of negative and positive going input signals. If these are not required pins 2 and 5 should be connected to V_{CC} (pin 1). A CMOS interface circuit is shown in Fig.8.

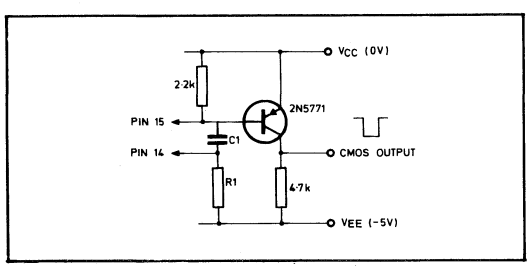


Fig.7(a) Interfacing with CMOS at the stretched output (SP1450)

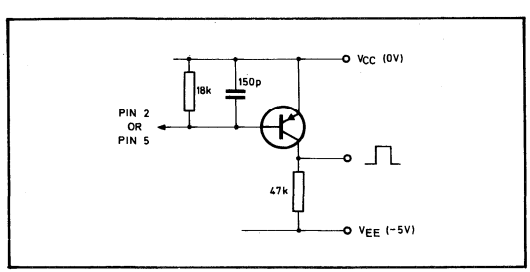


Fig.8 Interfacing with pulse fail output with CMOS

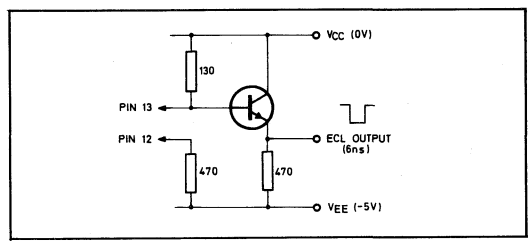


Fig.6 Interfacing with ECL at the output

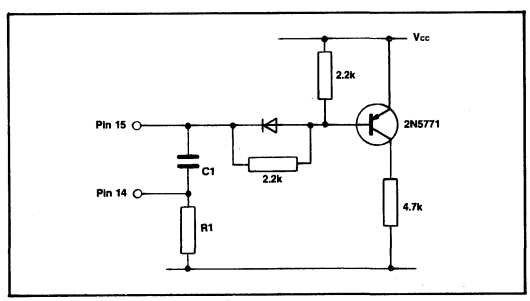


Fig.7(b) Interfacing with CMOS at the stretched output (SP1455)

Section 3
Line Card Circuits

Subscriber Line Interface Circuits (SLICs) - Selection Guide

Functional Features	SL373 (p.3-3)	SL374 (p.3-27)	SL376 (p.3-52)	SL7950 (p.3-79)	SL7953 (p.3-107)
Line Feed Regulator	√	√	√	√	√
Constant Current Feed (Normal, Active Region)	√	√			√
Resistive Feed (Normal, Active Region)			√	√	
Off-Hook Detector (OHD)	√	√	√	√	√
Off-Hook Detector Hysteresis		√			
Standby Mode	√	√	√	√	√
Ring Trip Detector (RTD)	√	√	√	√	√
Ground Key Detector (GKD)	√	√	√		√
Detector Select Input, E1 (OHD/GKD)	√	√	√		√
Detector Output Pin Enable Input, E0			√	√	√
Polarity Reversal (Active and Standby Modes)	√	√	√	√	√
Meter Pulse Capability			√		
Test Relay Driver	√	√		√	
Ring Relay Driver	√	√	√	√	√
Trimmable Longitudinal Balance - Note 1 (>60dB)		√			
On-chip Substrate Resistor			√	√	√

NOTE 1. This can be performed during device testing; however, standard production does not implement this feature. Refer to individual data sheet for specified untrimmed parameter value.

Parametric Differences	SL373 (p.3-3)	SL374 (p.3-27)	SL376 (p.3-52)	SL7950 (p.3-79)	SL7953 (p.3-107)
Standby Current Level	$K_{LIM} \times I_{DET}$	$1/2 \times I_{ACT}$	$K_{LIM} \times I_{DET}$	$K_{LIM} \times I_{DET}$	$K_{LIM} \times I_{DET}$
2-Wire Dynamic Range	±3V	±3V	±6V	±3V	±3V
Nominal Transmit Gain	0dB	0dB	−6dB	0dB	0dB
V_{CC} Supply Range	+5V ± 5%	+5V ± 5%	+5V ± 5%	+5V ± 5%	+5V ± 5%
V_{EE} Supply Range	−5V ± 5%	−5V ± 5%	−5V ± 5%	−5V ± 5%	−5V ± 5%
V_{BB} Supply Range	−40.5/−64V	−40.5/−64V	−44/−52V	−40.5/−64V	−40.5/−64V
Off-Hook Threshold/s	$350 \div R_{TH}$	$410 \div R_{TH}$ $465 \div RTH$	$350 \div R_{TH}$	$350 \div R_{TH}$	$350 \div R_{TH}$
Line Voltage Saturation Guard (V_{SG})	15V	15V	16.5V	15V	15V

Current Package Options
DG28 (28-lead ceramic DIL) - Standard for all SLICs
LC28 (28-lead LCC) - Optional
LC32 (32-lead LCC) - Optional
LC44 (44-lead LCC) - Optional
For details of optional and other types of packaging, please contact your local Customer Service Centre.

DS2098-1.0

SL373

SUBSCRIBER LINE INTERFACE CIRCUIT

The SL373 is a Subscriber Line Interface Circuit (SLIC) for use at the telephone exchange or PABX end of a telephone line.

It provides power feed, transmits and receives voice signals, controls ringing, supports line testing and detects Ground Key or Off-Hook conditions. These functions can be programmed to provide the flexibility required for different telephone networks.

The SL373 is fabricated using bipolar technology.

FEATURES

- Low Power Line Feed via Regulator
- Programmable Constant Current Feed Independent of Battery to Line
- Programmable AC Termination Impedance
- Good Longitudinal Balance
- Ground Key and Ring Trip Detection
- Programmable Off-Hook Detection
- Disconnect and Low Power Standby Modes
- A-Leg Disconnect, B-Leg Standby Mode
- Normal or Reversed Line Polarity Operation
- Ring and Test Relay Drivers
- Thermal Shut-Down Protection

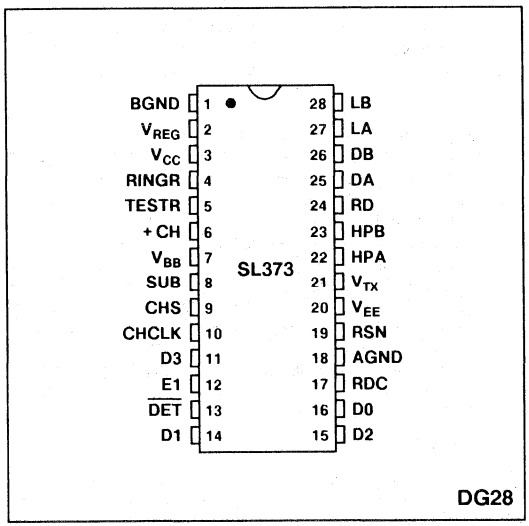


Fig. 1 Pin connections - top view

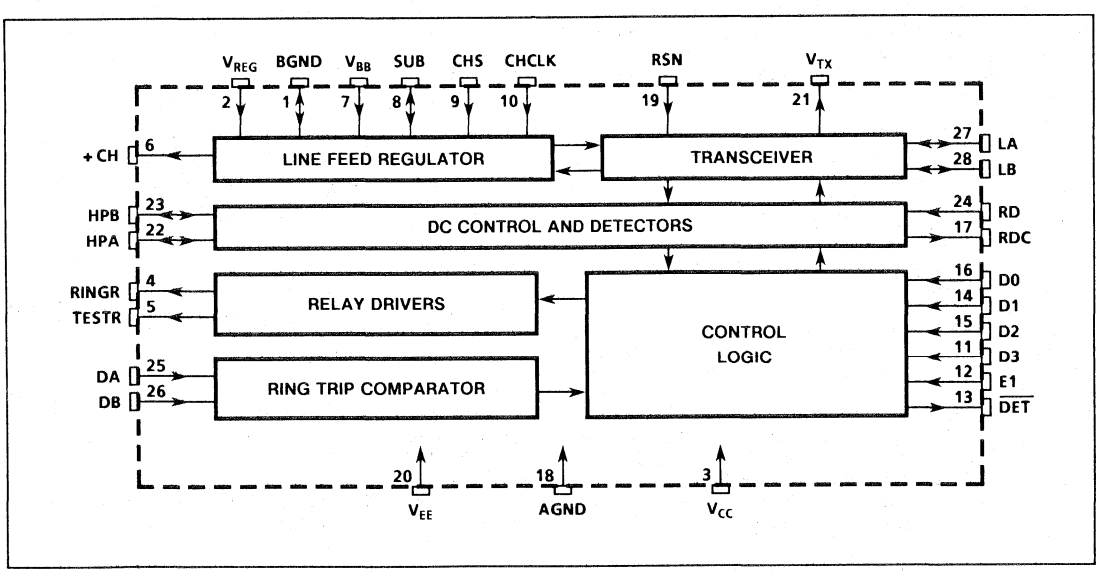


Fig. 2 : Functional Block Diagram

FUNCTIONAL OVERVIEW

The SL373 Subscriber Line Interface Circuit (SLIC), together with some external components, provides most of the line interface functions for ordinary or PABX line connections in a telephone network. It performs the interface between the two wire line and an ALAP (Analogue Line Audio Processor)/COMBO, such as the GEC Plessey Semiconductors MV3010 PSLAC (Plessesy Subscriber Line Audio Circuit) DSP device.

The SLIC circuit contains several functional blocks to achieve the design aims (Fig.2). Firstly, the Transceiver consists of the two wire port, pins LA and LB. These pins are fed from the 4 wire input (RSN) controlling AC conditions, and from the Line Feed Regulator and DC Control blocks, controlling DC conditions. The 2 wire transverse AC signal is fed onto the 4 wire transmit output, VTX.

Power dissipation is minimised, under varying line conditions, by the Line Feed Regulator which adjusts the internal high voltage supply to that required for line feed. It consists of a switching regulator which can be synchronised to a 256kHz clock.

DC line conditions at the 2 wire interface are determined by the DC Control block. These DC conditions (modes of operation) are set by the Control Logic, which also monitors line status (On/Off-Hook) via the DC Control block detectors (Loop/Ground Key/Ring Trip comparator). The control logic also controls the Ring Relay Driver for Ringing mode of operation and an undedicated Test relay driver.

A brief outline of the device functionality is given below, before a more detailed discussion of the SLIC circuitry in the Functional Description section.

LINE FEED

Line loop (pins LA &LB) feeding is obtained from the battery supply (pin 7) by means of an internal power circuit, which can be set to different modes of operation (refer to table 2). These modes are as follows:

Standby Mode

Standby mode is the SLIC's low power mode in which the battery feed circuit limits the DC loop current to a level just sufficient to enable the SLIC to detect current above the On/Off-Hook threshold. This mode is used when the subscriber is Off-Hook and no call is in progress, or if On-Hook, to save power. Both the Loop and Ground Key detectors work in this mode.

Disconnect A and B Leg

This mode programs the SLIC such that the A and B leg output amplifiers are turned off, preventing current flow to the line.

Disconnect A, Standby B Leg

This is the SLIC Standby mode with the A Leg amplifier turned off, so that current can only flow in the B Leg. In this state it is only possible to detect the application of a ground to the B Leg.

Active Mode

This is the normal operating mode with a call in progress. The SLIC is used as a constant current feed device, with the feed current being set by external resistors.

Polarity reversal

The polarity of the feeding voltage at the SLIC can be reversed on command, in Active and Standby modes. All Active and Standby conditions apply equally to the respective reverse conditions. In these conditions the polarity of any DC parameter is reversed.

Ringing

This mode enables the Ring Relay output and selects the Ring Trip comparator. It does not provide DC line feed or AC ringing voltage which must be supplied externally (via the ring relay).

Test Mode

Testing of the line is not performed by the SLIC. This mode enables external access to the telephone line by directly driving the test relay.

SUPERVISION

The SLIC provides an Off-Hook (or loop) Detector (OHD), Ring Trip Detector (RTD) and a Ground Key Detector (GKD). These are described below, in addition to the SLIC on-chip thermal protection.

Off-Hook Detector

The Off-Hook Detector recognises the loop status by means of a threshold circuit. The OHD operates in Standby and Active modes (with or without polarity reversal), and in the presence of longitudinal currents. The detector threshold is nominally the same in Standby and Active modes, the actual level being externally programmable.

Ring Trip Detector

This detects when a subscriber goes off-hook during the application of a ringing signal (normally 25Hz) within a maximum delay of 150ms (determined by external components - see Applications section). The detector is active when the Ring Relay Driver is activated.

Ground Key Detector

The GKD circuit detects a current path from the A or B Leg to ground. It can be used in Standby, Active and Disconnect A Standby B modes.

Thermal Protection

In conditions which cause the chip junction temperature to rise above a critical level (around 170°C), the thermal protection will operate. This switches off the line current and therefore reduces the power dissipation.

TRANSMISSION

The signal transmission functions include 2 to 4-wire and 4 to 2- wire conversions.

The 2-wire termination impedance of the SLIC is programmed by external components. Transmit and Receive Gain are fixed and are nominally both unity (0dB), with the 2- wire port terminated in a matched load.

All the transmission parameters apply when the SLIC is operating in the presence of longitudinal currents, as specified in the Electrical Characteristics.

CONTROL

The SLIC is provided with a digital interface for controlling the 2-wire line status and passing line status information to the line card/system hardware. The operating characteristics can be selected by hardware with external components (see Digital Interface).

METERING

Injection of high amplitude high frequency meter pulses is not supported by the SL373. If this function is required, then the GPS SL376 Metering SLIC can be used instead (refer to separate Data Sheet).

RINGING

The application of the ringing voltage to the subscriber line can be via a relay or suitable high voltage crosspoint, external to the SLIC. This component is driven by the on-chip Ring Relay Driver. The relay is connected between RINGR and V_{BAT}.

When the SLIC is set to RING mode, the Ring Relay Driver output will be activated to energise the ring relay. The relay should be connected so as to cause the line to be disconnected from the SLIC and connected to a suitable ringing supply (continuous) voltage. Ring cadence can then be obtained by de-energising and re-energising the relay as required.

OVERVOLTAGE PROTECTION

Overvoltage protection is required to protect the SLIC from such line phenomena as lightning strikes, and induced AC signals from, or direct contact with, power lines. This protection can be realised with components external to the SLIC (refer to SL373/SL376 Application Note AN82).

INTERFACES

The SLIC has three main interfaces to external circuitry. These are the 2-wire, 4-wire and Digital interfaces which are described below.

Subscriber Line Interface (2-wire port)

Pins LA and LB form the Subscriber Line Interface providing line feed, signalling supervision and voice transmission between the subscriber's apparatus and exchange. It exhibits very good balance about ground to minimise the crosstalk between adjacent pairs in the local cable and noise from longitudinal interference. The termination impedance is set externally by Z_{TX} (see Fig. 3 and Functional Description).

The 2-wire port is designed to offer a low impedance to any longitudinal signals that appear on the subscriber line and the resulting signal level at the 4-wire output port is minimised.

It is able to handle longitudinal currents on the subscriber line in all modes of operation, except Disconnect mode, Ringing and Disconnect A Standby B when the SLIC 2-wire port is no longer connected to the line.

Analog 4-wire interface

Two pins of the SLIC (V_{TX} and RSN), together with associated grounds, provide the 4 wire interface to an ALAP or COMBO device. Both the transmit (V_{TX}) and receive (RSN) signals are unbalanced and have fixed gain settings. The V_{TX} pin has a low output impedance, whilst the RSN pin is a low impedance virtual earth input. The input current is normally a combination of the receive voice signal from the ALAP, line feed current programmed by the RDC pin (see Applications section) and termination of the V_{TX} pin.

Hybrid Balancing is not provided on the SLIC. This can be done by an ALAP such as the MV3010 PSLAC which uses DSP techniques, including an Adaptive Echo Cancellation feature.

Digital Interface

This is a parallel interface providing control of all the SLIC operating modes and indication of line status information. It consists of the 6 pins as listed in Table 1, the functions of which are described in Table 2.

Pin designation	Pin description
D0	Data Input
D1	Data Input
D2	Data Input
D3	Test Select Input
E1	Detector Select Input
$\overline{DET}$	Detector Data Output

Table 1 Digital interface pin designation

Mode	D3	D2	D1	D0	$\overline{DET}$ output status (Note 2)		Test relay
					E1 = 0	E1 = 1	
Disconnect A & B Legs	X	0	0	0	(Invalid)	(Invalid)	-
Ringing	X	0	0	1	Ring Trip (Note 3)	-	-
Active(Non-ringing)	X	0	1	0	Loop Detect	Ground Key	-
Standby	X	0	1	1	Loop Detect	Ground Key	-
Disconnect A,Standby B	X	1	0	0	(Invalid)	Ground Key	-
Reserved	X	1	0	1	-	-	-
Active, Polarity Reversed	X	1	1	0	Loop Detect	Ground Key	-
Standby, Polarity Reversed	X	1	1	1	Loop Detect	Ground Key	-
Line Test (Note 1)	0	X	X	X	-	-	Enabled
	1	X	X	X	-	-	Disabled

NOTES

1. D2, D1, D0 still change SLIC status even though Line outputs will be disconnected from line.
2. $\overline{DET}$ = 1 for On-Hook (high line impedance), $\overline{DET}$ = 0 for Off-Hook (low line impedance).
3. $\overline{DET}$ = 1 for Voltage DA > DB , $\overline{DET}$ = 0 for Voltage DA < DB.

Table 2 Digital interface functional description.

FUNCTIONAL DESCRIPTION

VOICE TRANSMISSION AND RECEPTION

It is conventional to assign the signal directions from the point of view of the served telephone set. The receive direction is towards the served telephone and the transmit direction is from it.

The basic voice circuit for the device is shown in Fig.3. The current which flows on the line, into LA and out of LB, is 1000 times the current which flows into RSN and through the device to AGND.

The AC voice current flowing into RSN is composed of the current from V_{RX} through Z_{GR}, which controls the signal received at the remote telephone and a current from V_{TX} through Z_{TX} which controls the termination impedance. There is also a DC current at RSN which is analysed later in the discussion on DC line feed.

The 2 wire termination impedance is $Z_{AB} = (Z_{TX} \div \alpha)$ where α ($\simeq 1000$) is the current gain between RSN and I_L (see Fig.3). This can be checked by setting V_{RX} to zero.

The Receive Gain, for normal voice signals (at V_{RX}), is inversely proportional to Z_{GR}. The actual value, which is negative, can be obtained by setting $(V_L)_{ac}$ equal to zero in Fig.3. This gives:-

AC voltage between LA and LB $(V_{LA}-V_{LB})_{ac}$

$$= (V_{LA} - V_{LB}) - (V_{HPA} - V_{HPB})$$
$$= (I_L)_{ac} \times \{Z_{AB} \| Z_L\}$$
$$= -\left(\frac{Z_L \times \frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right) \frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}$$

i.e. minus the ratio of the line and terminating impedances (Z_L and $Z_{TX} \div \alpha$) in parallel, to the receive impedance divided by the current gain ($Z_{GR} \div \alpha$). This expression simplifies to :-

$$= \frac{-V_{RX}\alpha Z_L Z_{TX}}{(\alpha Z_L + Z_{TX})Z_{GR}}$$

In the transmit direction, the voltage at V_{TX} is the superposition of the voltage from the line, with the voltage produced on the line from V_{RX}, i.e:-

$$V_{TX} = \left[\left(\frac{\frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right) V_L - \left(\frac{Z_L \times \frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right) \frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}\right]$$

This expression simplifies to :-

$$V_{TX} = \frac{[Z_{GR}(V_L)_{ac} - \alpha Z_L V_{RX}]Z_{TX}}{(\alpha Z_L + Z_{TX})Z_{GR}}$$

This equation can be used to determine the transmit gain, from $(V_L)_{ac}$ to V_{TX}, by setting $V_{RX} = 0$ which gives $+Z_{TX} \div (\alpha Z_L + Z_{TX})$. The 4 wire-4 wire gain, V_{RX} to V_{TX}, is also given by this equation when setting $(V_L)_{ac} = 0$, which gives us the alternative result $-\alpha Z_L Z_{TX} \div [(\alpha Z_L + Z_{TX})Z_{GR}]$. If fuse resistors are included in the 2 wire loop, then Z_L is modified to become $(Z_L + 2R_{FUSE})$ in the above equations.

The transmission circuitry also contains a longitudinal feedback circuit, such that the SLIC appears as typically 25Ω resistors from LA and LB to a bias voltage (see DC Line feed section). This bias voltage comes from the DC feed circuitry. The feedback circuit attenuates longitudinal signals from the transmit path, and has no effect on transverse signals.

DC LINE FEED (Active Mode)

DC line feed (loop) current $I_L = \frac{1}{2}(|I_A - I_B|)$ is provided by the device when it is in non-ringing modes. In RING mode, DC line feed and AC ringing voltage are normally applied through the ring relay which is controlled by the device. The line feed current is reduced during standby operation.

In Active mode, Power feed is controlled by the resistance R_{DC} ($= R_{DC1} + R_{DC2}$) between the R_{DC} pin and the RSN pin (Fig.4). Again, the current in the 2 wire loop will be 1000 times the current into RSN. Operation of the DC feed circuitry is described with reference to Fig.4, which shows a conceptual model.

For the normal line feed region, a voltage V_{DC}, of magnitude 2.5V is produced at the R_{DC} pin. The sign of V_{DC} determines normal or reverse polarity operation. If negative, normal polarity is established and if positive, reverse polarity will occur (polarity is set by control logic - see Table 2). This normal line feed region exists when $|V_{BAT}| - |V_{DCT}| \geq V_{SG}$ ($V_{SG} = 15V$ nominally, $V_{DCT} = |V_{LA} - V_{LB}|$), else the Saturation Guard circuit is active (described later).

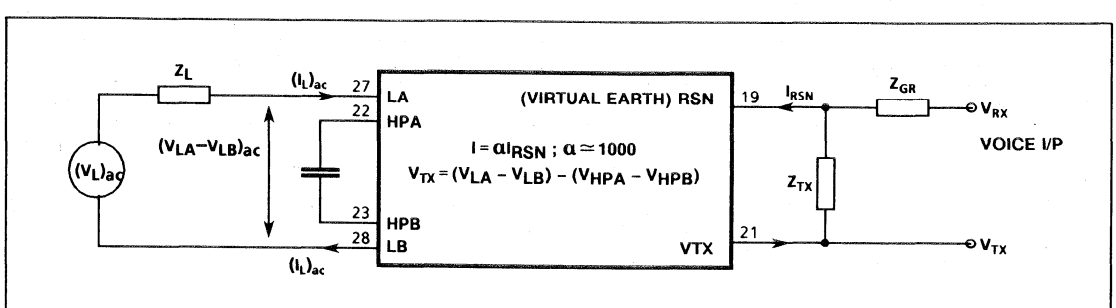


Fig.3 Voice circuit

Note that the internal resistors, R_{HP}, and external capacitor, C_{HP}, form a low pass filter network (see discussion on C_{HP} in SL373/SL376 Application Note AN82 Applications General Considerations Section). During the action of reversing polarity, the resistors R_{HP} are momentarily short-circuited to reduce the time taken for the DC voltage on C_{HP} to change sign.

The ×1000 virtual earth input current amplifier means that the feed current is determined by R_{DC}, i.e:-

$$I_{FEED} = 2500 \div R_{DC} \text{ (Saturation Guard inactive)}$$

If fuse resistors are included in the 2-wire loop, the feed current will not be affected. However, the fuse resistors will affect the line current in the saturation guard region (desribed later).

As an example, to set $I_{FEED} = 40mA$, then:-

$$R_{DC} = (R_{DC1} + R_{DC2}) = 2500 \div I_{FEED} = 62.5k\Omega$$

The values of R_{DC1} and R_{DC2} should be kept nearly equal, forming a low pass filter network with C_{DC} to reduce chopper noise from the RDC pin (see also discussion in AN82 Applications General Considerations Section). The time constant of this network (C_{DC} and $R_{DC1} \| R_{DC2}$) also affects the time taken for a polarity reversal, and it is normally ≈1.5ms.

The remaining circuitry models the action of the saturation guard circuit. This operates to reduce the voltage at the RDC pin when:- $|V_{BAT}| - |V_{DCT}| < V_{SG}$. V_{SG} is a notional threshold voltage which is the headroom between the value of V_{DCT} and the battery voltage at the point where saturation guard becomes active (this includes the diode drop in series with the V_{BAT} supply, D_2 figure 7). Thus, when the comparator determines this condition, the magnitude of the difference is used to reduce the voltage at RDC.

The total line feed characteristic is shown graphically in Figs. 6a and 6b. The nearly constant voltage region is due to the action of the saturation guard circuit, and is affected by the value of R_{FUSE} as shown in Fig. 6a. Fig. 6b plots the loop current value as a function of line resistance R_L. The example shown is that of a 40mA ($R_{DC} = 62.5K\Omega$) feed current, the graphs being obtained by using the simple models of Figs. 5a and 5b (0Ω fuse resistors). Figs. 6a and 6b also show the action of V_{BB} on the line characteristics.

With the Saturation Guard inactive, normal line feed conditions apply such that the feed current and line/loop resistance determine V_L by the following relationship:-

$$V_L = I_L \times R_L$$

This gives the characteristic shown in Fig. 6a, which is the vertical line section of the graph.

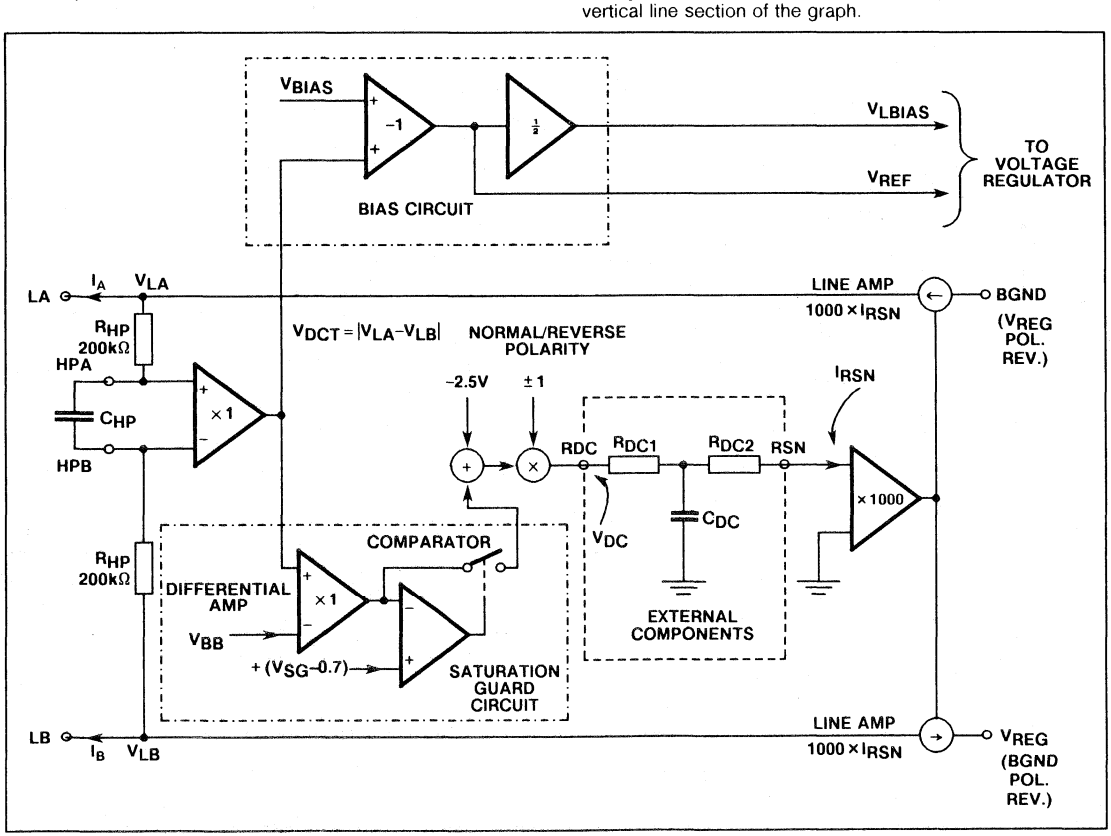


Fig.4 DC power feed circuit model.

When the saturation guard is active, then the line voltage is effectively held constant due to the reduction of the voltage at the RDC pin. Thus, line conditions are set by the following:

$$I_L = [(|V_{BAT}| - V_{SG}) \div (R_L + 2R_{FUSE})]$$

To determine the line resistance (R_{LSG}) and Line voltage (V_{LSG}) at which the saturation guard becomes active, these parameters are obtained by equating the two expressions for normal and saturation guard regions. Thus,

$$R_{LSG} = [(|V_{BAT}| - V_{SG}) \times (R_{DC} \div 2500)] - 2R_{FUSE}$$
$$V_{LSG} = |V_{BAT}| - V_{SG} - [2R_{FUSE} \times (2500 \div R_{DC})]$$

The resultant line voltage (V_{LSG}) that occurs depends on the ohmic relationship of I_{LSG} and R_{LSG} (see Fig. 6a) which will equal $|V_{BAT}| - V_{SG}$ when $2R_{FUSE} = 0\Omega$. The open circuit voltage, $V_{LOC} \approx |V_{BAT}| - V_{SG}$ at $R_L = \infty\Omega$, will always be greater than V_{LSG}, even when $2R_{FUSE} = 0\Omega$. This change in voltage between V_{LSG} and V_{LOC} will be greater at lower battery voltages. Fig. 6a shows the nominal effect.

DC LINE FEED (Standby Mode)

For Standby mode, the DC current is limited to a value just sufficient for the loop Detector to sense Off-Hook.

Normally this threshold (I_{DET}) is set externally by a resistor, R_{TH} (see Control and Signalling section). The limited loop current (I_{LIM}) is also determined by R_{TH} via a conversion factor K_{LIM} (nominally 1.7, see Electrical Characteristics) such that :-

$$I_L \leq I_{LIM} = K_{LIM} \times I_{DET}$$

The shape of this characteristic is almost a constant current, as shown in Fig. 6a. Since $K_{LIM} > 1$, the current level is still sufficient to detect the Off-Hook threshold (see Control and Signalling section).

LINE POLARITY

Normal polarity (Active/Standby) consists of the LA pin voltage near BGND and the LB pin voltage near V_{BB}. Under these conditions $I_L = +\frac{1}{2}|I_A - I_B|$ and the voltage at the RDC pin is negative. Reverse polarity will give LA voltage near V_{BB}, LB voltage near BGND, $I_L = -\frac{1}{2}|I_A - I_B|$ and the voltage at the RDC pin is positive.

BIAS CIRCUIT

The Bias circuit (Fig. 4) produces two reference voltages, both referred to ground. These are V_{REF}, being related to the 2-wire transverse DC voltage and V_{LBIAS} approximately half V_{REF}.

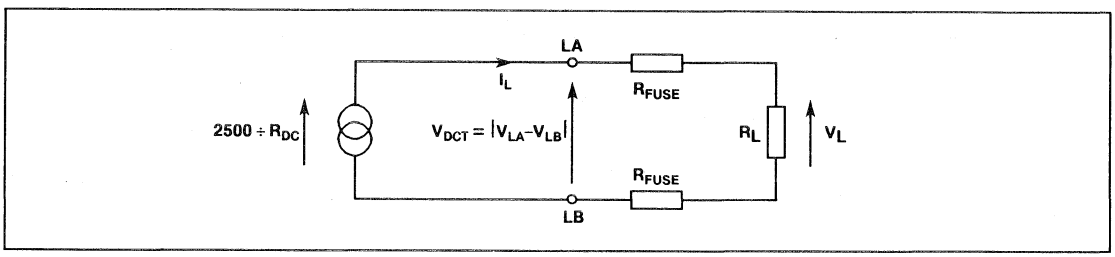


Fig. 5a Simple power feed model (normal line feed)

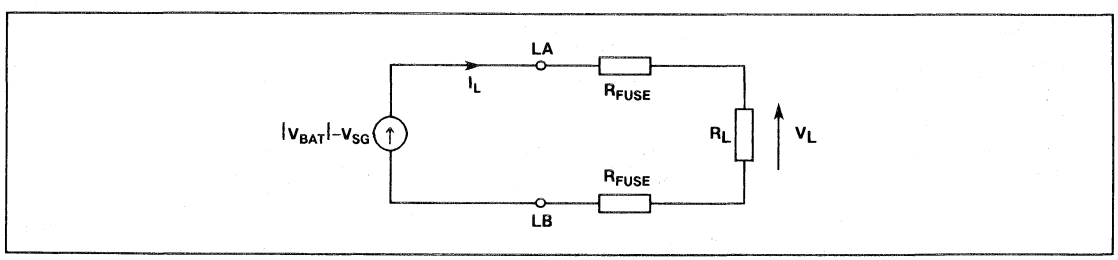


Fig. 5b Simple power feed model (saturation guard active)

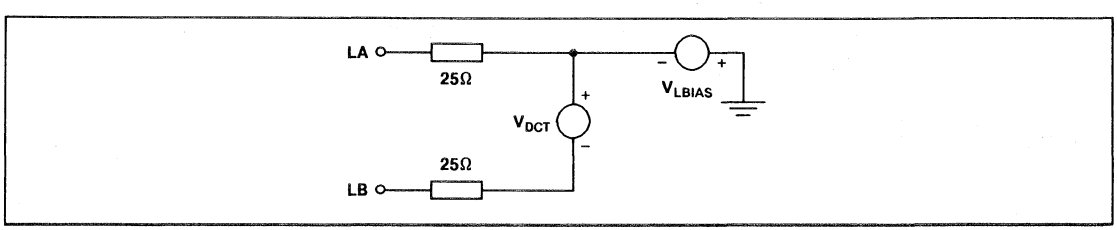
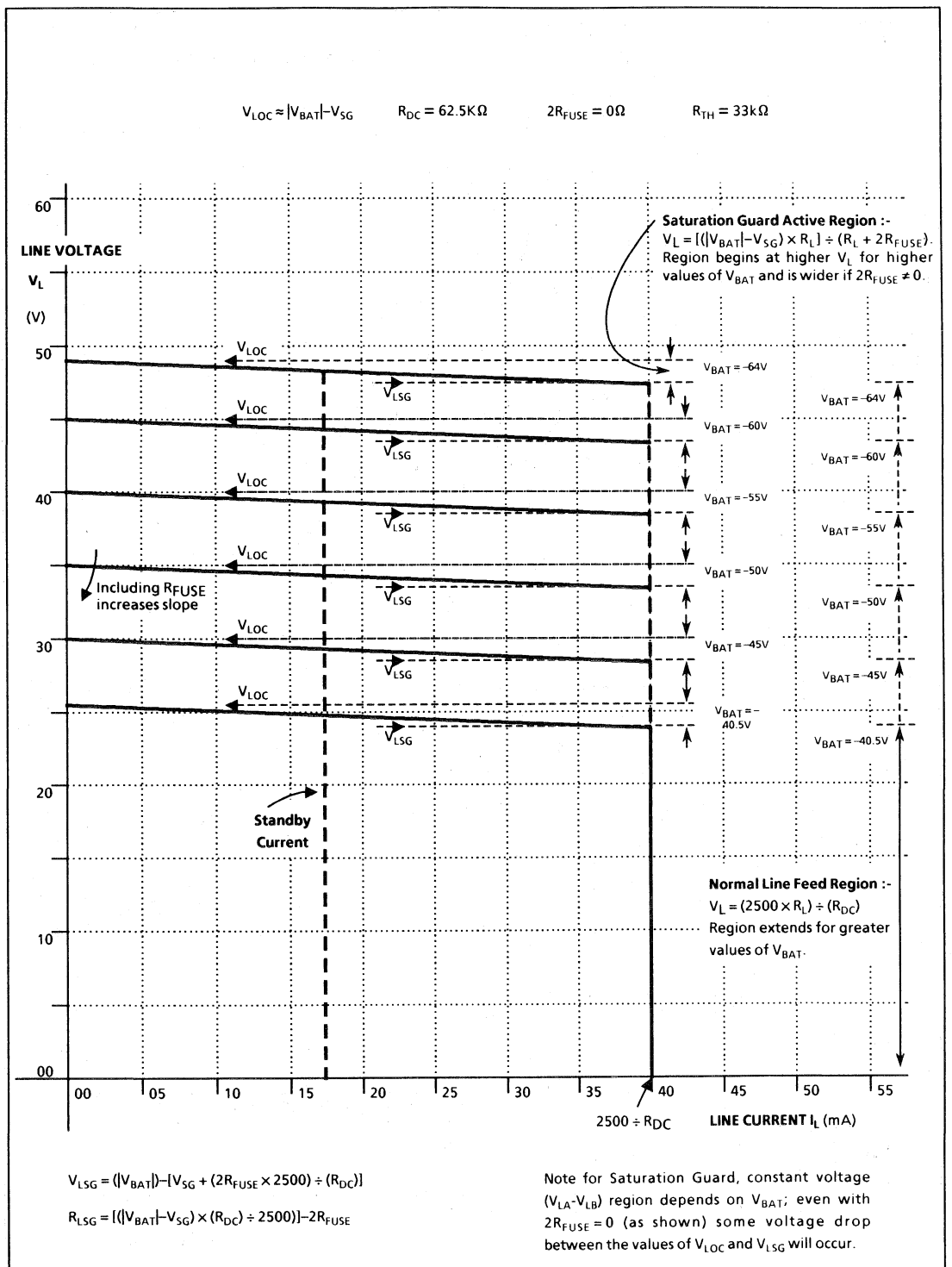


Fig. 5c Longitudinal bias circuit.



$V_{LSG} = (|V_{BAT}|) - [V_{SG} + (2R_{FUSE} \times 2500) \div (R_{DC})]$

$R_{LSG} = [(|V_{BAT}| - V_{SG}) \times (R_{DC}) \div 2500)] - 2R_{FUSE}$

Note for Saturation Guard, constant voltage (V_{LA}-V_{LB}) region depends on V_{BAT}; even with $2R_{FUSE} = 0$ (as shown) some voltage drop between the values of V_{LOC} and V_{LSG} will occur.

Fig. 6a Line feed characteristic, V_L vs I_L.

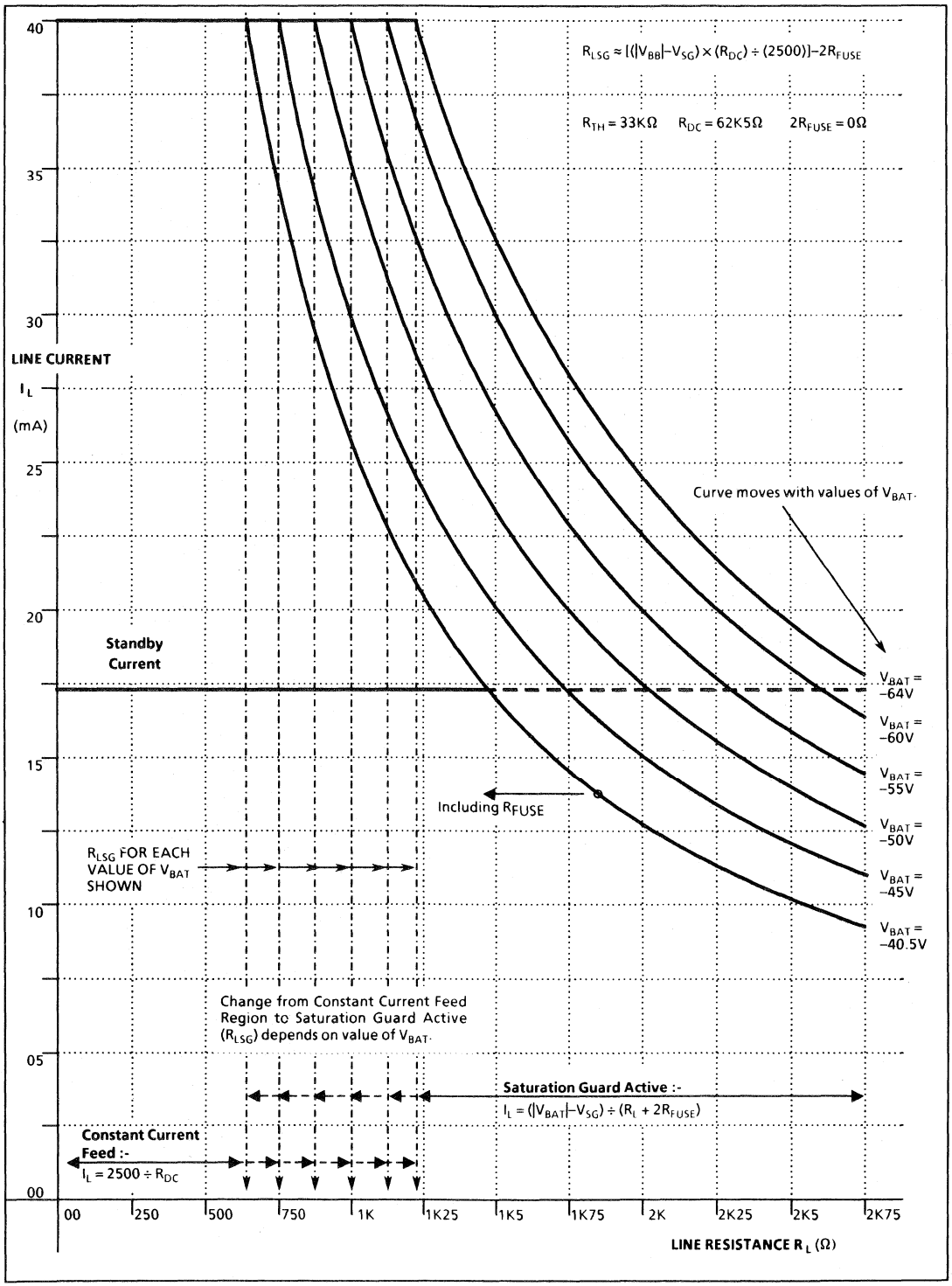


Fig. 6b Line feed characteristic, I_L vs R_L.

V_{REF} controls the line feed regulator and V_{LBIAS} sets the 2-wire feed balance voltage (centre point voltage of the lines). The longitudinal control loop achieves an input impedance of approximately 25Ω per line for longitudinal signals, as shown in Fig. 5c.

LINE FEED REGULATOR

The DC voltage between LA and LB will vary with the DC loop resistance. Unless the voltage supplied to the SLIC can be varied to match that on the line there will be a voltage drop across the chip along the path taken by the feed current. This could cause significant power dissipation. The purpose of the line feed regulator is to minimise this power dissipation by regulating the voltage supplied to the Line Amplifiers.

Regulated voltage is supplied to the Line Amplifiers on V_{REG} and unregulated voltage is supplied on V_{BB}. The chip switches V_{BB} onto +CH when more power is required at the V_{REG} pin. V_{REG} is the voltage used by the device to power the 2-wire interface, and it is adjusted to follow a reference voltage V_{REF} (from Power Feed). This reference voltage is determined as follows:

$$V_{REF} = -\{ | V_{DCT} | + V_{BIAS} \}$$

and is such to set V_{REG} to the minimum required to power the line interface. This then ensures a minimum power dissipation. The voltage V_{BIAS} is needed to keep the amplifier response linear when audio signals are transmitted.

Fig. 7 shows the external components associated with the power supply aspect of the voltage regulator. +CH is the positive terminal of the regulator switch that connects to V_{BB}. When the switch is turned on, current in L_1 and C_1 increases, thus increasing stored energy. When the switch turns off, this stored energy sustains L_1 current which flows in D_1. The voltage at +CH is thus a square wave of up to 50V p-p making this node sensitive to PCB layout. Note that the inductor should be capable of taking twice the line current without saturating. The regulator will work with a wide range of inductor resistance, although if this is too large, long line drive capability and regulator efficiency will be reduced. Since there are large current fluctuations from V_{BB} through the switch, C_2 provides filtering of the VBB pin, whilst D_2 isolates the V_{BAT} supply should the LA/LB pins be taken negative of the V_{BAT} supply.

The chip senses the voltage at V_{REG}, compares it to its requirements and switches power from V_{BB} to +CH, using the variable mark/space method, to give appropriate matching. The rate of switching can be governed by CHCLK (pin 10) or allowed to free run, its stability ensured by the network on CHS (pin 9) , i.e. C_3, R_1, C_5. Since noise is produced by the switching, a decoupling node is provided at SUB (pin 8).

CONTROL AND SIGNALLING

The mode of operation of the SL373 is determined by the Digital Interface pins, as described in Tables 1 and 2. These pins enable Ringing or Non-Ringing modes of operation, controlling line status, line polarity, Relay Driver and selection of line detector.

The line status is selected by use of the D2..D0 pins, Table 2, to determine the modes as listed. The function of these modes has already been described in the 'Overview' and 'DC Line Feed' sections; more detail of the device detectors is given here (refer to Fig. 8).

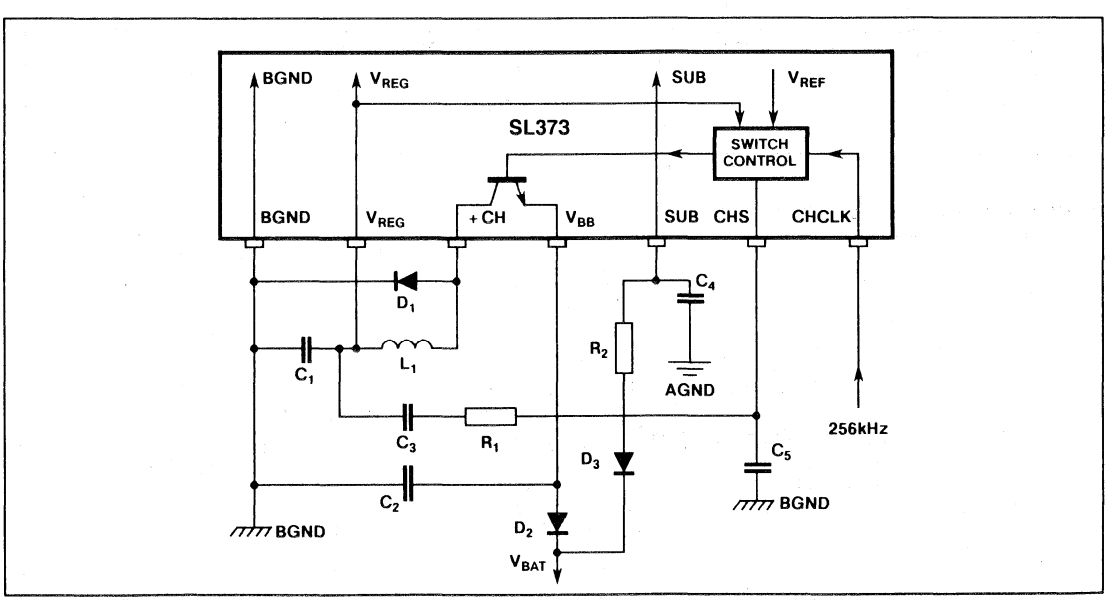


Fig.7 Voltage regulator power supply circuit.

Loop Detect

This detector is used in Active and Standby modes (with/without polarity reversal). The loop current at which the detector indicates the Off-Hook condition, is set by the comparator at pins 24 (RD) and 20 (V_{EE}). Normally a resistor, R_{TH}, is connected between these pins, such that Off-Hook line current threshold (I_{DET}) is set by:

$$I_{DET} = 350 \div R_{TH}$$

This is due to the fact that the current out of the RD pin is equal to the loop current $I_L = (\frac{1}{2}|I_A - I_B|)$ divided by ~280. This will create a voltage across R_{TH} at the RD pin. Off-Hook is given by a logic low at the $\overline{DET}$ output pin (detector selected) when this voltage rises above the internal 1.25V reference.

Ground Key Detector

This detector is selected by the E1 pin of the Digital Interface. It can be used in Active and Standby modes (with/without polarity reversal), as well as Disconnect A Standby B mode.

Operation of the detector is via an internal threshold and the longitudinal current $I_{LL} = I_A + I_B$ of the 2-wire loop. Ground Key detection is indicated when either the midpoint of the A and B legs is connected to ground, or the B leg (A leg, polarity reversed) is connected to ground. The resistance values for which Ground Key detection is valid are given in the Electrical Characteristics section.

Ring Trip Detector

This consists of a comparator connected to the DA and DB pins, and indicates Ring Trip when the voltage at DA < DB. Selection of Ringing mode operates the Ring Relay and enables the Ring Trip Detector. The external ringing supply must consist of DC line feed in addition to the AC ringing voltage. In order that the Ring Trip Detector senses Ring Trip in ringing mode, a resistance bridge network is used in association with pins DA, DB, line and ring source. This network is described in the Applications section and discussed further in AN82.

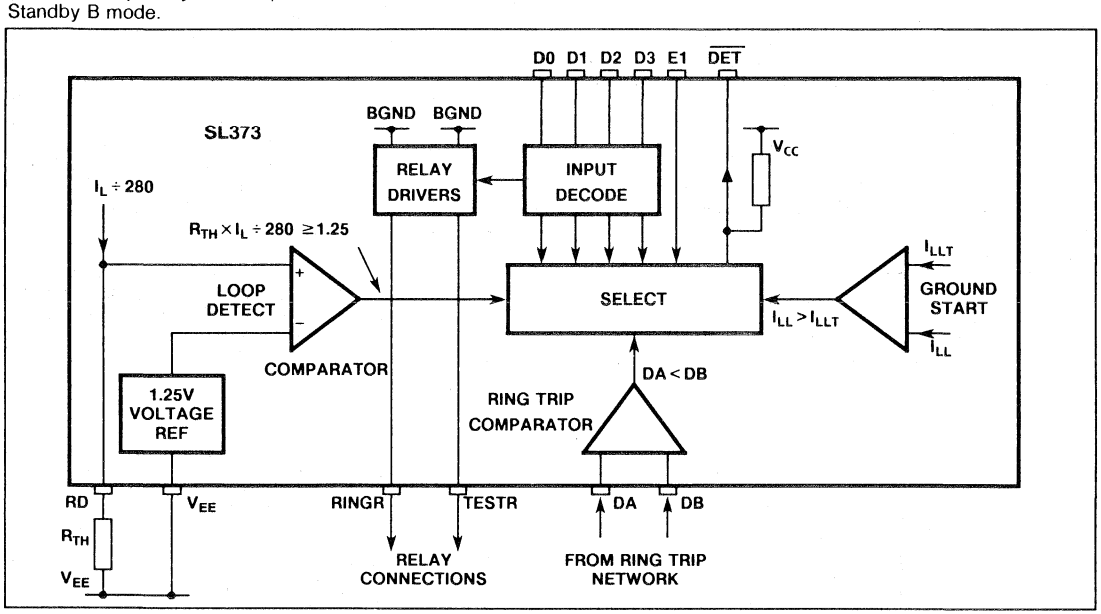


Fig.8 Detector circuits.

FUNCTIONAL PARAMETER SUMMARY

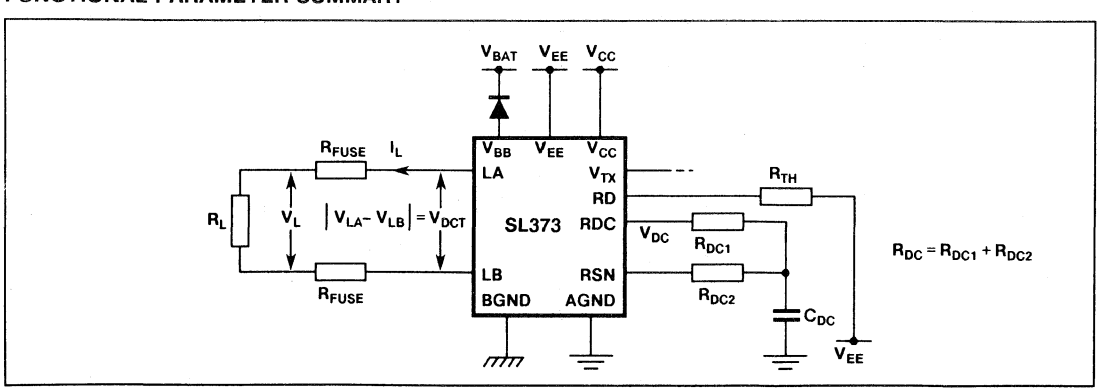


Fig.9 DC parameters and components for the SL373

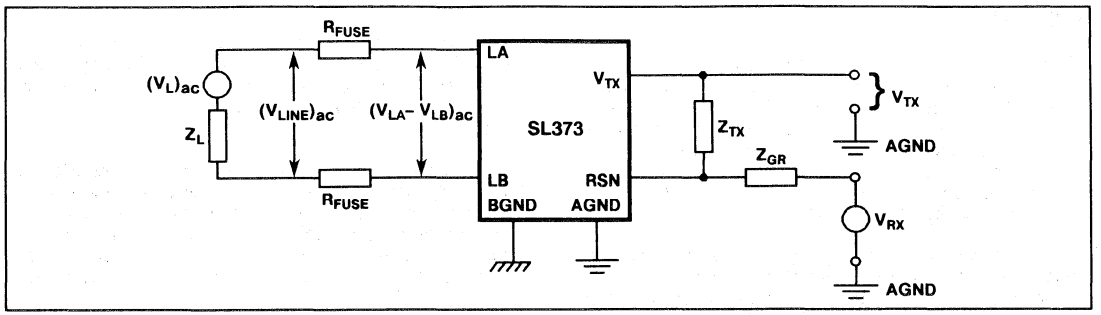


Fig.10 AC parameters and components for the SL373

LIST OF DEFINITIONS

1. Loop Current is defined as :- $I_L = \pm\frac{1}{2}|I_A - I_B|$

   I_A = current out of LA pin, I_B = current out of LB pin, + ⇒ normal line polarity and –⇒ reverse line polarity.

2. Longitudinal Current is defined as :- $ILL = (I_A + I_B)$

   I_A = current out of LA pin, I_B = current out of LB pin

3. Normal Line Feed Region when $|V_{BAT}|-|V_{DCT}| > V_{SG}$ with $I_L = I_{FEED} = (2500 \div R_{DC})$

4. Saturation Guard Threshold when $|V_{BAT}|-|V_{DCT}| = V_{SG} = 15.0V$ such that :-

   $V_L = V_{LSG} = |V_{BAT}|-V_{SG}-[2R_{FUSE} \times (2500 \div R_{DC})]$ which will equal $|V_{BAT}|-V_{SG}$ with $2R_{FUSE} = 0$ and
   $R_{LSG} = [(|V_{BAT}|-V_{SG}) \times (R_{DC} \div 2500)]-[2R_{FUSE}]$

5. Saturation Guard feed Region when $|V_{BAT}|-|V_{DCT}| < V_{SG}$ with $I_L = [|V_{BAT}|-V_{SG}] \div [R_L + 2R_{FUSE}]$

6. Note that V_{LSG} is referred to as the value of the line voltage, V_L, at the point where Saturation Guard becomes active. This will differ from the value of $|V_{LA}-V_{LB}|$ (i.e. V_{DCT}) if $2R_{FUSE} \neq 0$. V_{SG} is used as a notional threshold voltage which is the internal headroom between the $|V_{LA}-V_{LB}|$ voltage and the battery supply, at this same point.

7. Open Circuit Line Voltage V_{LOC} at $R_L = \infty\Omega$ such that :- $V_L = V_{LOC} \approx [|V_{BAT}|-V_{SG}]$

   V_{LOC} will be $\geq V_{LSG}$ even with $2R_{FUSE} = 0$. The voltage drop from V_{LOC} to the defined V_{LSG} point will be greater at lower values of V_{BAT}.

8. Standby Mode DC Feed Current $I_L \leq I_{LIM} = K_{LIM} \times I_{DET} \approx 600 \div R_{TH}$

9. 2 Wire Termination Impedance $Z_{AB} = (Z_{TX} \div \alpha) = (Z_{TX} \div 1000)$

   Note that Z_{TX} is normally set to $[\alpha(Z_L + 2R_{FUSE})]$ where Z_L is the desired termination impedance.

10. Recieve Gain from V_{RX} to $(V_{LA}-V_{LB})_{ac}$ or $(V_{LINE})_{ac}$ is set by Z_{GR} after setting Z_{TX}. Thus, with $(V_L)_{ac} = 0$:-

    $\frac{(V_{LA}-V_{LB})_{ac}}{V_{RX}} = \frac{-\alpha Z_L Z_{TX}}{[\alpha(Z_L) + Z_{TX}]Z_{GR}}$ with $2R_{FUSE} = 0$; $\frac{(V_{LINE})_{ac}}{V_{RX}} = \frac{-\alpha Z_L Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]Z_{GR}}$ with $2R_{FUSE} \neq 0$

11. Resultant Transmit Gain is then :- $\frac{V_{TX}}{(V_L)_{ac}} = \frac{Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]}$ with $V_{RX} = 0$

12. Resultant 4 Wire-4 Wire Gain is then :- $\frac{V_{TX}}{V_{RX}} = \frac{-\alpha(Z_L + 2R_{FUSE})Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]Z_{GR}}$ with $(V_L)_{ac} = 0$

13. Off-Hook Threshold is set by R_{TH} at :- $I_L = I_{DET} = 350 \div R_{TH}$

14. Ring Trip Threshold is set by the bridge associated with pins 25 .. 28 and the 2 Wire Line, thus :-

    $R_L = R_{LTH} = R_{B4}(2R_F) \div (R_{B4}-R_{B1})$ assuming $R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$ and $R_{FEED1} = R_{FEED2}$ for the bridge components (balanced ringing). $R_{B1}..R_{B4}$ ≈ a few 100KΩ and R_{FEED1} ≈ a few 100Ω.

15. AC ringing voltage at DA (DB by the same amount) is reduced by a factor of :- $[1 + (2\pi f_r t_r)^2]^{-\frac{1}{2}}$

    f_r is the ringing frequency and t_r is determined by the bridge components including C_B, thus :- $t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$

    for Balanced Ringing.

APPLICATIONS

The requirements for the subscriber line interface vary considerably from one telephone administration to another. The SL373 is designed to have the flexibility to meet these varying requirements. For simplicity, only a single example is given to illustrate how the device is connected. Fig. 11 shows the circuit which can be used to evaluate the device. Further applications information is given in the SL373/SL376 Application Note AN82 (page 7-18).

The DA and DB pins are connected to a resistance bridge network (R_{B3} to R_{B4}). This allows the change in line resistance to be sensed when the remote telephone goes off-hook during ringing (Ring Trip). The details of this network (and C_B) are given later (see Ring Trip section). The resistors R_{FEED1} and R_{FEED2} provide feeding of the ringing source onto the line during ringing mode. The Ring and Test Relay Drives are connected through current limiting resistors.

Connections to the LA and LB pins are shown, and include the resistors R_{FUSE} in addition to the ring relay. These resistors have a value around 20 to 30 ohms, depending on the application, and provide current line protection.

Overvoltage and protection circuitry may consist of slew-limiting inductors between the pins and the line itself and a thyristor or zener protection network at the line. In many applications, especially in PBXs, the amount of protection circuitry can be reduced. The capacitors between LA, LB and ground, allow noise from the regulator to be decoupled.

The capacitor C_{HP} between HPA and HPB (pins 22 and 23) is used to filter out the AC component of the signal on the line. The voltage difference between the two pins should be effectively DC. The SL373/SL376 Application Note AN82 contains a further discussion on this

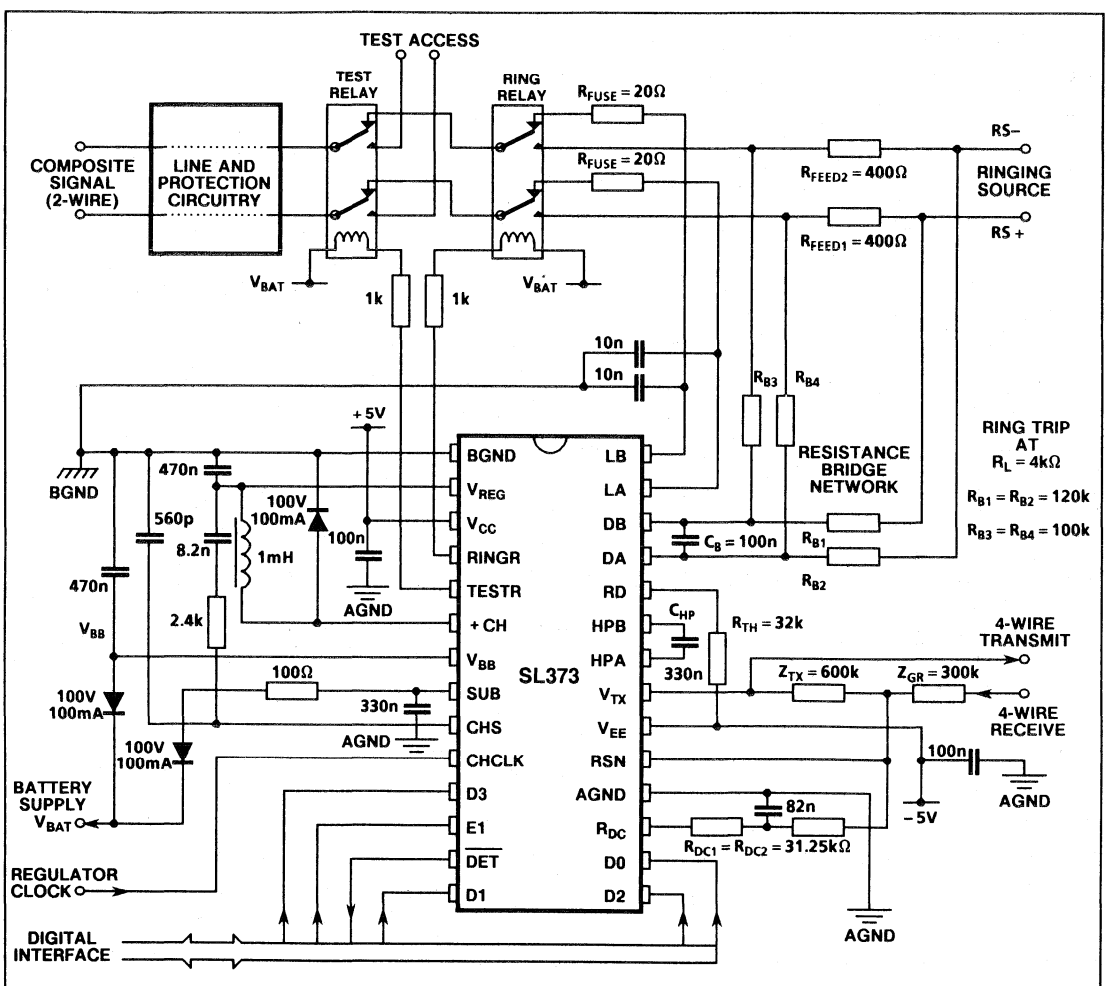


Fig. 11 Application circuit

The resistor, R_{TH}, between RD (Pin 24) and V_{EE} (pin 20) programs the threshold current for the loop detector. A capacitor in parallel can be added to reduce the effect of the AC component of the line current, but this can cause instability in standby operation with highly inductive lines if it is too large. The value of R_{TH} sets the current I_{DET} according to the relationship :

$$I_{DET} = 350 \div R_{TH}$$

The CHS pin (Pin 9) is connected to BGND through a capacitor and to V_{REG} by a capacitor and resistor in series. This stabilises the regulator control loop. Operation of the regulator has been described earlier in the Functional Description section (pins 2,6 & 7).

It is recommended that the substrate (SUB) pin be decoupled to AGND. However, BGND may be used if this is sufficiently quiet, otherwise some degradation in noise performance may be experienced.

DC current flows between the RDC (pin 17) and RSN (pin 19). This is used to set the line feed current. Any minor AC fluctuations are reduced by dividing the resistance RDC equally such that $R_{DC1} = R_{DC2} = \frac{1}{2}R_{DC}$ and connecting a capacitor from the junction of R_{DC1} and R_{DC2} to AGND.

The Receive Gain is set by the network (Z_{GR}) which controls the receive current flowing into RSN. This can be a complex impedance network to allow for complex impedance terminations.

The network (Z_{TX}) between V_{TX} and RSN controls the 2 wire terminating impedance (Z_T). This can also be a complex impedance. The value of Z_{TX} can be calculated from the relationship :-

$$Z_{TX} = (\text{Required } Z_T) \times (\text{Receive Current Gain})$$

Connections for both Ring and Test relays are also shown in Fig. 11. Note that the 1kΩ resistors provide current limit through the relay coils when the driver outputs are on.

Control and status pins are TTL compatible. They are designed to give a simple interface to digital circuits and are directly compatible with the MV3010 PSLAC.

RING TRIP

Ring Trip detection operates by comparing the voltages on DA and DB and providing the output on $\overline{DET}$ when this function is enabled by the status input pins of the Digital Interface. A resistance bridge (R_{B1} to R_{B4}) must be connected to the line and the ringing voltage sources to cause the differential voltage between DA and DB to change sign when the line resistance falls below the level associated with Ring Trip. Note that it is simplified by use of $R_{B1} = R_{B2}$ and $R_{B3} = R_{B4}$ (see discussion in AN82)

Ringing voltage is normally applied to the line through the Ring Relay which is activated by RINGR. The ringing voltage sources, including line feed, are connected to the line via ringing feed resistors, R_{FEED1} and R_{FEED2}. The resistance bridge operates by allowing the DC voltage dropped across the ringing feed resistors (R_F) in the Off-Hook condition to reverse the polarity of the voltage on DA and DB (DA < DB). Since the AC ringing voltage is greater than the DC feed, the capacitor C_B (Fig. 12) will filter this out at the comparator inputs. The connection shown is suitable for balanced ringing only. For unbalanced ringing, separate capacitors from DA (C_{B1}) and DB (C_{B2}) to ground will be required to achieve the same result.

Fig. 12 shows how the resistance bridge is connected when used with balanced ringing. The circuit can operate correctly provided there is a DC feed in addition to the AC ringing voltage.

If R_{LTH} is the line resistance corresponding to the Ring Trip threshold (DA = DB), this can be determined from the values of R_F ($R_{FEED1} = R_{FEED2} = R_F$), R_{B1} and R_{B4} ($R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$) as:-

$$R_{LTH} = \frac{R_{B4}(2R_F)}{(R_{B1} - R_{B4})}$$

R_{B1} and R_{B4} should be a few hundred kΩ.

The amplitude of the AC ringing voltage at DA (DB by the same amount) is reduced by a factor of $[1 + (2\pi f_r t_r)^2]^{-\frac{1}{2}}$ where f_r is the ringing AC frequency and t_r is set by:-

$$t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$$

for balanced ringing. For $f_r \approx 20$Hz, t_r should be ≈ 50ms. For unbalanced ringing C_B will become $C_{B1}C_{B2} + (C_{B1} + C_{B2})$ in the above equation. More detail on Balanced and Unbalanced ringing is given in AN82.

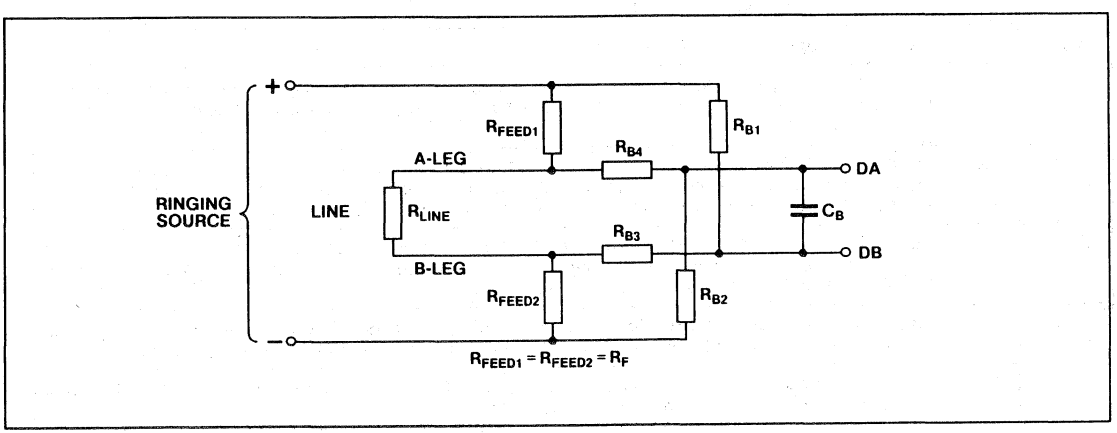


Fig. 12 Ring trip circuit (balanced ringing).

PIN DESCRIPTIONS

Symbol	Pin no.	Pin name and description
BGND	1	**Battery Ground (Power Input).** 0 Volts.
V_{REG}	2	**Regulated Voltage (Negative Power Input).** The voltage at this pin is compared to that required for line feed, and the result is used to control the voltage regulator.
V_{CC}	3	**Positive Supply (Power Input).** +5 Volts.
RINGR	4	**Ring Relay Driver Output (Pull-up Output).** This output is designed to drive a relay, when used together with the V_{BAT} supply.
TESTR	5	**Test Relay Driver Output (Pull-up Output).** This output is designed to drive a relay, when used together with the V_{BAT} supply.
+CH	6	**Switching Regulator (Chopper) Output (Negative Power Output).** Chopper switch transistor collector. An internal regulator controls the mark/space ratio of the switching waveform to maintain V_{REG} (pin 2) at the required voltage.
V_{BB}	7	**Battery Voltage (Negative Power Input).** This is the –50 Volt battery supply pin which connects to the V_{BAT} supply via an external diode. It is connected to the chopper switch emitter.
SUB	8	**Substrate (Decoupling Node).** An external decoupling capacitor (0.33µF) should be connected between this pin and AGND.
CHS	9	**Line Feed Regulator (Chopper) Stabilising Network.** This is the input to the voltage comparator which is used to control the switching regulator.
CHCLK	10	**Line Feed Regulator (Chopper) Clock (Digital Input).** This is the positive edge triggered, 256kHz clock input for the voltage regulator, which will free run in the absence of an input signal.
D3	11	**Control Input (Digital Input).** Enables the Test relay driver output pin.
E1	12	**Control Input (Digital Input).** Selects the line status detector (Loop or Ground Key).
$\overline{DET}$	13	**Detector Data output (Digital Output).** This pin outputs the status of the detector which has been selected by D0 - D3.
D1 D2 D0	14 15 16	**Control Input (Digital Input)** **Control Input (Digital Input)** **Control Input (Digital Input)** — These inputs determine the SLIC operating mode, and control the ring relay, selection of ringing and non-ringing modes, line polarity, line status and line detector.
RDC	17	**DC Reference Voltage (Voltage Output).** A reference voltage of ±2.5 Volts (± depending on line polarity), is output at this pin, excepting Saturation Guard operation.
AGND	18	**Analog Ground (Analog Reference Node).** This is the ground reference pin for the analog signals. It also provides a ground reference for the Digital Interface. Signal reference and decoupling connections should be separately run to this pin.
RSN	19	**Receive Summing Node (Current Input).** The current which is input on this pin is used to control the transverse current at LA and LB.
V_{EE}	20	**Negative Supply (Power Input).** – 5 Volts.
V_{TX}	21	**Transmit Voltage (Voltage Output).** The voltage output at this pin is equal to the difference between the voltage (V_{LA}–V_{LB}) and the differential DC voltage (V_{HPA}–V_{HPB}), multiplied by the 2 to 4 wire voltage gain.
HPA HPB	22 23	**High Pass A, High Pass B - AC/DC separation (Voltage Inputs).** These inputs sense the DC feed voltages on the LA and LB pins respectively. Under normal operation they are connected to LA and LB respectively by internal resistors and should be connected as shown in Fig. 11.
RD	24	**Loop Detection Control (Current Output / Voltage Input).** This pin outputs a current which equals the transverse loop current through LA and LB divided by 280. Off-Hook is indicated via the $\overline{DET}$ pin when the voltage at this pin is $\geq(V_{EE}+1.25)$ Volts.
DA DB	25 26	**Ring Trip Detector A, Ring Trip Detector B (Voltage Inputs).** These are the A and B inputs to the internal ring trip comparator. The output of the comparator controls the ring trip output on $\overline{DET}$.
LA LB	27 28	**A Line Transceiver, B Line Transceiver (Current Outputs / Voltage Inputs).** These two pins form the 2 wire port connecting to the subscriber loop.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Range - see page 3-21)

Test conditions (unless otherwise stated)

V_{CC} = +5.0V, V_{EE} = –5.0V, V_{BAT} = –50V (see note 3), $V_{AGND} = V_{BGND}$, T_{AMB} = +25°C, V_{IL} = 0.7V and V_{IH} = 2.0V. Test circuit Fig. 24. Voltages are measured with respect to analog ground (V_{AGND}). Typical figures are for design aid only; they are not guaranteed and are not subject to production testing.

Supply Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply (V_{CC}) current, disconnect mode	I_{CC1}			4	mA	
Positive supply (V_{CC}) current, standby mode	I_{CC2}			10	mA	On / Off-Hook, $I_L = 0$
Positive supply (V_{CC}) current, active mode	I_{CC3}			10	mA	On / Off-Hook, $I_L = 0$
Negative supply (V_{EE}) current, disconnect mode	I_{EE1}			2	mA	
Negative supply (V_{EE}) current standby mode	I_{EE2}			3	mA	On / Off-Hook, $I_L = 0$
Negative supply (V_{EE}) current active mode	I_{EE3}			3	mA	On / Off-Hook, $I_L = 0$
Battery supply (V_{BB}) current disconnect mode	I_{BB1}			1	mA	
Battery supply (V_{BB}) current standby mode	I_{BB2}			5	mA	On-Hook, $I_L = 0$
Battery supply (V_{BB}) current active mode	I_{BB3}			6	mA	On-Hook, $I_L = 0$
Positive supply (V_{CC}) rejection ratio (supply to 2-wire transverse)	P_{SRT}		17		dB	See notes 1 & 2; 50mV on supply, 300-3400Hz, $Z_L = 600\Omega$
Positive supply (V_{CC}) rejection ratio (supply to 2-wire longitudinal)	P_{SRL}		17		dB	See notes 1 & 2; 50mV on supply, 300-3400Hz, $Z_L = 600\Omega$
Negative supply (V_{EE}) rejection ratio (supply to 2-wire transverse)	N_{SRT}		17		dB	See notes 1 & 2; 50mV on supply, 300-3400Hz, $Z_L = 600\Omega$
Negative supply (V_{EE}) rejection ratio (supply to 2-wire longitudinal)	N_{SRL}		17		dB	See notes 1 & 2; 50mV on supply, 300-3400Hz, $Z_L = 600\Omega$
Battery supply (V_{BB}) rejection ratio (supply to 2-wire transverse)	B_{SRT}		27		dB	See notes 1 & 2; 50mV on supply, 300-3400Hz, $Z_L = 600\Omega$
Battery supply (V_{BB}) rejection ratio (supply to 2-wire longitudinal)	B_{SRL}		27		dB	See notes 1 & 2; 50mV on supply, 300-3400Hz, $Z_L = 600\Omega$
Power dissipation, active state	P_{WA}			1.00	W	$Z_L = 600\Omega$
Power dissipation, standby state, on-hook	P_{WD1}			0.35	W	$I_L = 0$

NOTES

1. Non production test; figures are guaranteed by characterisation.
2. Figures will degrade when saturation guard is active, i.e. when $|V_{BAT}| - |V_{DCT}| < V_{SG}$. V_{DCT} is voltage between pins LA and LB and $V_{SG} \approx 15.0V$.
3. Battery voltage V_{BAT} is generally defined. The corresponding V_{BB} voltage is assumed to be 0.7V more positive than V_{BAT} allowing for the diode drop in D_2, see Fig. 24.

Analog Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
2-wire port, low frequency overload level	V_{OAB}	– 3.1		+ 3.1	V (pk)	Refer Fig. 13, note 4: V_R = 1000 Hz, E_L = 0V
2-wire port,longitudinal impedance	Z_{LL}			35	Ω/wire	Refer Fig. 14: f < 100 Hz Z_L = 600Ω
Longitudinal current limit, active state	I_{LLA}	17.5			mA/wire (rms)	Refer Fig. 15, note 5: E_R = – 10dBm 700-1100Hz, Z_L = 600Ω
Longitudinal current limit, standby state	I_{LLS}	3.6			mA/wire (rms)	Refer Fig. 15, note 5: E_R = – 10dBm 700-1100Hz, Z_L = 600Ω
Longitudinal current limit, active state, B leg	I_{LLB}	63			mA	I_{LLB} is Current in B leg with B leg = 0V and A leg O/C
4-wire transmit port, overload level	V_{OT}	– 3.1		+ 3.1	V (pk)	Refer Fig. 13, note 4: f = 1000 Hz, V_R = 0V 4-wire load ≥ 25kΩ
4-wire transmit port, offset voltage	V_{TOFF}	– 30		+ 30	mV	Refer Fig. 13: V_R = 0
4-wire transmit port,output impedance	Z_T			20	Ω	Refer Fig. 13: E_L = 0V
Transmit (2 to 4-wire) voltage gain	G_T	– 0.1		+ 0.1	dB	Refer Fig. 13: E_L = 0dBu (see note 6), 1kHz, V_R = 0
4-wire receive port, low frequency voltage gain	G_{RL}	– 0.2		+ 0.2	dB	Refer Fig. 16: V_R = 2.6dBu, 1kHz
4-wire receive port, current gain	G_{RI}	59.8	60.0	60.2	dB	Refer Fig. 13:
4 to 4-wire voltage gain	$G_R \times G_T$	– 0.2		+ 0.2	dB	Refer Fig. 16: R3 = 600kΩ, V_R = 2.6dBu, 1000Hz
2-wire to 4-wire frequency response	F_{24}	– 0.1		+ 0.1	dB	Refer Fig. 13, note 7: V_R = 0, E_L = 0dBu, 200-3400Hz,
4-wire to 2-wire frequency response	F_{42}	– 0.1		+ 0.1	dB	Refer Fig. 13, note 7: E_L = 0, V_R = 0dBu, 200-3400Hz
4 to 4-wire frequency response	$F_{44} = F_{24} \times F_{42}$	– 0.1		+ 0.1	dB	Refer Fig. 13, note 7: E_L = 0, V_R = 0dBu, 200-3400Hz
Gain linearity, 2-wire to 4-wire	G_{L24-1}	– 0.1		+ 0.1	dB	Refer Fig. 13, note 8: V_R = 0, E_L = + 7 to – 30 dBu, 1kHz
Gain linearity, 2-wire to 4-wire	G_{L24-2}	– 0.1		+ 0.1	dB	Refer Fig. 13, note 1: V_R = 0, E_L = –30 to – 59 dBu, 1kHz
Gain linearity, 4-wire to 2-wire	G_{L42-1}	– 0.1		+ 0.1	dB	Refer Fig. 13, note 8: E_L = 0, V_R = + 3 to –30 dBu, 1kHz
Gain linearity, 4-wire to 2-wire	G_{L42-2}	– 0.1		+ 0.1	dB	Refer Fig. 13, note 1: E_L = 0, V_R = –30 to –64 dBu, 1kHz

NOTES
4. Overload occurs when distortion is 2% of total signal in the range 300-3400Hz.
5. E_{LL} = 50Hz. Amplitude of I_{LL} when signal-to-distortion ratio at $V_T \leq 30$dB.
6. dBu is defined thus: 0dBu is equivalent to the voltage at 0dBm when loaded with 600Ω ($0.775V_{RMS}$).
7. Response is measured with respect to 1kHz.
8. Linearity is measured with respect to gain at 0dBu.

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
4-wire idle channel noise (psophometric weighted)	N_{P4}			-75.0	dBup	Refer Fig. 13: $E_L = V_R = 0V$
2-wire idle channel noise (psophometric weighted)	N_{P2}			-75.0	dBup	Refer Fig. 13: $E_L = V_R = 0V$
2-wire differential noise (wide band)	N_{D2}		Fig. 19			Refer Fig. 13, note 1; $E_L = V_R = 0V$
2-wire longitudinal noise (wide band)	N_{L2}		Fig. 20			Refer Fig. 18, note 1; $E_R = 0V$
Regulator noise, 4-wire receive, single frequency	N_{R4}			-55.0	dBu	Refer Fig. 21, note 1
Regulator noise, 2-wire transverse, single frequency.	N_{RT}			-50.0	dBu	Refer Fig. 21, note 1; measure V_{A-B}.
Regulator noise, 2-wire longitudinal, single frequency.	N_{RL}			-50.0	dBu	Refer Fig. 21, note 1; measure V_{LL}.
Longitudinal balance, longitudinal to transverse	B_{L-T1}	50	60		dB	Refer Fig. 14, note 11: $Z_L = 600\Omega, V_R = 0$, E_{LL} = +2dBu 40-4000Hz
Longitudinal balance, longitudinal to transverse	B_{L-T2}	35.5 40.0 45.0	40.0 45.0 50.0		dB dB dB	Ref Fig. 14: $V_R = 0, Z_L = 1.6k\Omega$ E_{LL} = +2dBu 40-400Hz E_{LL} = +2dBu 400-1000Hz E_{LL} = +2dBu 1000-4000Hz
Longitudinal balance, transverse to longitudinal + longitudinal to transverse	B_{T-L+} B_{L-T1}	98			dB	Refer Fig. 14 & Fig. 17: $Z_L = 600\Omega, V_R = 0$, E_{LL} = +2dBu 300-800Hz
Longitudinal balance, transverse to longitudinal + lonitudinal to transverse	B_{T-L+} B_{L-T2}	90			dB	Refer Fig. 14 & Fig. 17: $Z_L = 1600\Omega, V_R = 0$, E_{LL} = +2dBu 300-800Hz
Longitudinal signal rejection, longitudinal to 4-wire	$RJ_{L4\ A}$	50	60		dB	Refer Fig. 14: $Z_L = 600\Omega, V_R = 0$, E_{LL} = +2dBu 40-4000Hz
Longitudinal signal rejection, longitudinal to 4-wire	$RJ_{L4\ BL}$ $RJ_{L4\ BH}$	35 45	40 50		dB dB	Refer Fig. 14: $Z_L = 1600\Omega, V_R = 0$, E_{LL} = +2dBu 40-300Hz E_{LL} = +2dBu 300-4000Hz
Longitudinal signal generation, 4-wire to longitudinal	GN_{4-L}	40			dB	Refer Fig. 18; Z_L = 600 or 1.6kΩ E_R = 2.6dBu 300-800Hz,
Harmonic distortion, 4 to 2-wire	T_{HD1}			-50.0	dB	Refer Fig. 13, note 9: V_R = 0dBu, 1000Hz
Intermodulation distortion	ID_{A-B1}			-40.0	dB	Refer Fig. 13, note 10: $V_R = f_1 + f_2$, $f_1 = f_2 = -4$ to -21dBu
50Hz intermodulation distortion	ID_{A-B2}			-49.0	dB	Refer Fig. 13, note 1: $V_R = f_1 + f_2$, f_1 = -9dBu 300-3400Hz, f_2 = -23dBu 50Hz

NOTES
9. Distortion measured in the bandwidth 300-3400Hz.
10. f_1 & f_2 in the range 300-3.4kHz, $f_1 + f_2$ = Non-integer. Measure $(2f_1-f_2)$ relative to f_1 or f_2 level.
11. Parameter will degrade for some values of V_{BAT}

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Loop current, active state constant current region	I_{ACT1}	38	40	42	mA	Refer Fig. 24, note 12 : $Z_L = 600\Omega, R_{DC} = 62.5k\Omega$
Loop current, active state	I_{ACT2}	23			mA	Refer Fig. 24, note 12 : $Z_L = 2k\Omega, R_{DC} = 62.5k\Omega$
Loop current limit conversion factor K_{LIM} (see DC line feed section)	K_{LIM}	1.25		1.70	-	Standby mode
2-wire current, disconnected state	I_{DCT}			1.0	mA	LA to LB or Ground, or both LA and LB to Ground
2-wire current, disconnect A standby B mode	I_{DASB}			1.0	mA	$Z_L = 600\Omega$
Loop current, standby state, normal(+) or reverse(−)	I_{LIM}	14.7	17.3	22.0	(±)mA	Refer Fig. 24, note 13: $Z_L = 600\Omega$
Regulator voltage, pin 2	V_{REG1}	− 31.1 − 38.3		 − 32.2 − 39.1	V V V V	V_{LA}-V_{LB} = 18.9 Refer to V_{LA}-V_{LB} = 22.5 Fig. 13; V_{LA}-V_{LB} = 26.9 V_{BAT} = −63V V_{LA}-V_{LB} = 30.5
Loop detector, current threshold	I_{TH}	I_{TH} − 15%	I_{TH}	I_{TH} + 15%	A	Refer Fig. 24 : $I_{TH} = 350 \div R_{TH}$
Ring trip detector offset voltage	V_{RTO}	− 50		+ 50	mV	Refer Fig. 22 : R = 200kΩ $V_{BB} < V_{CMM} < -2V$
Ring trip detector bias current	I_{RTB}	−1.0			µA	Refer Fig. 22 : $I_{RTB} = \frac{1}{2}(I_{RTDA} + I_{RTDB})$
Ground key active mode $\overline{DET} = 0$	R_{G10}			900	Ω	Refer Fig. 23, note 14: SW1 Closed, RW = 300Ω
Ground key active mode $\overline{DET} = 1$	R_{G11}	10			kΩ	Refer Fig. 23, note 14: SW1 Closed, RW = 300Ω
Earthcall active mode $\overline{DET} = 0$	R_{G20}			1.7	kΩ	Refer Fig. 23, note 14: SW1 Open, RW = 300Ω
Earthcall active mode $\overline{DET} = 1$	R_{G21}	10			kΩ	Refer Fig. 23, note 14: SW1 Open, RW = 0Ω
Earthcall disconnect A standby B mode, $\overline{DET} = 0$	R_{G30}			1.7	kΩ	Refer Fig. 23, note 14: SW1 Open, RW = 300Ω
Earthcall disconnect A standby B mode, $\overline{DET} = 1$	R_{G31}	10			kΩ	Refer Fig. 23, note 14: SW1 Open, RW = 0Ω
Relay drivers, saturation voltage (active)	V_{SAT}	− 2			V	I = 25mA Connected to BGND
Relay drivers, leakage current (non-active)	I_{LK}			0.1	mA	V_{OUT} = Voltage at pin 8
Relay drivers, clamp voltage	V_{CLMP}	V_{BAT} − 2.0			V	I = 25mA into pin 4 or 5

NOTES
12. Applied $V_{BAT} = -63V$.
13. Constant current in Standby mode approximately $600 \div R_{TH}$.
14. For Polarity Reversed State, connections to LA and LB are reversed.

Digital Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Input low voltage (D_0-D_3, E_1, CHCLK)	V_{IL}			0.7	V	
Input high voltage (D_0-D_3, E_1, CHCLK)	V_{IH}	2.0			V	
Input low current (D_0-D_3, E_1, CHCLK)	I_{IL}			–0.25	mA	V_{IL} = 0.4V
Input high current (D_0-D_3, E_1, CHCLK)	I_{IH}			0.04	mA	V_{IH} = 2.4V
$\overline{DET}$ output low voltage	V_{OL}			0.4	V	I_{OL} = 0.8mA
$\overline{DET}$ output high voltage	V_{OH}	2.4			V	I_{OH} = 0.1mA
$\overline{DET}$ output, internal pull-up	R_{OUT}	10		20	kΩ	
Propagation delay, E_1 to $\overline{DET}$	t_{PD}			4	μs	$\overline{DET}$ 6.2kΩ to V_{CC}, 15pF to BGND
Loop detector make response time	t_{LM}			5	ms	Z_L = 2kΩ (V_{OL} < 0.45)
Loop detector break response time	t_{LB}			10	ms	Z_L = 2kΩ (V_{OL} > 2.35)
CHCLK input frequency	F_{CLK}		256		kHz	
CHCLK input minimum pulse width	T_{CLK}		500		ns	

Recommended Operating Range

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply voltage	V_{CC}	+4.75	5.0	+5.25	V	
Negative supply voltage	V_{EE}	– 4.75	– 5.0	– 5.25	V	
Battery supply voltage	V_{BAT}	– 40.5	– 48	– 64	V	
Battery ground voltage	V_{BGND}	– 0.1		+0.1	V	
Ambient temperature	T_{AMB}	0		+70	°C	

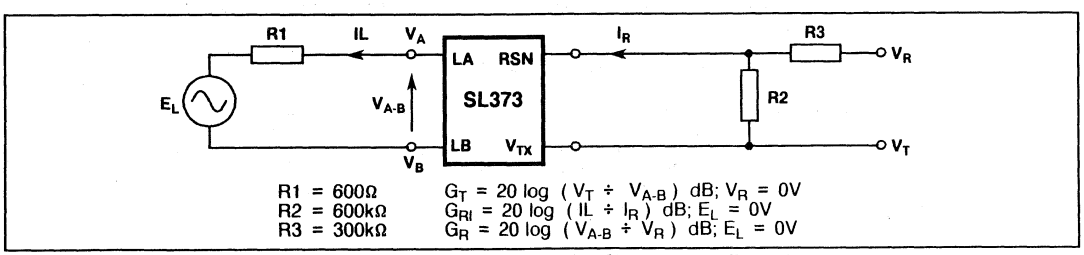


Fig.13 Test configuration (Note the SL373 block = Fig. 24).

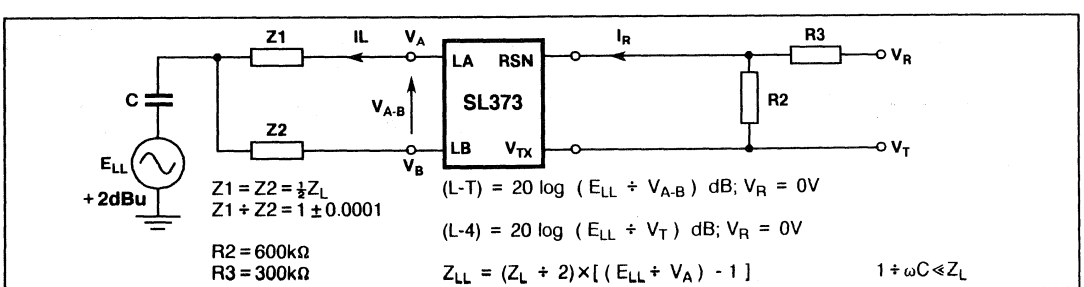


Fig.14 Test configuration (Note the SL373 block = Fig. 24).

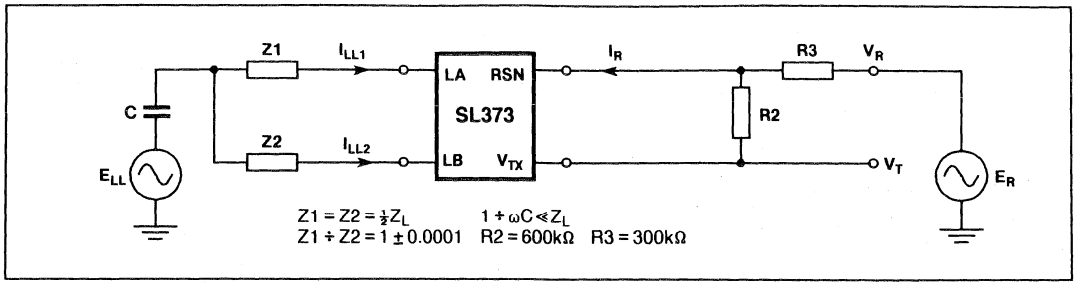


Fig.15 Test configuration (Note the SL373 block = Fig. 24).

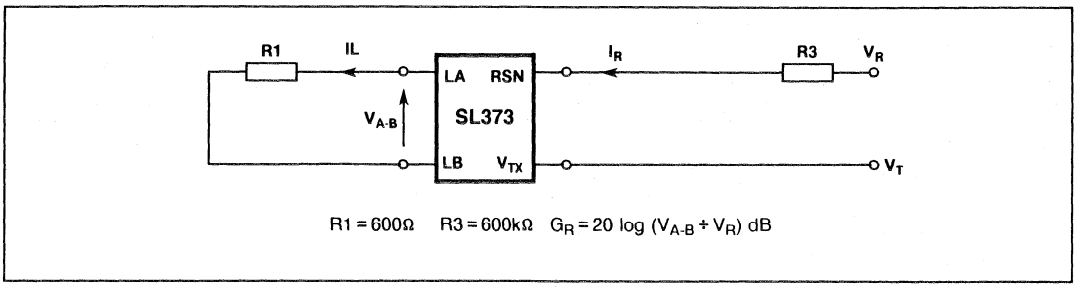


Fig.16 Test configuration (Note the SL373 block = Fig. 24).

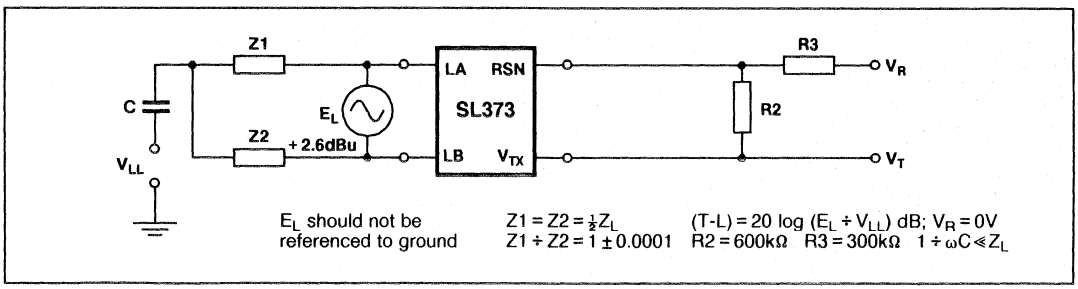


Fig.17 Test configuration (Note the SL373 block = Fig. 24).

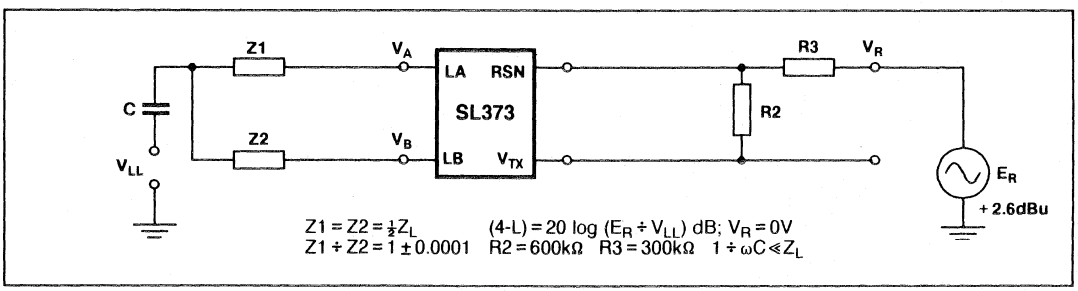
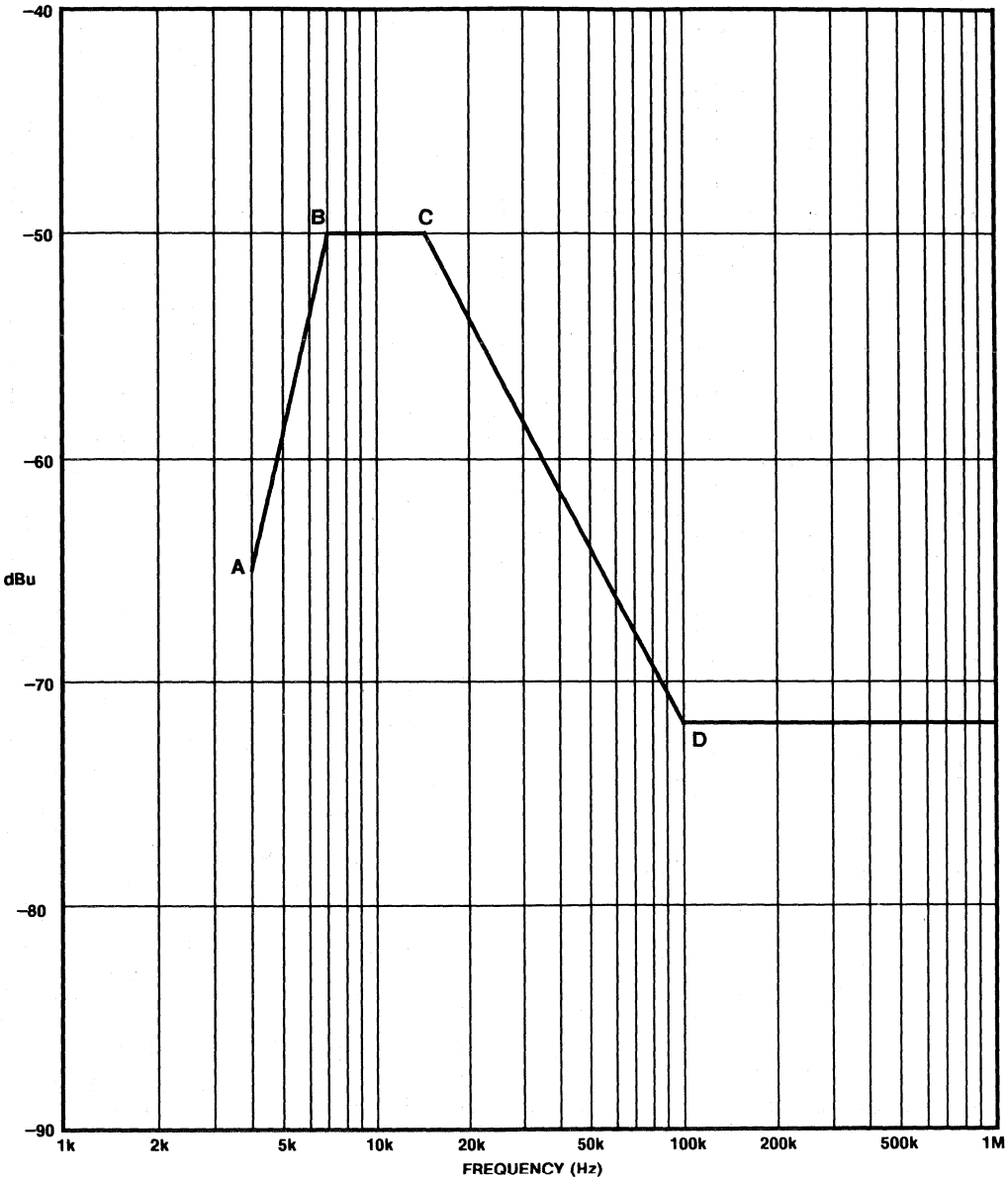


Fig.18 Test configuration (Note the SL373 block = Fig. 24).



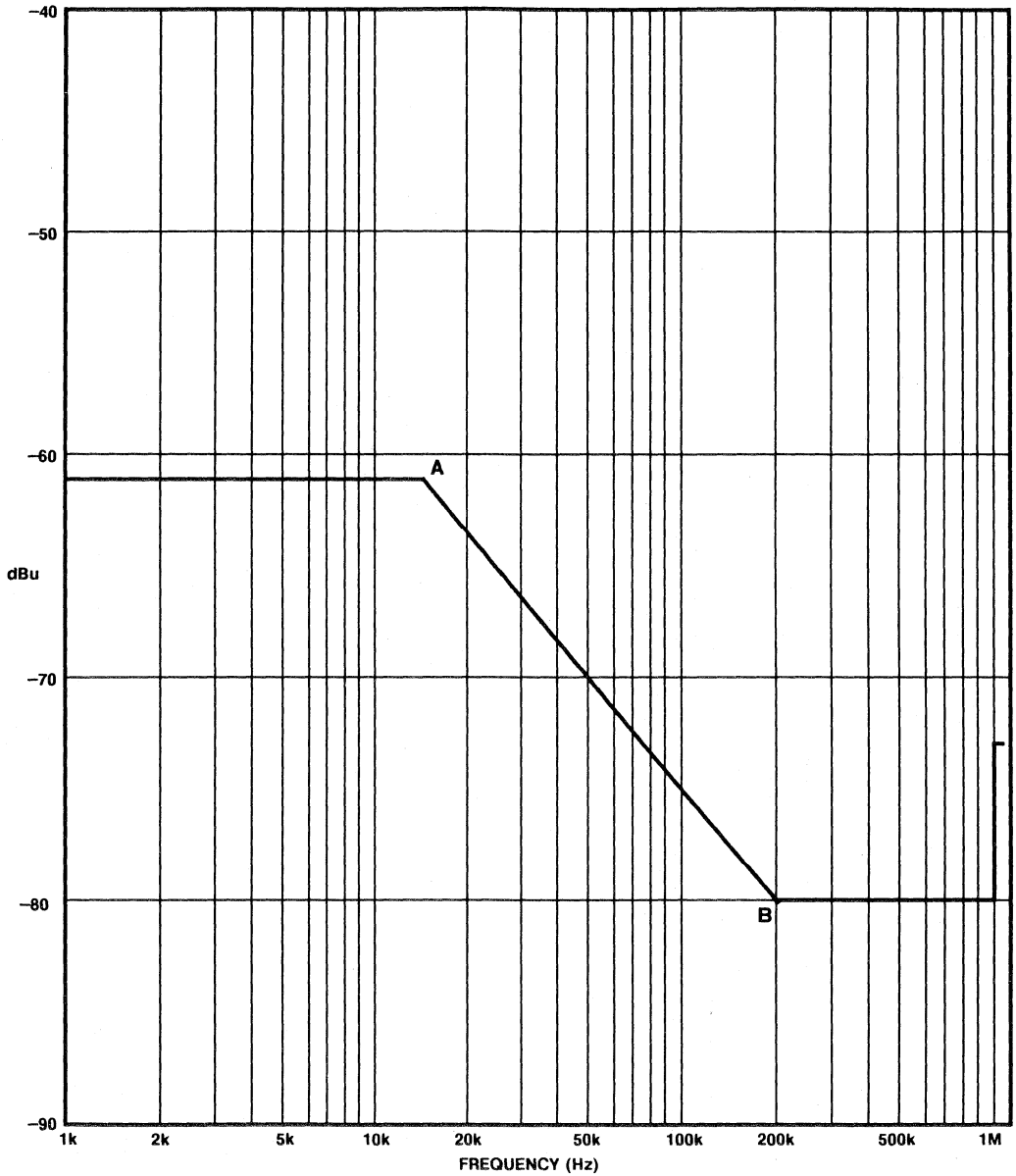
FREQUENCY AT CENTRE OF BAND

A = 4kHz	-65dBu	C = 15kHz	-50dBu
B = 7kHz	-50dBu	D = 100kHz	-73dBu

Bandwidth = 3kHz Minimum Centre Frequency = 1.6kHz

V_{A-B} < -73dBu. f > 1MHz

Fig.19 2-Wire differential noise



FREQUENCY AT CENTRE OF BAND

A = 15kHz –61dBu
B = 200kHz –80dBu
Bandwidth = 3kHz
V_{LL} < –73dBu. f > 1MHz

Fig.20 2-Wire longitudinal noise

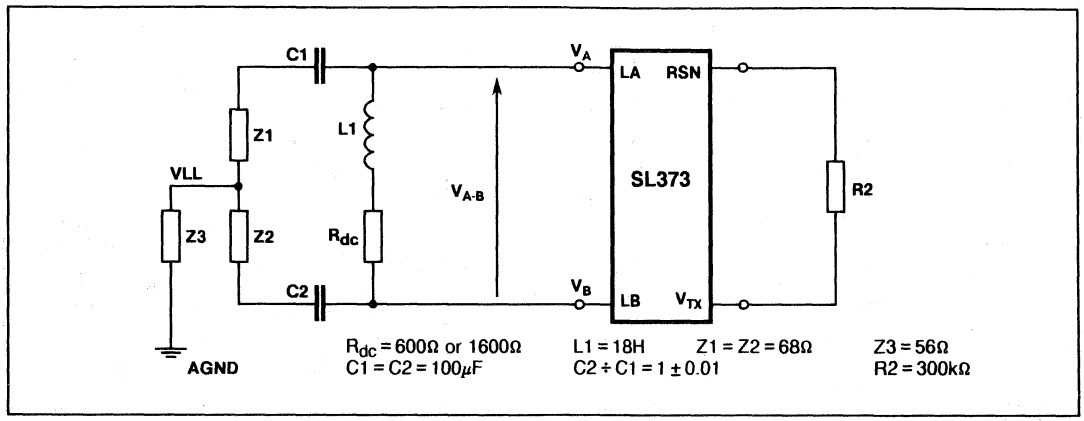


Fig.21 Test configuration (Note the SL373 block = Fig. 24)

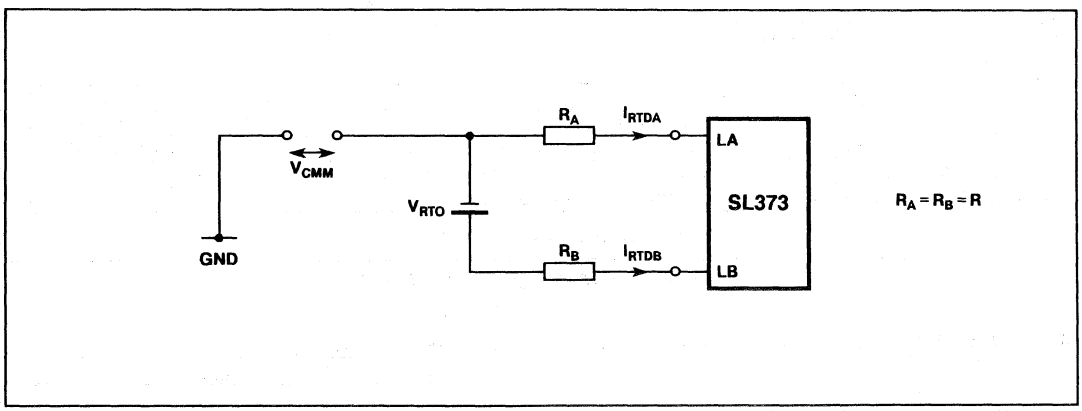


Fig.22 Test configuration (Note the SL373 block = Fig. 24)

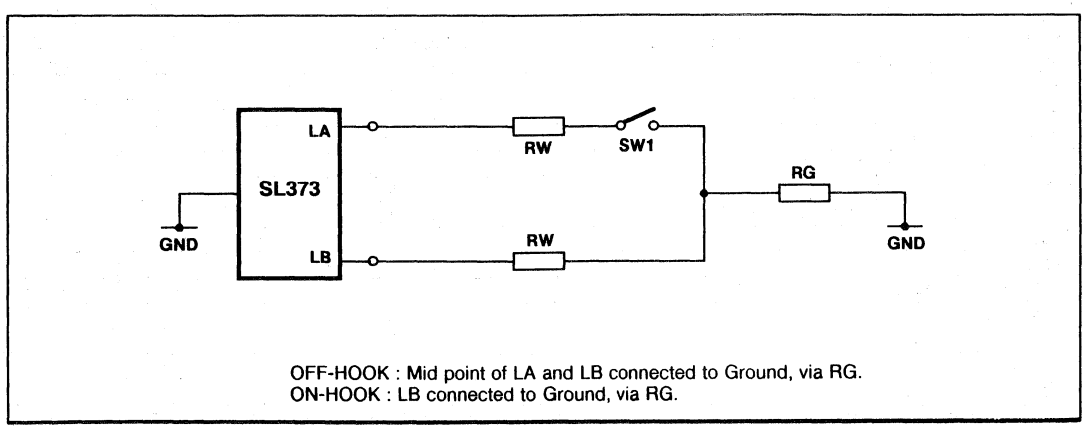
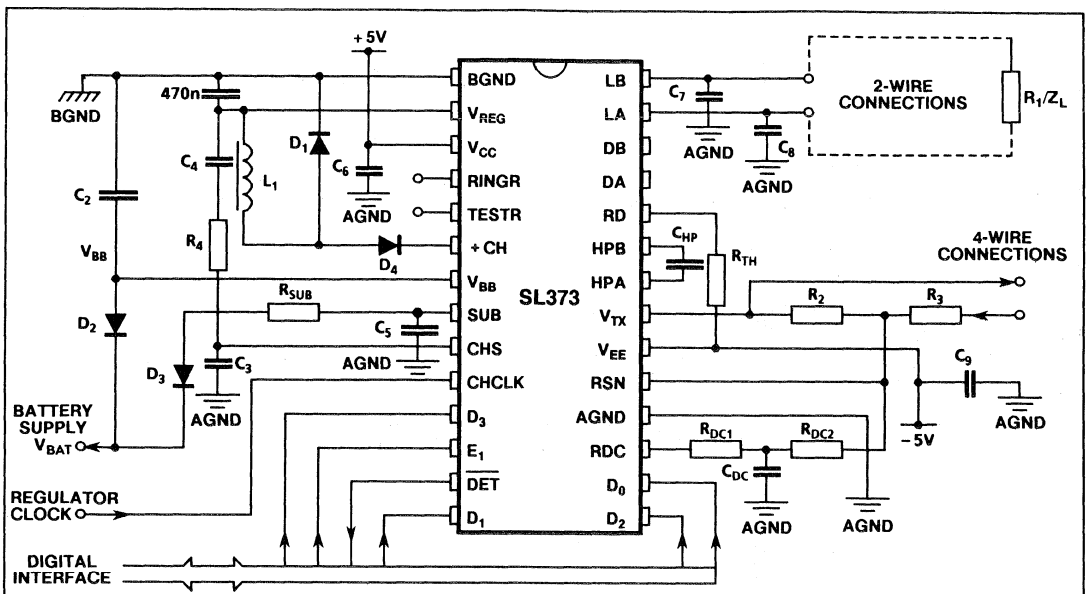


Fig.23 Test configuration (Note the SL373 block = Fig. 24)



C_1 = 470n	C_6 = 100n	C_{DC} = 82n	L_1 = 1mH	R_1 as Test Configuration
C_2 = 470n	C_7 = 10n	D_1 = 100V,100mA	R_{SUB} = 100Ω	R_2 as Test Configuration
C_3 = 560p	C_8 = 10n	D_2 = 100V,100mA	R_{TH} = 32kΩ (see Elec. Char.)	R_3 as Test Configuration
C_4 = 8.2n	C_9 = 100n	D_3 = 100V,100mA	R_{DC1} = R_{DC2} = 31.25kΩ(see Elec. Char.)	R_4 = 2.4kΩ
C_5 = 330n	C_{HP} = 330n	D_4 = 100V,100mA	Z_L = see Elec. Char.	

For all tests assume AGND = BGND.

Fig.24 Test circuit for Figs. 13-18 and 21-23.

ABSOLUTE MAXIMUM RATINGS* - Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value		Units
		Min.	Max.	
Battery supply voltage	V_{BB}	– 70	+ 1.0	V
Continuous battery ground voltage	V_{BGNDC}	– 0.3	+ 0.3	V
Intermittent (10μs) battery ground voltage	V_{BGNDI}	– 4.0	+ 4.0	V
Positive supply voltage	V_{CC}	– 0.4	+ 7.0	V
Negative supply voltage	V_{EE}	– 7.0	+ 0.4	V
Subscriber line voltage on LA, LB or both, continuous	V_{LC}	– 70.0	+ 0.4	V
Differential DC line current	I_{LDC}		150	mA
Switched regulator voltage (off)	V_{CH}	V_{BB}	+ 1.0	V
Switched regulator current (on)	I_{CH}		150	mA
Relay drivers output voltage	V_{RLY}	V_{BAT}		V
Relay drivers output source current	I_{RLY}		30	mA
Ring-Trip input voltage (DA or DB)	V_{RT}	V_{BB}	0	V
Ring-Trip input current (non-repetitive 10 ms pulse)	I_{RT}	– 10.0	+ 10.0	mA
Digital input voltage	V_{ID}	– 0.4	V_{CC}	V
Digital input current (sink)	I_{ID}		5.0	mA
Digital output voltage	V_{OD}	– 0.3	V_{CC}	V
Digital output current (source)	I_{OD}		3	mA
Storage temperature	T_{ST}	– 55	+ 125	°C
Operating junction temperature †	T_{JOP}		150	°C
Package power dissipation (DG28)	P_{PDG28}		1.5	W

*** Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.**

† Circuit includes thermal protection such that T_{PROT} (MIN) = 150°C.

SL374

SUBSCRIBER LINE INTERFACE CIRCUIT

The SL374 is a Subscriber Line Interface Circuit (SLIC) for use at the telephone exchange or PABX end of a telephone line.

It provides power feed, transmits and receives voice signals, controls ringing, supports line testing and detects Ground Key or Off-Hook conditions. These functions can be programmed to provide the flexibility required for different telephone networks.

The SL374 is fabricated using bipolar technology.

FEATURES

- Low Power Line Feed via Regulator
- Programmable Constant Current Feed to Line
- Programmable AC Termination Impedance
- Good Longitudinal Balance
- Ground Key and Ring Trip Detection
- Programmable Off-Hook Detection with Hysteresis
- Disconnect and Low Power Standby Modes
- A-Leg Disconnect, B-Leg Standby Mode
- Normal or Reversed Line Polarity Operation
- Ring and Test Relay Drivers
- Thermal Shut-Down Protection
- Transmission Characteristics Battery Independent Region

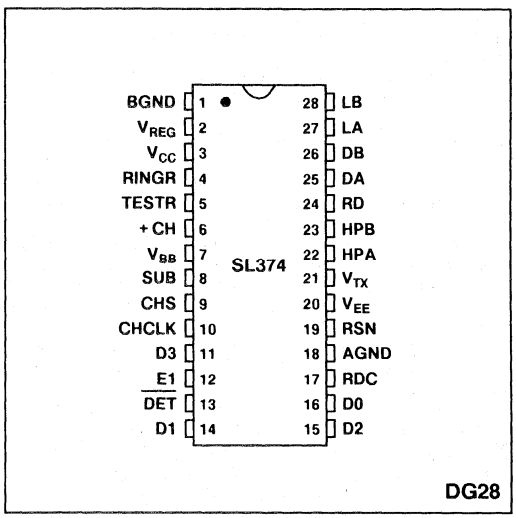


Fig. 1 Pin connections - top view

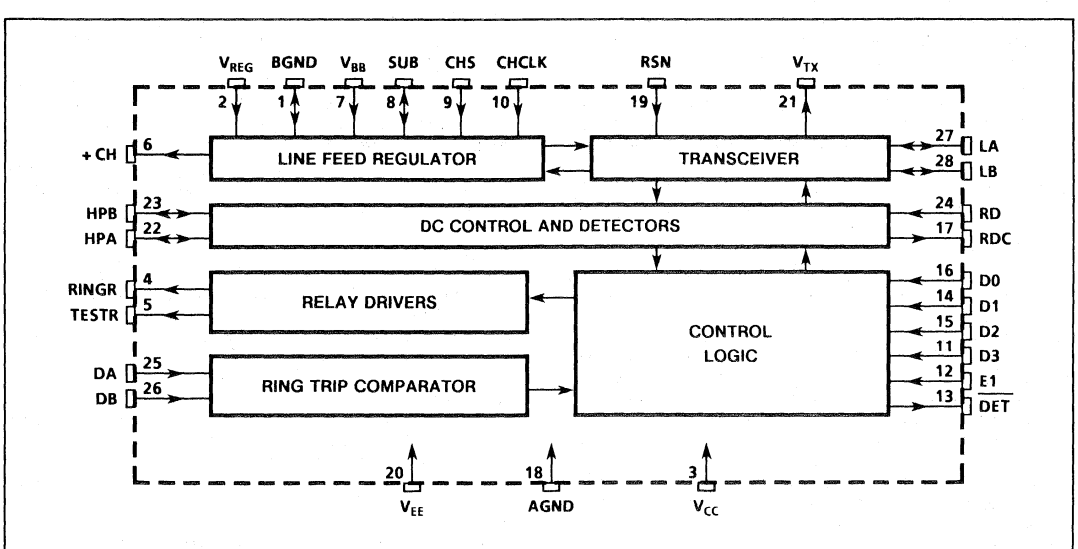


Fig.2 Functional block diagram

FUNCTIONAL OVERVIEW

The SL374 Subscriber Line Interface Circuit (SLIC), together with some external components, provides most of the line interface functions for ordinary or PABX line connections in a telephone network. It performs the interface between the two wire line and an ALAP (Analogue Line Audio Processor)/COMBO, such as the GEC Plessey Semiconductors MV3010 PSLAC (Plessesy Subscriber Line Audio Circuit) DSP device.

The SL374 is functionally equivalent to the SL373 but offers improved 2-wire balance, noise performance and supply rejection. The 4 to 2-wire current gain is reduced to 200, requiring appropriate scaling of associated components (compared with the SL373), as detailed in this data sheet.

The SLIC circuit contains several functional blocks to achieve the design aims (Fig.2). Firstly, the Transceiver consists of the two wire port, pins LA and LB. These pins are fed from the 4 wire input (RSN) controlling AC conditions, and from the Line Feed Regulator and DC Control blocks, controlling DC conditions. The 2 wire transverse AC signal is fed onto the 4 wire transmit output, VTX.

Power dissipation is minimised, under varying line conditions, by the Line Feed Regulator which adjusts the internal high voltage supply to that required for line feed. It consists of a switching regulator which can be synchronised to a 256kHz clock.

DC line conditions at the 2 wire interface are determined by the DC Control block. These DC conditions (modes of operation) are set by the Control Logic, which also monitors line status (On/Off-Hook) via the DC Control block detectors (Loop/Ground Key/Ring Trip comparator). The control logic also controls the Ring Relay Driver for Ringing mode of operation and an undedicated Test Relay Driver.

A brief outline of the device functionality is given below, before a more detailed discussion of the SLIC circuitry in the Functional Description section.

LINE FEED

Line loop (pins LA &LB) feeding is obtained from the battery supply (pin 7) by means of an internal power circuit, which can be set to different modes of operation (refer to table 2). These modes are as follows:

Standby Mode

Standby mode is the SLIC's low power mode in which the battery feed circuit limits the DC loop current to a level just sufficient to enable the SLIC to detect current above the On/Off-Hook threshold. This mode is used when the subscriber is Off-Hook and no call is in progress, or if On-Hook, to save power. Both the Loop and Ground Key detectors work in this mode.

Disconnect A and B Leg

This mode programs the SLIC such that the A and B leg output amplifiers are turned off, preventing current flow to the line.

Disconnect A, Standby B Leg

This is the SLIC Standby mode with the A Leg amplifier turned off, so that current can only flow in the B Leg. In this state it is only possible to detect the application of a ground to the B Leg.

Active Mode

This is the normal operating mode with a call in progress. The SLIC is used as a constant current feed device, with the feed current being set by external resistors.

Polarity reversal

The polarity of the feeding voltage at the SLIC can be reversed on command in Active and Standby modes.

All Active and Standby conditions apply equally to the respective reverse conditions. In these conditions the polarity of any DC parameter is reversed.

Ringing

This mode enables the Ring Relay output and selects the Ring Trip comparator. It does not provide DC line feed or AC ringing voltage which must be supplied externally (via the ring relay).

Test Mode

Testing of the line is not performed by the SLIC. This mode enables external access to the telephone line by directly driving the test relay.

SUPERVISION

The SLIC provides an Off-Hook or loop Detector (OHD), Ring Trip Detector (RTD) and a Ground Key Detector (GKD). These are described below, in addition to the SLIC on-chip thermal protection.

Off-Hook Detector

The Off-Hook Detector recognises the loop status by means of a threshold circuit. The OHD operates in Standby and Active modes (with or without polarity reversal), and in the presence of longitudinal currents. The detector threshold contains hysteresis and is nominally the same in Standby and Active modes, the actual level being externally programmable.

Ring Trip Detector

This detects when a subscriber goes off-hook during the application of a ringing signal (normally 25Hz) within a maximum delay of 150ms (determined by external components - see Applications section). The detector is active when the Ring Relay Driver is activated.

Ground Key Detector

The GKD circuit detects a current path from the A or B Leg to ground. It can be used in Standby, Active and Disconnect A Standby B modes.

Thermal Protection

In conditions which cause the chip junction temperature to rise above a critical level (around 150°C), the thermal protection will operate. This switches off the line current and therefore reduces the power dissipation.

TRANSMISSION

The signal transmission functions include 2 to 4-wire and 4 to 2- wire conversions.

The 2-wire termination impedance of the SLIC is programmed by external components. Transmit and Receive Gain are fixed and are nominally both unity (0dB), with the 2-wire port terminated in a matched load.

All the transmission parameters apply when the SLIC is operating in the presence of longitudinal currents, as specified in the Electrical Characteristics.

CONTROL

The SLIC is provided with a digital interface for controlling the 2-wire line status and passing line status information to the line card/system hardware. The operating characteristics can be selected by hardware with external components (see Digital Interface).

METERING

Injection of high amplitude high frequency meter pulses is not supported by the SL374. If this function is required, then the GPS SL376 Metering SLIC can be used instead (refer to separate Data Sheet).

RINGING

The application of the ringing voltage to the subscriber line can be via a relay or suitable high voltage crosspoint, external to the SLIC. This component is driven by the on-chip Ring Relay Driver. The relay is connected between RINGR and V_{BAT}.

When the SLIC is set to RING mode, the Ring Relay Driver output will be activated to energise the ring relay. The relay should be connected so as to cause the line to be disconnected from the SLIC and connected to a suitable ringing supply (continuous) voltage. Ring cadence can then be obtained by de-energising and re-energising the relay as required.

OVERVOLTAGE PROTECTION

Overvoltage protection is required to protect the SLIC from such line phenomena as lightning strikes and induced AC signals from, or direct contact with, power lines. This protection can be realised with components external to the SLIC.

INTERFACES

The SLIC has three main interfaces to external circuitry. These are the 2-wire, 4-wire and Digital interfaces which are described below.

Subscriber Line Interface (2-wire port)

Pins LA and LB form the Subscriber Line Interface providing line feed, signalling supervision and voice transmission between the subscriber's apparatus and exchange. It exhibits very good balance about ground to minimise the crosstalk between adjacent pairs in the local cable and noise from longitudinal interference. The termination impedance is set externally by Z_{TX} (see Fig. 3 and Functional Description).

The 2-wire port is designed to offer a low impedance to any longitudinal signals that appear on the subscriber line and the resulting signal level at the 4-wire output port is minimised.

It is able to handle longitudinal currents on the subscriber line in all modes of operation, except Disconnect mode, Disconnect A Standby B and Ringing when the SLIC 2-wire port is no longer connected to the line.

Analog 4-wire interface

Two pins of the SLIC (V_{TX} and RSN), together with associated grounds, provide the 4 wire interface to an ALAP or COMBO device. Both the transmit (V_{TX}) and receive (RSN) signals are unbalanced and have fixed gain settings. The V_{TX} pin has a low output impedance, whilst the RSN pin is a low impedance virtual earth input. The input current is normally a combination of the receive voice signal from the ALAP, line feed current programmed by the RDC pin (see Applications section) and termination of the V_{TX} pin.

Hybrid Balancing is not provided on the SLIC. This can be done by an ALAP such as the MV3010 PSLAC which uses DSP techniques, including an Adaptive Echo Cancellation feature.

Digital Interface

This is a parallel interface providing control of all the SLIC operating modes and indication of line status information. It consists of the 6 pins as listed in Table 1, the functions of which are described in Table 2.

Pin designation	Pin description
D0	Data Input
D1	Data Input
D2	Data Input
D3	Test Select Input
E1	Detector Select Input
$\overline{DET}$	Detector Data Output

Table 1 Digital interface pin designation

Mode	D3	D2	D1	D0	$\overline{DET}$ output status (Note 2)		Test relay
					E1 = 0	E1 = 1	
Disconnect A & B Legs	X	0	0	0	(Invalid)	(Invalid)	-
Ringing	X	0	0	1	Ring Trip (Note 3)	-	-
Active(Non-ringing)	X	0	1	0	Loop Detect	Ground Key	-
Standby	X	0	1	1	Loop Detect	Ground Key	-
Disconnect A,Standby B	X	1	0	0	Ground Key	(Invalid)	-
Reserved	X	1	0	1	-	-	-
Active, Polarity Reversed	X	1	1	0	Loop Detect	Ground Key	-
Standby, Polarity Reversed	X	1	1	1	Loop Detect	Ground Key	-
Line Test (Note 1)	0	X	X	X	-	-	Enabled
	1	X	X	X	-	-	Disabled

NOTES

1. D2, D1, D0 still change SLIC status even though Line outputs will be disconnected from line.
2. $\overline{DET}$ = 1 for On-Hook (high line impedance), $\overline{DET}$ = 0 for Off-Hook (low line impedance).
3. $\overline{DET}$ = 1 for Voltage DA > DB , $\overline{DET}$ = 0 for Voltage DA < DB.

Table 2 Digital interface functional description.

FUNCTIONAL DESCRIPTION

VOICE TRANSMISSION AND RECEPTION

It is conventional to assign the signal directions from the point of view of the served telephone set. The receive direction is towards the served telephone and the transmit direction is from it.

The basic voice circuit for the device is shown in Fig.3. The current which flows on the line, into LA and out of LB, is 200 times the current which flows into RSN and through the device to AGND.

The AC voice current flowing into RSN is composed of the current from V_{RX} through Z_{GR}, which controls the signal received at the remote telephone and a current from V_{TX} through Z_{TX} which controls the termination impedance. There is also a DC current at RSN which is analysed later in the discussion on DC line feed.

The 2 wire termination impedance is $Z_{AB} = (Z_{TX} \div \alpha)$ where α ($\simeq 200$) is the current gain between RSN and I_L (see Fig.3). This can be checked by setting V_{RX} to zero.

The Receive Gain, for normal voice signals (at V_{RX}), is inversely proportional to Z_{GR}. The actual value, which is negative, can be obtained by setting V_L equal to zero in Fig.3. This gives:-

AC voltage between LA and LB $(V_{LA}-V_{LB})_{ac}$

$$= (V_{LA} - V_{LB}) - (V_{HPA} - V_{HPB})$$
$$= I_L \times \{Z_{AB} \| Z_L\}$$
$$= -\left(\frac{Z_L \times \frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right)\frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}$$

i.e. minus the ratio of the line and terminating impedances (Z_L and $Z_{TX} \div \alpha$) in parallel, to the receive impedance divided by the current gain ($Z_{GR} \div \alpha$). This expression simplifies to :-

$$= \frac{-V_{RX}\alpha Z_L Z_{TX}}{(\alpha Z_L + Z_{TX})Z_{GR}}$$

In the transmit direction, the voltage at V_{TX} is the superposition of the voltage from the line, with the voltage produced on the line from V_{RX}, i.e:-

$$V_{TX} = \left[\left(\frac{\frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right)V_L - \left(\frac{Z_L \times \frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right)\frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}\right]$$

This expression simplifies to :

$$V_{TX} = \frac{[Z_{GR}(V_L)_{ac} - \alpha Z_L V_{RX}]Z_{TX}}{(\alpha Z_L + Z_{TX})Z_{GR}}$$

This equation can be used to determine the transmit gain, from $(V_L)_{ac}$ to V_{TX}, by setting $V_{RX} = 0$ which gives $+Z_{TX} \div (\alpha Z_L + Z_{TX})$. The 4-wire to 4-wire gain, V_{RX} to V_{TX}, is also obtained by setting $(V_L)_{ac} = 0$ instead, which gives us the expression $-\alpha Z_L Z_{TX} \div [(\alpha Z_L + Z_{TX})Z_{GR}]$. If fuse resistors are included in the 2-wire loop, then Z_L is modified to become $(Z_L + 2R_{FUSE})$ in the above equations.

The transmission circuitry also contains a longitudinal feedback circuit, such that the SLIC appears as typically 25Ω resistors from LA and LB to a bias voltage (see DC Line feed section). This bias voltage comes from the DC feed circuitry. The feedback circuit attenuates longitudinal signals from the transmit path, and has no effect on transverse signals.

DC LINE FEED (Active Mode)

DC line feed (loop) current $I_L = \frac{1}{2}(|I_A - I_B|)$ is provided by the device when it is in non-ringing modes. In RING mode, DC line feed and AC ringing voltage are normally applied through the ring relay which is controlled by the device. The line feed current is reduced during standby operation.

In Active mode, Power feed is controlled by the resistance R_{DC} ($= R_{DC1} + R_{DC2}$) between the R_{DC} pin and the RSN pin (Fig.4). Again, the current in the 2 wire loop will be 200 times the current into RSN. Operation of the DC feed circuitry is described with reference to Fig.4, which shows a conceptual model.

For the normal line feed region, a voltage V_{DC}, of magnitude 2.5V is produced at the R_{DC} pin. The sign of V_{DC} determines normal or reverse polarity operation. If negative, normal polarity is established and if positive, reverse polarity will occur (polarity is set by control logic - see Table 2). This normal line feed region exists when $|V_{BAT}| - |V_{DCT}| \geq V_{SG}$ ($V_{SG} = 15V$ nominally), otherwise the Saturation Guard circuit is active (described later).

Note that the internal resistor, R_{HP}, and external capacitor, C_{HP} form a low pass filter network The issues raised in the discussion on C_{HP} for the SL373/SL376 SLICs in Application Note AN82 are also valid for choosing C_{HP} for the SL374. During the action of reversing polarity, the resistors R_{HP} are momentarily short-circuited to reduce the time taken for the DC voltage on C_{HP} to change sign.

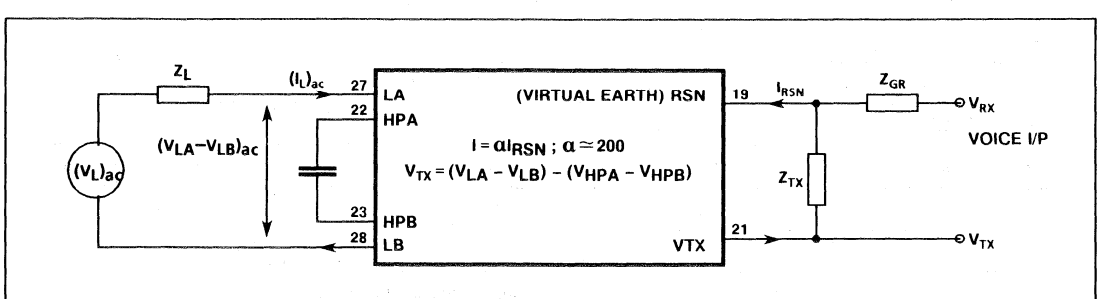


Fig.3 Voice circuit

The ×200 virtual earth input current amplifier means that the feed current is determined by R_{DC}, i.e:

$$I_L = 500 \div R_{DC} = 500 \div (R_{DC1} + R_{DC2})$$
(Saturation Guard inactive)

If fuse resistors are included in the 2-wire loop, the feed current will not be affected. However, the fuse resistors will affect the line current in the saturation guard region (desribed later).

As an example, to set $I_L = 40mA$, then:

$$(R_{DC1} + R_{DC2}) = 500 \div I_L = 12.5k\Omega$$

The values of R_{DC1} and R_{DC2} should be kept equal, forming a low pass filter network with C_{DC} to reduce chopper noise from the R_{DC} pin (again, the discussion on C_{HP} in the SL373/SL376 Application Note AN82 is also valid for the SL374). The time constant of this network (C_{DC} and $R_{DC1} \| R_{DC2}$) also affects the time taken for a polarity reversal, and it is normally ≈1.5ms.

The remaining circuitry models the action of the saturation guard circuit, which can operate in two modes. If the battery voltage is above about 59V, then the saturation guard (battery independent mode) will operate under the control of an internal 'noiseless' reference voltage. This ensures that with long lines, V_{DCT} will be limited to about 46V, thus protecting the internal circuitry from saturation. At battery voltages below about 59V, the battery dependent saturation guard mode is active.

This operates to reduce the voltage at the RDC pin when $|V_{BAT}| - |V_{DCT}| < V_{SG}$. V_{SG} is a notional threshold voltage which is the headroom between the value of V_{DCT} and the battery voltage at the point where saturation guard becomes active (this includes the diode drop in series with the V_{BAT} supply, D_2 Fig. 7). Thus, when the comparator determines this condition, the magnitude of the difference is used to reduce the voltage at R_{DC}.

The total line feed characteristic is shown graphically in Figs. 6a and 6b. The nearly constant voltage region is due to the action of the saturation guard circuit, and is affected by the value of $2R_{FUSE}$ as shown in Fig. 6a (nominal constant voltage is maintained at the LA-LB pins, not V_L). Fig. 6b plots the loop current value as a function of line resistance R_L. The example shown is that of a 40mA ($R_{DC} = 12.5k\Omega$) feed current, the graphs being obtained by using the simple models of Figs. 5a and 5b (0Ω fuse resistors). Figs. 6a and 6b also show the action of V_{BAT} on the line characteristics (note the region where V_{BAT} exceeds about 59V with the DC characteristics independent of battery).

With the Saturation Guard inactive, normal line feed conditions apply such that the feed current and line/loop resistance determine V_L by the relationship $V_L = I_L \times R_L$. This gives the characteristic shown in Fig. 6a, which is the vertical line section of the graph.

When the saturation guard is active, then the line voltage is effectively held constant due to the reduction of the voltage at the R_{DC} pin.

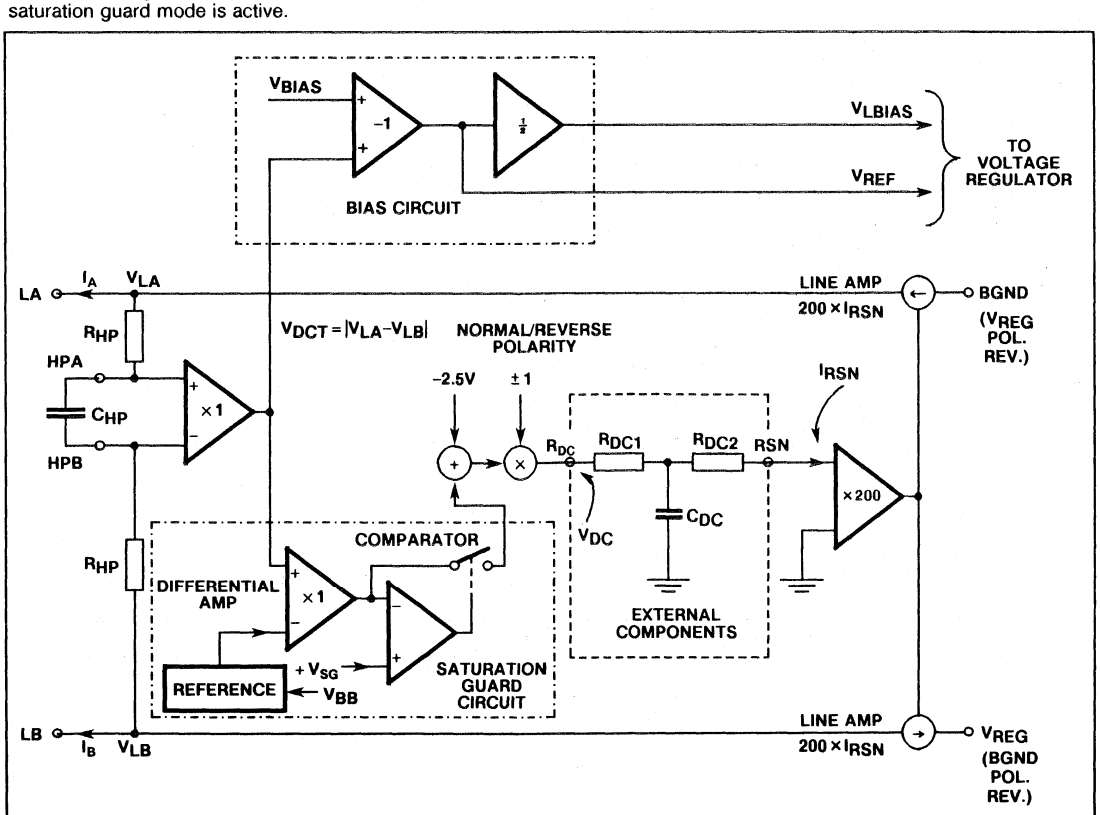


Fig.4 DC power feed circuit model.

Thus, line conditions are set by the following:

$I_L = [(|V_{BAT}|-V_{SG}) \div (R_L + 2R_{FUSE})]$ $(|V_{BAT}| < \approx 59V)$
$I_L = [(46) \div (R_L + 2R_{FUSE})]$ $(|V_{BAT}| > \approx 59V)$

To determine the line resistance (R_{LSG}) and Line voltage (V_{LSG}) at which the battery dependent saturation guard becomes active, these parameters are obtained by equating the two expressions for normal and saturation guard regions. Thus :

$R_{LSG} = [(|V_{BAT}|-V_{SG}) \times (R_{DC} \div 500)]-2R_{FUSE}$ and
$V_{LSG} = |V_{BAT}|-V_{SG}-[2R_{FUSE} \times (500 \div R_{DC})]$ $(|V_{BAT}| < \approx 59V)$

In the battery independent saturation guard region, we get, alternatively:

$R_{LSG} = [(46) \times (R_{DC} \div 500)]-2R_{FUSE}$ and
$V_{LSG} = 46-[2R_{FUSE} \times (500 \div R_{DC})]$ $(|V_{BAT}| > \approx 59V)$

The resultant line voltage (V_{LSG}) that occurs depends on the ohmic relationship of I_{LSG} and R_{LSG} (see Fig. 6a) which will equal $|V_{BAT}|-V_{SG}$ when $2R_{FUSE} = 0\Omega$. The open circuit voltage, $V_{LOC} \approx |V_{BAT}|-V_{SG}$ at $R_L = \infty\Omega$, will always be greater than V_{LSG}, even when $2R_{FUSE} = 0\Omega$. This change in voltage between V_{LSG} and V_{LOC} will be greater at lower values of V_{BAT}. Fig. 6a shows the nominal effect.

DC LINE FEED (Standby Mode)

For Standby mode, the DC current is half the active mode value. Normally the loop detector current threshold (I_{DET}) is set externally by a resistor, R_{TH} (see Control and Signalling section). The limited loop current in Standby (I_{LIM}) is determined by R_{DC} as $I_L \leq I_{LIM} = 250 \div R_{DC}$

The shape of this characteristic is almost a constant current, as shown in Fig. 6a.

LINE POLARITY

Normal polarity (Active/Standby) consists of the LA pin voltage near BGND and the LB pin voltage negative of LA. Under these conditions $I_L = +\frac{1}{2}|I_A-I_B|$ and the voltage at the RDC pin is negative. Reverse polarity will give LA voltage negative of LB, LB voltage near BGND, $I_L = -\frac{1}{2}|I_A-I_B|$ and the voltage at the RDC pin is positive.

BIAS CIRCUIT

The Bias circuit (Fig. 4) produces two reference voltages, both referred to ground. These are V_{REF}, being related to the 2-wire transverse DC voltage and V_{LBIAS} approximately half V_{REF}. V_{REF} controls the line feed regulator and V_{LBIAS} sets the 2-wire feed balance voltage (centre point voltage of the lines). The longitudinal control loop achieves an input impedance of approximately 25Ω per line for longitudinal signals, as shown in Fig.5c.

LINE FEED REGULATOR

The DC voltage between LA and LB will vary with the DC loop resistance. Unless the voltage supplied to the SLIC can be varied to match that on the line there will be a voltage drop across the chip along the path taken by the feed current.

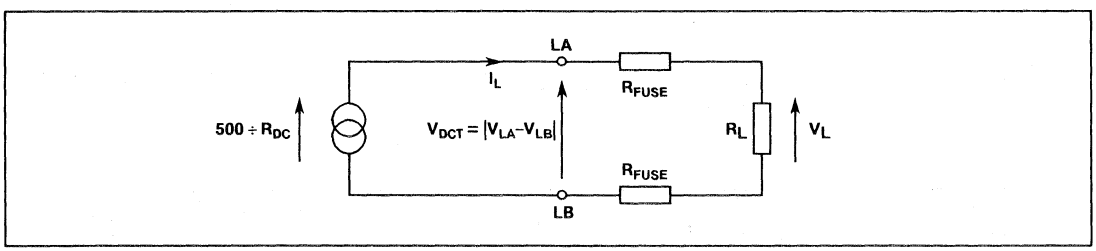


Fig. 5a Simple power feed model (normal line feed)

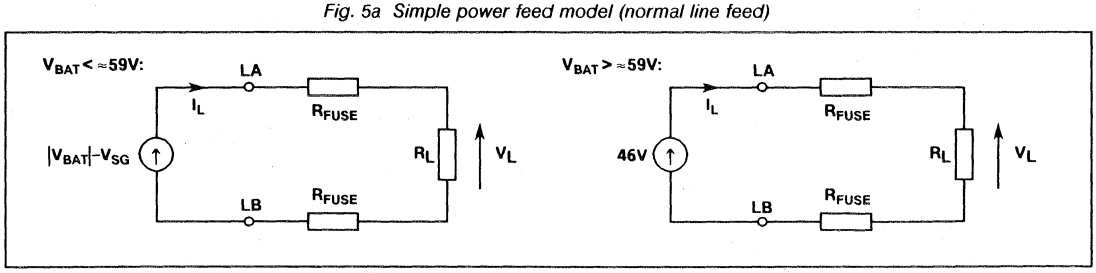


Fig. 5b Simple power feed model (saturation guard active)

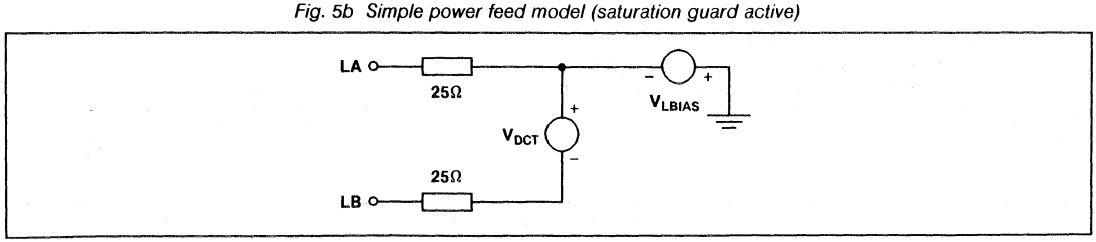
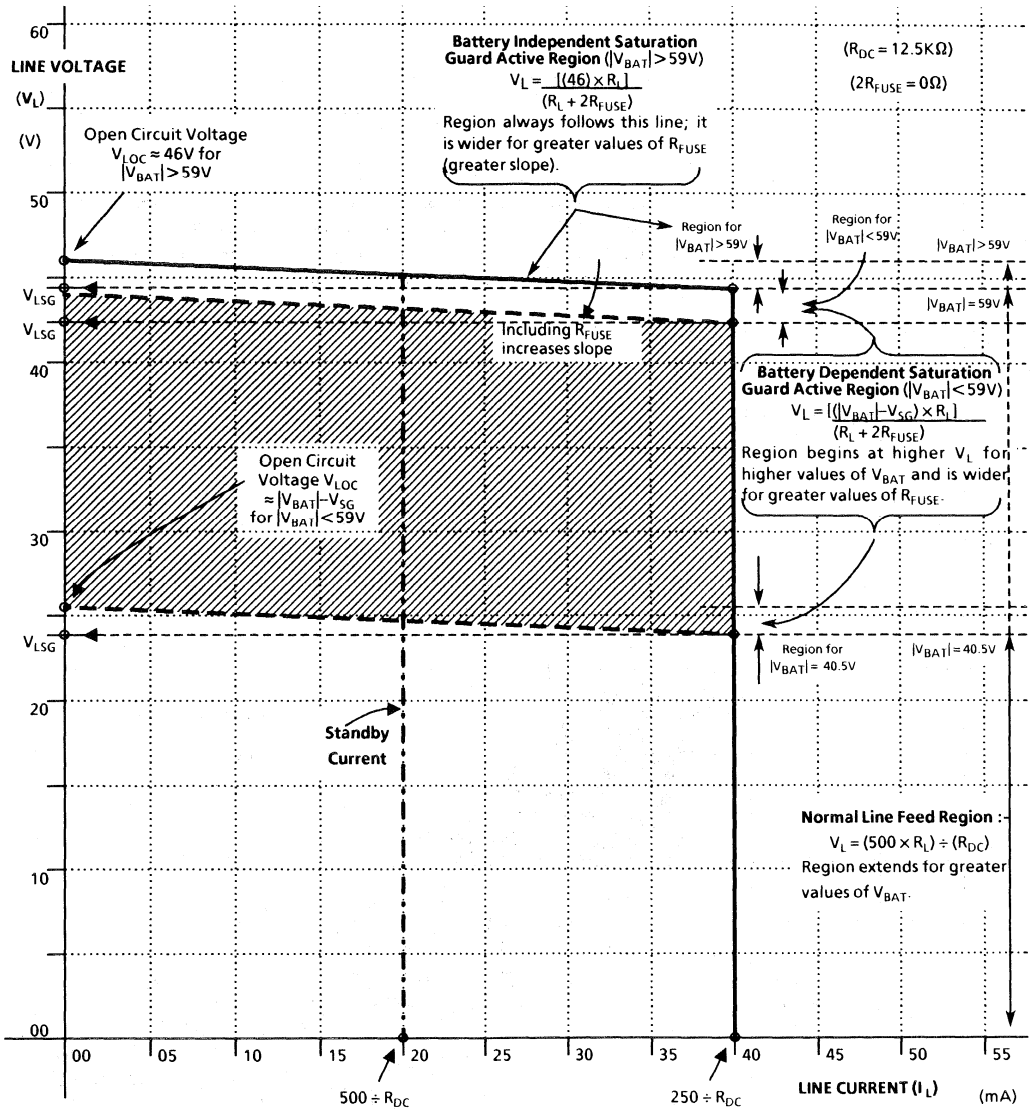


Fig. 5c Longitudinal bias circuit.



For $|V_{BAT}|<59V$:-

$V_{LSG} = |V_{BAT}|-V_{SG}-[2R_{FUSE} \times (500 \div R_{DC})]$

$R_{LSG} = [(|V_{BAT}|-V_{SG}) \times (R_{DC} \div 500)]-2R_{FUSE}$

For $|V_{BAT}|>59V$:-

$V_{LSG} = 46-[2R_{FUSE} \times (500 \div R_{DC})]$

$R_{LSG} = [46 \times (R_{DC} \div 500)]-2R_{FUSE}$

For the Saturation Guard active regions, near constant voltage exists at the LA/LB pins. This is modified by R_{FUSE} as shown by the graph. Some voltage drop between open circuit voltage V_{LOC} and the value of V_{LSG} will occur, even with $2R_{FUSE} = 0$ as shown.

Note : In the region shaded ▨ some of the transmission parameters will degrade when the battery voltage is between −40.5V and −59V (see Electrical Characteristics section). The performance of the SL374 is optimised for a −62V battery supply. For values of $V_{BAT}>-59V$, the characteristic always follows the solid line.

Fig.6a Line feed characteristic, V_L vs I_L.

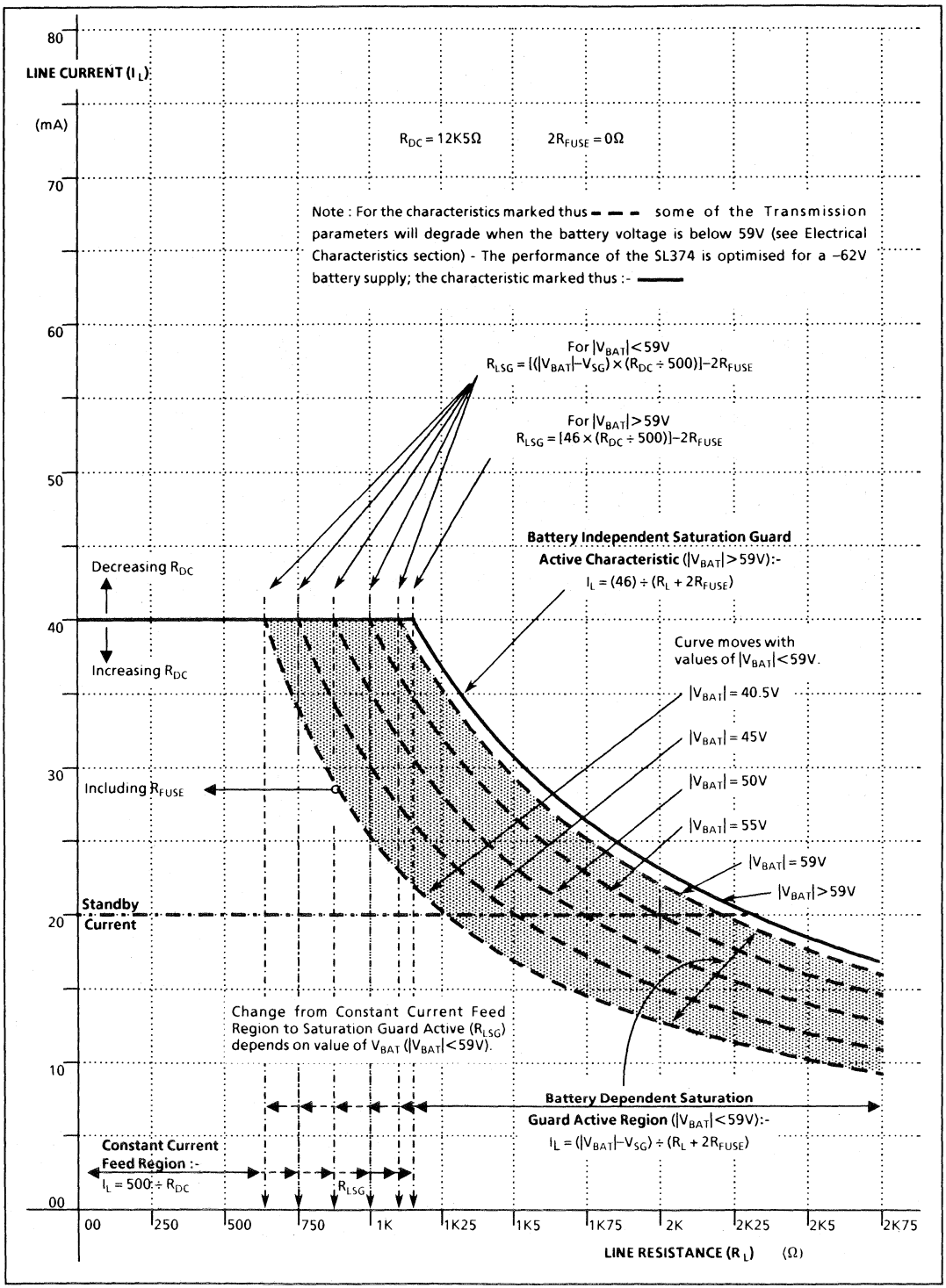


Fig.6b Line feed characteristic, I_L vs R_L.

This could cause significant power dissipation. The purpose of the line feed regulator is to minimise this power dissipation by regulating the voltage supplied to the Line Amplifiers.

Regulated voltage is supplied to the Line Amplifiers on V_{REG} and unregulated voltage is supplied on V_{BB}. The chip switches V_{BB} onto +CH when more power is required at the V_{REG} pin. V_{REG} is the voltage used by the device to power the 2-wire interface, and it is adjusted to follow a reference voltage V_{REF} (from Power Feed). This reference voltage is determined as follows:

$$V_{REF} = -\{ | V_{DCT} | + V_{BIAS} \}$$

and is such to set V_{REG} to the minimum required to power the line interface. This then ensures a minimum power dissipation. The voltage V_{BIAS} is needed to allow voltage headroom for circuit operation.

Fig. 7 shows the external components associated with the power supply aspect of the voltage regulator. +CH is the positive terminal of the regulator switch that connects to V_{BB}. When the switch is turned on, current in L_1 and C_1 increases, thus increasing stored energy. When the switch turns off, this stored energy sustains L_1 current which flows in D_1. The voltage at +CH is thus a square wave of up to 50V p-p making this node sensitive to PCB layout. Note that the inductor should be capable of taking twice the line current without saturating. The regulator will work with a wide range of inductor resistance, although if this is too large, long line drive capability and regulator efficiency will be reduced. Since there are large current fluctuations from V_{BB} through the switch, C_2 provides filtering of the VBB pin, whilst D_2 isolates the V_{BAT} supply should the LA/LB pins be taken negative of the V_{BAT} supply.

The chip senses the voltage at V_{REG}, compares it to its requirements and switches power from V_{BB} to +CH, using the variable mark/space method, to give appropriate matching. The rate of switching can be synchronised to the system clock at approximately 256KHz via CHCLK (pin 10) or allowed to free run, its stability ensured by the network on CHS (pin 9), i.e. C_3, R_1, C_5. Since noise is produced by the switching, a decoupling node is provided at SUB (pin 8).

CONTROL AND SIGNALLING

The mode of operation of the SL374 is determined by the Digital Interface pins, as described in Tables 1 and 2. These pins enable Ringing or Non-Ringing modes of operation, controlling line status, line polarity, Relay Driver and selection of line detector.

The line status is selected by use of the D2..D0 pins, Table 2, to determine the modes as listed. The function of these modes has already been described in the 'Overview' and 'DC Line Feed' sections; more detail of the device detectors is given here (refer to Fig. 8).

Loop Detector

This detector is used in Active and Standby modes (with/without polarity reversal). The loop current at which the detector indicates the Off-Hook condition, is set by the comparator with hysteresis at pin 24 (RD). Normally a resistor, R_{TH}, is connected between pin 24 and pin 20, such that the line current thresholds I_{DETON} and I_{DETOFF} are set by:

$$I_{DETON} = 410 \div R_{TH}$$
$$I_{DETOFF} = 465 \div R_{TH}$$

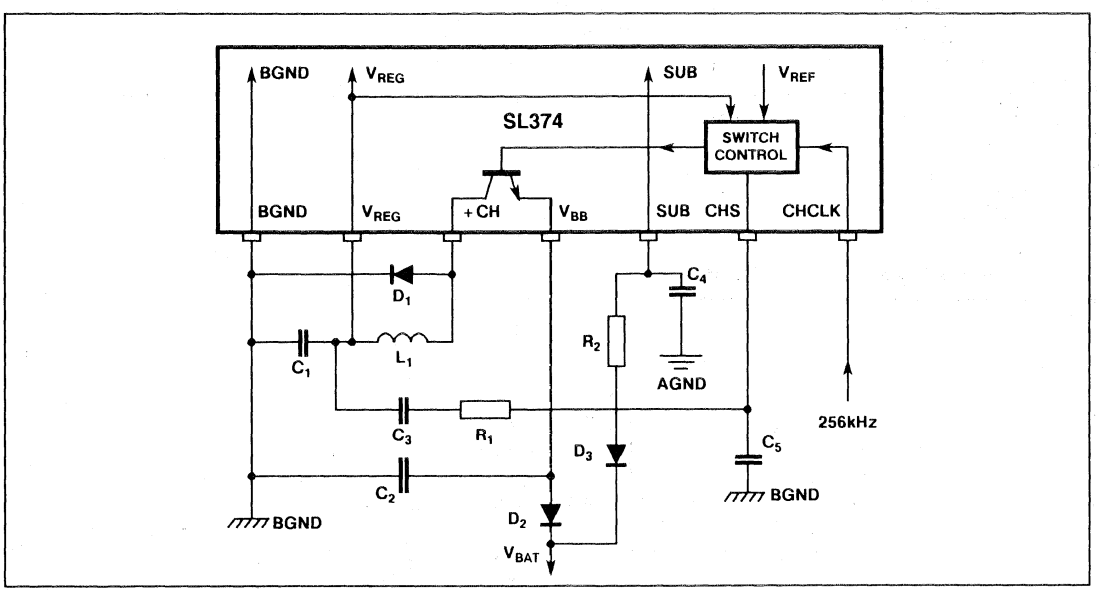


Fig.7 Voltage regulator power supply circuit.

This is due to the fact that the current out of the RD pin is linearly related to the loop current ($I_L = \frac{1}{2}|I_A - I_B|$). This creates a voltage across R_{TH} at the RD pin. Off-Hook is given by a logic low at the $\overline{DET}$ output pin (detector selected) when this voltage rises above the internal reference, and On-Hook a logic high when it falls below the lower I_{DETON} level.

Ground Key Detector

This detector is selected by the E1 pin of the Digital Interface (see Table 2). It can be used in Active and Standby modes (with/without polarity reversal), as well as Disconnect A Standby B mode. Operation of the detector is via an internal threshold and the longitudinal current $I_{LL} = I_A + I_B$ of the 2-wire loop. Ground Key detection is indicated when either the midpoint of the A and B legs or the B leg (A leg, polarity reversed) is connected to ground.

The resistance values for which Ground Key detection is valid are given in the Electrical Characteristics section.

Ring Trip Detector

This consists of a comparator connected to the DA and DB pins, and indicates Ring Trip when the voltage at DA < DB. Selection of Ringing mode operates the Ring Relay and enables the Ring Trip Detector. The external ringing supply must consist of DC line feed in addition to the AC ringing voltage. In order that the Ring Trip Detector senses Ring Trip in ringing mode, a resistance bridge network is used in association with pins DA, DB, line and ring source. This network is described in the Applications section and discussed further in AN82 and is the same as that which is discussed further in AN82 SL373/SL376 Applications Note.

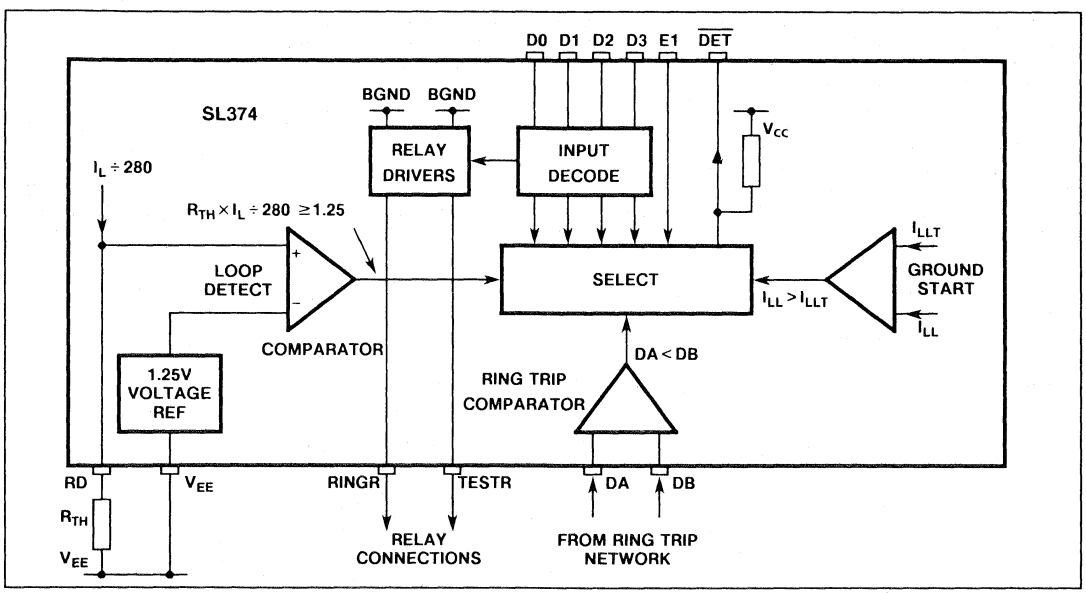


Fig.8 Detector circuits.

FUNCTIONAL PARAMETER SUMMARY

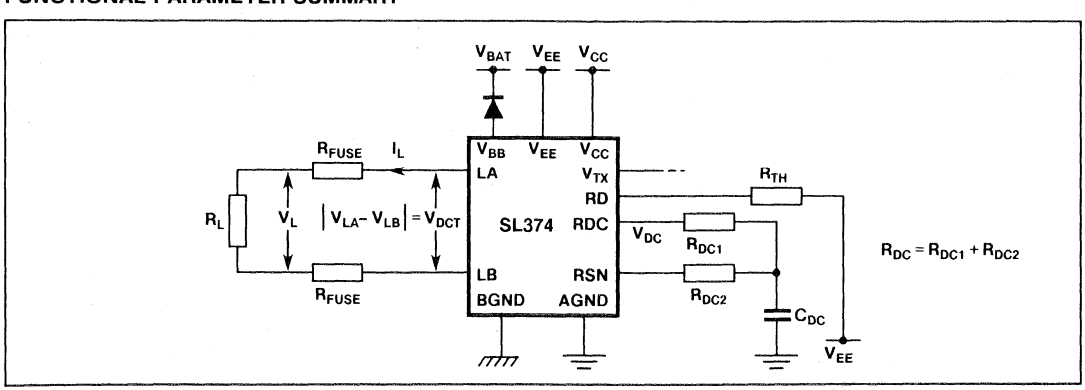


Fig.9 DC parameters and components for the SL374

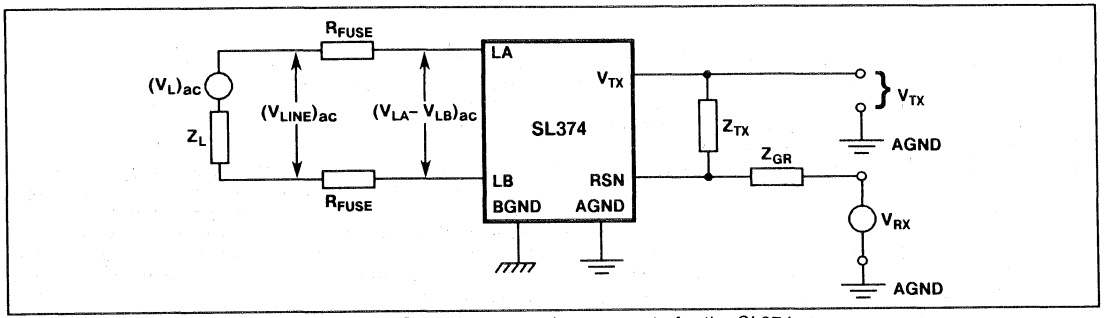


Fig.10 AC parameters and components for the SL374

LIST OF DEFINITIONS

1. Loop Current is defined as :- $I_L = \pm\frac{1}{2}|I_A - I_B|$

   I_A = current out of LA pin, I_B = current out of LB pin, + ⇒ normal line polarity and –⇒ reverse line polarity.

2. Longitudinal Current is defined as :- $ILL = (I_A + I_B)$

   I_A = current out of LA pin, I_B = current out of LB pin.

3. Normal Line Feed Region when $|V_{BAT}|-|V_{DCT}| > V_{SG}$ with $I_L = I_{FEED} = (500 \div R_{DC})$

4. Saturation Guard Threshold when $|V_{BAT}|-|V_{DCT}| = V_{SG} = 15.0V$ such that :-

   for $|V_{BAT}| < \approx 59V$ $\quad V_L = V_{LSG} = |V_{BAT}|-V_{SG}-[2R_{FUSE} \times (500 \div R_{DC})]$ which will equal $|V_{BAT}|-V_{SG}$ with $2R_{FUSE} = 0$ and
   $R_{LSG} = [(|V_{BAT}|-V_{SG}) \times (R_{DC} \div 500)]-[2R_{FUSE}]$

   for $|V_{BAT}| > \approx 59V$ $\quad V_L = V_{LSG} = 46-[2R_{FUSE} \times (500 \div R_{DC})]$ which will equal 46V with $2R_{FUSE} = 0$ and
   $R_{LSG} = [(46) \times (R_{DC} \div 500)]-[2R_{FUSE}]$

5. Saturation Guard feed Region when $|V_{BAT}|-|V_{DCT}| < V_{SG}$ with :-

   $I_L = [|V_{BAT}|-V_{SG}] \div [R_L + 2R_{FUSE}]$ for $|V_{BAT}| < \approx 59V$, the Battery Dependent Saturation Guard region
   or $\quad I_L = [|46] \div [R_L + 2R_{FUSE}]$ for $|V_{BAT}| > \approx 59V$, the Battery Independent Saturation Guard region.

6. Note that V_{LSG} is referred to as the value of the line voltage, V_L, at the point where Saturation Guard becomes active. This will differ from the value of $|V_{LA}-V_{LB}|$ (i.e. V_{DCT}) if $2R_{FUSE} \neq 0$. V_{SG} is used as a notional threshold voltage which is the internal headroom between the $|V_{LA}-V_{LB}|$ voltage and the battery supply, at this same point.

7. Open Circuit Line Voltage V_{LOC} at $R_L = \infty\Omega$ such that :$V_L = V_{LOC} \approx [|V_{BAT}|-V_{SG}]$ for $|V_{BAT}| < \approx 59V$
   $V_L = V_{LOC} \approx 46V$ for $|V_{BAT}| > \approx 59V$

   V_{LOC} will be $\geq V_{LSG}$ even with $2R_{FUSE} = 0$. The voltage drop from V_{LOC} to the defined V_{LSG} point will be greater at lower values of V_{BAT}.

8. Standby Mode DC Feed Current $I_L \leq I_{LIM} = 250 \div R_{DC}$ (i.e. $\frac{1}{2}$ Active Mode current).

9. 2 Wire Termination Impedance $Z_{AB} = (Z_{TX} \div \alpha) = (Z_{TX} \div 200)$.

   Note that Z_{TX} is normally set to $[\alpha(Z_L + 2R_{FUSE})]$ where Z_L is the desired termination impedance.

10. Recieve Gain from V_{RX} to $(V_{LA}-V_{LB})_{ac}$ or $(V_{LINE})_{ac}$ is set by Z_{GR} after setting Z_{TX}. Thus, with $(V_L)_{ac} = 0$:-

    $\frac{(V_{LA}-V_{LB})_{ac}}{V_{RX}} = \frac{-\alpha Z_L Z_{TX}}{[\alpha(Z_L) + Z_{TX}]Z_{GR}}$ with $2R_{FUSE} = 0$; $\frac{(V_{LINE})_{ac}}{V_{RX}} = \frac{-\alpha Z_L Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]Z_{GR}}$ with $2R_{FUSE} \neq 0$

11. Resultant Transmit Gain is then :- $\frac{V_{TX}}{(V_L)_{ac}} = \frac{Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]}$ with $V_{RX} = 0$

12. Resultant 4 Wire-4 Wire Gain is then :- $\frac{V_{TX}}{V_{RX}} = \frac{-\alpha(Z_L + 2R_{FUSE})Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]Z_{GR}}$ with $(V_L)_{ac} = 0$

13. Off-Hook Thresholds are set by R_{TH} at :- $I_L = I_{DETON} = 410 \div R_{TH}$
    $I_L = I_{DETOFF} = 465 \div R_{TH}$

Off Hook is valid for $I_L > I_{DETOFF}$ and On Hook is valid for $I_L < I_{DETON}$ with $I_{DETON} < I_L < I_{DETOFF}$ the hysteresis region.

14. Ring Trip Threshold is set by the bridge associated with pins 25 .. 28 and the 2 Wire Line, thus :-

    $R_L = R_{LTH} = R_{B4}(2R_F) \div (R_{B4}-R_{B1})$ assuming $R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$ and $R_{FEED1} = R_{FEED2}$ for the bridge components (balanced ringing). $R_{B1}..R_{B4} \approx$ a few 100KΩ and $R_{FEED1} \approx$ a few 100Ω.

15. AC ringing voltage at DA (DB by the same amount) is reduced by a factor of :- $[1 + (2\pi f_r t_r)^2]^{-\frac{1}{2}}$

    f_r is the ringing frequency and t_r is determined by the bridge components including C_B, thus :- $t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$

    for Balanced Ringing.

APPLICATIONS

The requirements for the subscriber line interface vary considerably from one telephone administration to another. The SL374 is designed to have the flexibility to meet these varying requirements. For simplicity, only a single example is given to illustrate how the device is connected. Fig. 11 shows the circuit which can be used to evaluate the device. Further Applications information is given in AN82 SL373/SL376 Applications Note.

The DA and DB pins are connected to a resistance bridge network (R_{B1} to R_{B4}). This allows the change in line resistance to be sensed when the remote telephone goes off-hook during ringing (Ring Trip). The details of this network (and C_B) are given later (see Ring Trip section). The resistors R_{FEED1} and R_{FEED2} provide feeding of the ringing source onto the line during ringing mode. The Ring and Test Relay coils are connected to the SL374 through current limiting resistors.

Connections to the LA and LB pins are shown, and include the resistors R_{FUSE} in addition to the ring relay. These resistors have a value around 20 to 30 ohms, depending on the application, and provide current line protection.

Overvoltage and protection circuitry may consist of slew-limiting inductors between the pins and the line itself and a thyristor or zener protection network at the line. In many applications, especially in PBXs, the amount of protection circuitry can be reduced. The capacitors between LA, LB and ground, allow noise from the regulator to be decoupled.

The capacitor C_{HP} between HPA and HPB (pins 22 and 23) is used to filter out the AC component of the signal on the line. The voltage difference between the two pins should be effectively DC. Application Note AN82 contains further relevant discussion on this component.

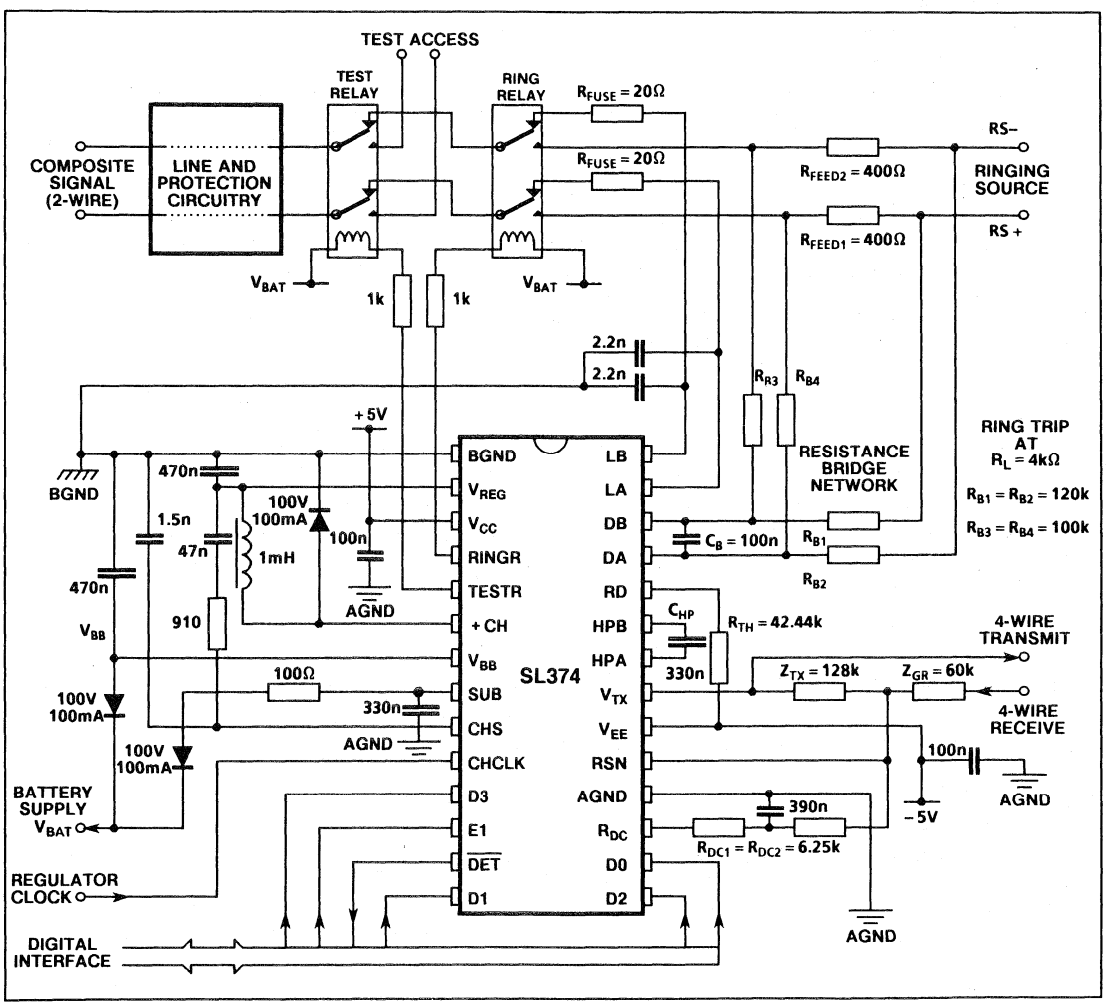


Fig. 11 Application circuit

The resistor, R_{TH}, between RD (Pin 24) and V_{EE} (pin 20) programs the threshold current for the loop detector. A capacitor in parallel can be added to reduce the effect of the AC component of the line current; a typical value might be 100n. The value of R_{TH} sets the loop detect threshold currents to :

$$I_{DETON} = 410 \div R_{TH} = 9.66mA$$
$$I_{DETOFF} = 465 \div R_{TH} = 10.96mA$$

The CHS pin (Pin 9) is connected to BGND through a capacitor and to V_{REG} by a capacitor and resistor in series. This stabilises the regulator control loop. Operation of the regulator has been described earlier in the Functional Description section (pins 2,6 & 7).

It is recommended that pin 8, the substrate (SUB) pin, be decoupled to AGND. However, BGND may be used if this is sufficiently quiet, otherwise some degradation in noise performance may be experienced.

DC current flows between pin 17 (R_{DC}) and pin 19 (RSN). This is used to set the line feed current. Any minor AC fluctuations are reduced by dividing the resistance R_{DC} equally such that $R_{DC1} = R_{DC2} = \frac{1}{2}R_{DC}$ and connecting a capacitor from the junction of R_{DC1} and R_{DC2} to AGND.

The Receive Gain is set by the network (Z_{GR}) which controls the receive current flowing into RSN. This can be a complex impedance network to allow for complex impedance terminations.

The network (Z_{TX}) between V_{TX} and RSN controls the 2-wire terminating impedance (Z_T). This can also be a complex impedance. The value of Z_{TX} can be calculated from the relationship :-

$$Z_{TX} = (\text{Required } Z_T) \times (\text{Receive Current Gain} = 200)$$

Connections for both Ring and Test relays are also shown in Fig. 11. Note that the 1kΩ resistors provide current limit through the relay coils when the driver outputs are on.

Control and status pins are TTL compatible. They are designed to give a simple interface to digital circuits and are directly compatible with the MV3010 PSLAC.

RING TRIP

Ring Trip detection operates by comparing thevoltages on DA and DB and providing the output on $\overline{DET}$ when this function is enabled by the status input pins of the Digital Interface. A resistance bridge (R_{B1} to R_{B4}) must be connected to the line and the ringing voltage sources to cause the differential voltage between DA and DB to change sign when the line resistance falls below the level associated with Ring Trip. Note that it is simplified by use of $R_{B1} = R_{B2}$ and $R_{B3} = R_{B4}$ (see AN82).

Ringing voltage is normally applied to the line through the Ring Relay which is activated by RINGR. The ringing voltage sources, including line feed, are connected to the line via ringing feed resistors, R_{FEED1} and R_{FEED2}. The resistance bridge operates by allowing the DC voltage dropped across the ringing feed resistors (R_F) in the Off-Hook condition to reverse the polarity of the voltage on DA and DB (DA < DB). Since the AC ringing voltage is greater than the DC feed, the capacitor C_B (Fig. 12) will filter this out at the comparator inputs. The connection shown is suitable for balanced ringing only. For unbalanced ringing, separate capacitors from DA (C_{B1}) and DB (C_{B2}) to ground will be required to achieve the same result.

Fig. 12 shows how the resistance bridge is connected when used with balanced ringing. The circuit can operate correctly provided there is a DC feed in addition to the AC ringing voltage.

If R_{LTH} is the line resistance corresponding to the Ring Trip threshold (DA = DB), this can be determined from the values of R_F ($R_{FEED1} = R_{FEED2} = R_F$), R_{B1} and R_{B4} ($R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$) as:-

$$R_{LTH} = \frac{R_{B4}(2R_F)}{(R_{B1} - R_{B4})}$$

R_{B1} and R_{B4} should be a few hundred kΩ.

The amplitude of the AC ringing voltage at DA (DB by the same amount) is reduced by a factor of $[1 + (2\pi f_r t_r)^2]^{-\frac{1}{2}}$ where f_r is the ringing AC frequency and t_r is set by:-

$$t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$$

for balanced ringing. For $f_r \approx 20Hz$, t_r should be $\approx 50ms$. For unbalanced ringing C_B will become $C_{B1}C_{B2} \div (C_{B1} + C_{B2})$ in the above equation. More detail on Balanced and Unbalanced ringing is given in AN82.

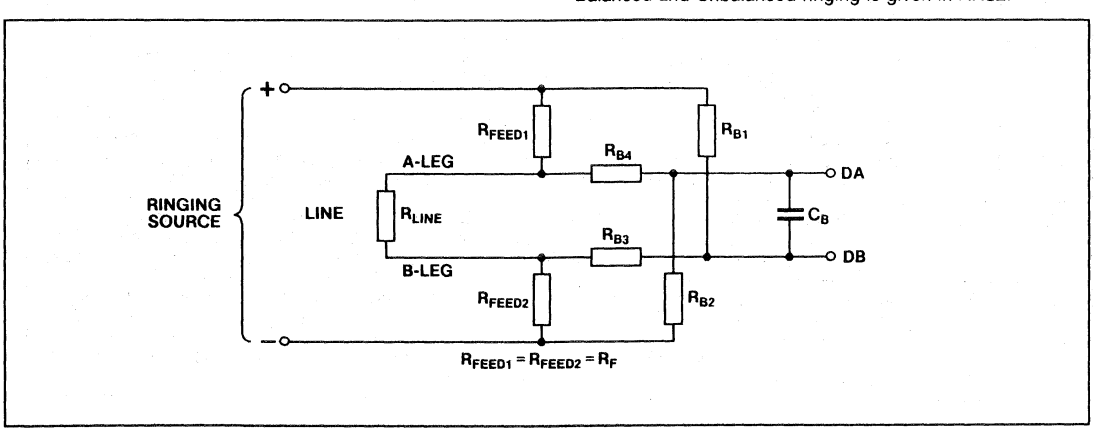


Fig. 12 Ring trip circuit (balanced ringing).

PIN DESCRIPTIONS

Symbol	Pin no.	Pin name and description
BGND	1	**Battery Ground (Power Input).** 0 Volts.
V_{REG}	2	**Regulated Voltage (Negative Power Input).** The voltage at this pin is compared to that required for line feed, and the result is used to control the voltage regulator.
V_{CC}	3	**Positive Supply (Power Input).** +5 Volts.
RINGR	4	**Ring Relay Driver Output (Pull-up Output).** This output is designed to drive a relay, when used together with the V_{BAT} supply.
TESTR	5	**Test Relay Driver Output (Pull-up Output).** This output is designed to drive a relay, when used together with the V_{BAT} supply.
+CH	6	**Switching Regulator (Chopper) Output (Negative Power Output).** Chopper switch transistor collector. An internal regulator controls the mark/space ratio of the switching waveform to maintain V_{REG} (pin 2) at the required voltage.
V_{BB}	7	**Battery Voltage (Negative Power Input).** This is the -62 Volt battery supply pin. It is connected to the chopper switch emitter.
SUB	8	**Substrate (Decoupling Node).** An external decoupling capacitor (0.33µF) should be connected between this pin and AGND.
CHS	9	**Line Feed Regulator (Chopper) Stabilising Network.** This is the input to the voltage comparator which is used to control the switching regulator.
CHCLK	10	**Line Feed Regulator (Chopper) Clock (Digital Input).** This is the positive edge triggered, 256kHz clock input for the voltage regulator, which will free run in the absence of an input signal.
D3	11	**Control Input (Digital Input).** Enables the Test relay driver output pin.
E1	12	**Control Input (Digital Input).** Selects the line status detector (Loop or Ground Key).
$\overline{DET}$	13	**Detector Data output (Digital Output).** This pin outputs the status of the detector which has been selected by D0 - D3.
D1 D2 D0	14 15 16	**Control Input (Digital Input)** **Control Input (Digital Input)** **Control Input (Digital Input)** These inputs determine the SLIC operating mode, and control the ring relay, selection of ringing and non-ringing modes, line polarity, line status and line detector.
RDC	17	**DC Reference Voltage (Voltage Output).** A reference voltage of ±2.5 Volts (depending on line polarity), is output at this pin, excepting Saturation Guard operation.
AGND	18	**Analog Ground (Analog Reference Node).** This is the ground reference pin for the analog signals. It also provides a ground reference for the Digital Interface. Signal reference and decoupling connections should be separately run to this pin.
RSN	19	**Receive Summing Node (Current Input).** The current which is input on this pin is used to control the transverse current at LA and LB.
V_{EE}	20	**Negative Supply (Power Input).** -5 Volts.
V_{TX}	21	**Transmit Voltage (Voltage Output).** The voltage output at this pin is equal to the difference between the voltage (V_{LA}-V_{LB}) and the differential DC voltage (V_{HPA}-V_{HPB}), multiplied by the 2 to 4-wire voltage gain.
HPA HPB	22 23	**High Pass A, High Pass B - AC/DC separation (Voltage Inputs).** These inputs sense the DC feed voltages on the LA and LB pins respectively. Under normal operation they are connected to LA and LB respectively by internal resistors and should be connected as shown in Fig. 11.
RD	24	**Loop Detection Control (Current Output / Voltage Input).** This pin outputs a current which is linearly related to the transverse loop current through LA and LB. The current is used to develop a voltage at this pin which determines On/Off Hook in relation to an internal reference (with hysteresis).
DA DB	25 26	**Ring Trip Detector A, Ring Trip Detector B (Voltage Inputs).** These are the A and B inputs to the internal ring trip comparator. The output of the comparator controls the ring trip output on $\overline{DET}$.
LA LB	27 28	**A Line Transceiver, B Line Transceiver (Current Outputs / Voltage Inputs).** These two pins form the 2 wire port connecting to the subscriber loop.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Range - see page 3-45)

Test conditions (unless otherwise stated)

V_{CC} = +5.0V, V_{EE} = –5.0V, V_{BAT} = –63V (see note 3), $V_{AGND} = V_{BGND}$, T_{AMB} = +25°C, V_{IL} = 0.7V and V_{IH} = 2.0V. Test circuit Fig. 26. Voltages are measured with respect to analog ground (V_{AGND}). Typical figures are for design aid only; they are not guaranteed and are not subject to production testing.

Supply Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply (V_{CC}) current, disconnect mode	I_{CC1}			6	mA	
Positive supply (V_{CC}) current, standby mode	I_{CC2}			11	mA	On / Off-Hook, I_L = 0
Positive supply (V_{CC}) current, active mode	I_{CC3}			11	mA	On / Off-Hook, I_L = 0
Negative supply (V_{EE}) current, disconnect mode	I_{EE1}			3	mA	
Negative supply (V_{EE}) current standby mode	I_{EE2}			9	mA	On / Off-Hook, I_L = 0
Negative supply (V_{EE}) current active mode	I_{EE3}			9	mA	On / Off-Hook, I_L = 0
Battery supply (V_{BB}) current disconnect mode	I_{BB1}			1.5	mA	
Battery supply (V_{BB}) current standby mode	I_{BB2}			5	mA	On-Hook, I_L = 0
Battery supply (V_{BB}) current active mode	I_{BB3}			6	mA	On-Hook, I_L = 0
Positive supply (V_{CC}) rejection ratio (supply to 2-wire transverse)	P_{SRT}	20			dB	See Fig.13 and note 1 ; 50mV on V_{CC}, 300-3400Hz, $R_1 \leq 1840\Omega$, $E_L = V_R = 0V$
Positive supply (V_{CC}) rejection ratio (supply to 2-wire longitudinal)	P_{SRL}	20			dB	See Fig.18 and note 1 ; 50mV on V_{CC}, 300-3400Hz
Negative supply (V_{EE}) rejection ratio (supply to 2-wire transverse)	N_{SRT}	10			dB	See Fig.13, notes 1 &2 ; 50mV on V_{EE}, 300-3400Hz, $R_1 \leq 1840\Omega$, $E_L = V_R = 0V$
Negative supply (V_{EE}) rejection ratio (supply to 2-wire longitudinal)	N_{SRL}	20			dB	See Fig.18 and note 1 ; 50mV on V_{EE}, 300-3400Hz
Battery supply (V_{BB}) rejection ratio (supply to 2-wire transverse)	B_{SRT}†	15			dB	See Fig.13 and note 1 ; 50mV on V_{BAT}, 300-3400Hz, $R_1 \leq 1840\Omega$, $E_L = V_R = 0V$
Battery supply (V_{BB}) rejection ratio (supply to 2-wire longitudinal)	B_{SRL}†	15			dB	See Fig.18, notes 1&2 ; 50mV on V_{BAT}, 300-3400Hz
Power dissipation, active state	P_{WA}			1.00	W	Off-Hook, R_L = 0-∞Ω
Power dissipation, standby state	P_{WD1}			0.35	W	On-Hook, I_L = 0
Power dissipation, standby state	P_{WD2}			0.75	W	Off-Hook, R_L = 0-∞Ω

NOTES

1. Non production test; figures are guaranteed by characterisation.
2. Parameter shown thus:† will degrade with battery voltages below 59V.
3. Battery voltage V_{BAT} is generally defined. The corresponding V_{BB} voltage is assumed to be 0.7V more positive than V_{BAT} allowing for the diode drop in D_2, Fig. 26.

Analog Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
2-wire port, low frequency overload level	V_{OABL}	– 3.1		+ 3.1	V (pk)	See Fig. 13 & note 4: V_R = 1000 Hz, EL = 0V
2-wire port, high frequency overload level	V_{OABH}	– 2.0		+ 2.0	V (pk)	See Fig. 13 & note 5: EL = 0V, V_R = 16kHz, R1 = 200Ω
2-wire port,longitudinal input impedance, off-hook	Z_{LL1}			35	Ω/wire	See Fig. 14: f < 100 Hz Z_L = 600Ω
2-wire port,longitudinal input impedance, on-hook	Z_{LL2}			35	Ω/wire	See Fig. 15: f < 100 Hz Z_L = 600Ω
Longitudinal current limit, active state	ILL_A	17.5			mA/wire (rms)	See Fig. 16 & note 6: E_R = – 10dBm 700-1100Hz, Z_L = 600Ω
Longitudinal current limit, standby state	ILL_S	12.5			mA/wire (rms)	See Fig. 16 & note 6: E_R = – 10dBm 700-1100Hz, Z_L = 600Ω
Longitudinal current limit, active state, B leg	ILL_B	63			mA	ILL_B is current in B leg: B leg = 0V via 600Ω, A leg O/C, V_{BAT} = –62V
4-wire transmit port, overload level	V_{OT}	– 3.1		+ 3.1	V (pk)	See Fig. 13 & note 4: f = 1000 Hz, V_R = 0V 4-wire load ≥ 25kΩ
4-wire transmit port, offset voltage	V_{TOFF}	– 30		+ 30	mV	See Fig. 13: V_R = 0
4-wire transmit port,output impedance	Z_T			20	Ω	See Fig. 13: V_R = 0V
Transmit (2 to 4-wire) voltage gain	G_T	– 0.1		+ 0.1	dB	See Fig. 13: EL = 0dBu (see note 7), 1kHz, V_R = 0V
4-wire receive port, low frequency voltage gain	G_{RL}	– 0.2		+ 0.2	dB	See Fig. 19: V_R = 2.6dBu, 1kHz
4-wire receive port, high frequency voltage gain	G_{RH}	– 3.7	– 2.7	– 1.7	dB	See Fig. 19: V_R = 2.6dBu, 15kHz
4 to 4-wire voltage gain	$G_{RT} \times G_{TT}$	– 0.2		+ 0.2	dB	See note 8
2-wire to 4-wire frequency response	F_{24}	– 0.1		+ 0.1	dB	See Fig. 13 & note 9: V_R = 0, EL = 0dBu, 200-3400Hz,
4-wire to 2-wire frequency response	F_{42}	– 0.1		+ 0.1	dB	See Fig. 13 & note 9: EL = 0, V_R = 0dBu, 200-3400Hz
4 to 4-wire frequency response	$F_{44} = F_{24T} \times F_{42T}$	– 0.1		+ 0.1	dB	See note 10
Gain linearity, 2-wire to 4-wire	G_{L24}	– 0.1		+ 0.1	dB	See Fig. 13 & note 11: V_R = 0, EL = + 7 to – 59 dBu, 1kHz
Gain linearity, 4-wire to 2-wire	G_{L42}	– 0.1		+ 0.1	dB	See Fig. 13 & note 11: EL = 0V, V_R = + 3 to –64 dBu, 1kHz

4. Overload occurs when distortion is 2% of total signal in the range 300-3400Hz.
5. Overload occurs when distortion is 2% of total signal in the range 20kHz to 100kHz.
6. E_{LL} = 50Hz. Amplitude of I_{LL} when signal-to-distortion ratio at $V_T \leq 30$dB.
7. dBu is defined thus: 0dBu is equivalent to the voltage at 0dBm when loaded with 600Ω ($0.775V_{RMS}$).
8. G_{RT} is measured as G_R, G_{TT} is measured as G_T.
9. Response is measured with respect to 1kHz
10. F_{24T} is measured as F_{24}, F_{42T} is measured as F_{42}.
11. Linearity is measured with respect to gain at 0dBu.

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
4-wire idle channel noise (psophometric weighted)	N_{P4}			– 75.0	dBup	See Fig. 14: V_{BAT} = – 48V, $E_L = V_R$ = 0V
4-wire idle channel noise (psophometric weighted)	N_{P4B}†			– 75.0	dBup	See Fig. 14: V_{BAT} = – 48V, $E_L = V_R$ = 0V
2-wire idle channel noise (psophometric weighted)	N_{P2}			– 76.0	dBup	See Fig. 14: V_{BAT} = – 48V, $E_L = V_R$ = 0V
2--wire idle channel noise (psophometric weighted)	N_{P2B} †			– 76.0	dBup	See Fig.13 & note 2: $E_L = V_R$ = 0V, 1140Ω < R1 ≤ 1840Ω
2-wire differential noise (wide band)	N_{D2}		Fig.20			See Fig. 19 & note 6
2-wire longitudinal noise (wide band)	N_{L2}		Fig.21			See Fig. 21 & note 1; E_R = 0V, Z_L ≤ 1840Ω
Regulator noise, 4-wire receive, single frequency	N_{R4}			– 55.0	dBu	See Fig. 17 & note 1
Regulator noise, 2-wire transverse, single frequency.	N_{RT}			– 50.0	dBu	See Fig. 17 & note 1; measure V_{A-B}.
Regulator noise, 2-wire longitudinal, single frequency.	N_{RL}			– 50.0	dBu	See Fig. 17 & note 1; measure V_{LL}.
Longitudinal balance, longitudinal to transverse	B_{L-T1}	50.0			dB	See Fig. 14, & notes 12,13: Z_L = 600Ω, V_R = 0V, E_{LL} = + 2dBu 40-4000Hz
Longitudinal balance, longitudinal to transverse	B_{L-T2}	50.0			dB	See Fig. 14, & notes 2, 13: Z_L = 1.6kΩ, V_R = 0V, E_{LL} = + 2dBu 40-4000Hz
Longitudinal balance, trans-long + long-trans	B_{T-L+} B_{L-T1}	102			dB	See Figs. 14, 20 & note 13: Z_L = 600Ω, V_R = 0V, E_{LL} = + 2dBu 300-800Hz
Longitudinal balance, trans-long + long-trans	B_{T-L+} B_{L-T2}†	102.0			dB	See Figs.14, 20 & notes 2, 13: Z_L = 1.6kΩ, V_R = 0V, E_{LL} = + 2dBu 300-800Hz
Longitudinal signal rejection, longitudinal to 4-wire	RJ_{L4A}	50.0			dB	See Fig. 14 & note 13: Z_L = 600Ω, V_R = 0V, E_{LL} = + 2dBu 40-4000Hz
Longitudinal signal rejection, longitudinal to 4-wire	RJ_{L4B}†	50.0			dB	See Fig. 14 & notes 2, 13: Z_L = 1600Ω, V_R = 0V, E_{LL} = + 2dBu 300-4000Hz
Longitudinal signal generation, 4-wire to longitudinal	GN_{4-L}†	42.0			dB	See Fig. 21 & notes 2, 13; Z_L = 600 or 1.6kΩ, E_R = 2.6dBu 300/800Hz,
Harmonic distortion, 4 to 2-wire	T_{HD1}			– 50.0	dB	See Fig. 13 & note 14: V_R = 0dBu, 1kHz
Harmonic distortion, 4 to 2-wire, 16kHz on-hook	T_{HD2}†			– 37.0	dB	See Fig.13 & notes 2,15,16: V_R = 0dBu 1kHz, R1 = ∞
Intermodulation distortion	ID_{A-B1}			– 40.0	dB	See Fig. 13 & note 1017: $V_R = f_1 + f_2$, $f_1 = f_2$ = –4 to –21dBu
50Hz intermodulation distortion	ID_{A-B2}			– 49.0	dB	See Fig. 13 & note 1: f_1 = –9dBu 300-3400Hz, f_2 = –23dBu 50Hz, $V_R = f_1 + f_2$

NOTES
12. Parameter will degrade for some values of V_{BAT}.
13. V_{BAT} is such that saturation guard is inactive.
14. Distortion measured in the bandwidth 300-3400 Hz.
15. Distortion measured in the bandwidth 20-100kHz.
16. V_R adjusted so that V_{A-B} = 0.5V RMS, 16kHz.
17. f_1 & f_2 in the range 300-3400Hz, $f_1 \div f_2$ = non-integer. Measure $(2f_1-f_2)$ relative to f_1 or f_2 level.

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Loop current, active state constant current region	I_{ACT1}	38	40	42	mA	See Fig.26 & note 18: $Z_L = 600\Omega$, $R_{DC} = 12.5k\Omega$.
Loop current, active state	I_{ACT2}	25			mA	See Fig.26 & note 19: $Z_L = 1840\Omega$ $R_{DC} = 12.5k\Omega$
2-wire current, disconnected state	I_{DCT}			1.0	mA	LA to LB or Ground, or both LA and LB to Ground.
2-wire current, disconnect A standby B mode	I_{DASB}			1.0	mA	LA to LB or Ground, $Z_L = 600\Omega$
Loop current, standby state, normal(+) or reverse(–)	I_{LIM}	18.0		22.0	(±)mA	See Fig.26 & note 20 ; $Z_L = 600\Omega$
Loop detector, on-hook current threshold	I_{DETON}	I_{DETON} –15%	I_{DETON}	I_{DETON} +15%	A	See Fig.26 & note 21: $I_{DETON} = 410 \div R_{TH}$
Loop detector, off-hook current threshold	I_{DETOFF}	I_{DETOFF} –15%	I_{DETOFF}	I_{DETOFF} +15%	A	See Fig.26 & note 21: $I_{DETOFF} = 465 \div R_{TH}$
Loop detector hysteresis	I_{DETHYS}	0.5		2.0	mA	
Ring trip detector offset voltage	V_{RTO1}	– 50		+ 50	mV	See Fig.24: R = 200KΩ $V_{BB} < V_{CMM} < -2V$
Ring trip detector offset voltage	V_{RTO2}	– 25		+ 25	mV	See Fig.24: R = 0Ω $V_{BB} < V_{CMM} < -2V$
Ring trip detector bias current	I_{RTB}	– 1.0			µA	See Fig.24: $V_{BB} < V_{CMM} < -2V$ $I_{RTB} = \frac{1}{2}(I_{RTDA} + I_{RTDB})$
Ground key active mode, $\overline{DET} = 0$	R_{G10}			900	Ω	See Fig.25 & note 22: SW1 Closed, RW = 300Ω.
Ground key active mode, $\overline{DET} = 1$	R_{G11}	10K			Ω	See Fig.25 & note 22: SW1 Closed, RW = 300Ω.
Earthcall active mode, $\overline{DET} = 0$	R_{G20}			1K7	Ω	See Fig.25, notes 19 & 22: SW1 Open, RW = 300Ω.
Earthcall active mode, $\overline{DET} = 1$	R_{G21}	9K7			Ω	See Fig.25 & note 22: SW1 Open, RW = 0Ω.
Earthcall disconnect A standby B mode, $\overline{DET} = 0$	R_{G30}			1K7	Ω	See Fig.25, notes 19 & 22: SW1 Open, RW = 300Ω.
Earthcall disconnect A standby B mode, $\overline{DET} = 1$	R_{G31}	9K7			Ω	See Fig.25 & note 22: SW1 Open, RW = 0Ω.
Relay drivers, saturation voltage (active)	V_{SAT}	– 2			V	I = 25mA drawn from BGND
Relay drivers, leakage current (non-active)	I_{LK}			0.1	mA	V_{OUT} = Voltage at pin 8
Relay drivers, clamp voltage	V_{CLMP}	V_{BAT} – 2.5			V	I = 25mA into pin

NOTES

18. Constant current in Active mode $= 500 \div R_{DC}$. Tolerance on current is ±2mA for $12.5k \leq R_{DC} \leq 15.625k\Omega$.
19. Applied $V_{BAT} = -63V$.
20. Constant current in Standby mode $= 250 \div R_{DC}$. Tolerance on current is ±2mA for $12.5k \leq R_{DC} \leq 15.625k\Omega$.
21. Differential loop current between LA and LB. The Loop Detector contains hysteresis. Thresholds determined by R_{TH} Fig 26.
22. For polarity reversed state, connections to LA and LB are reversed.

Digital Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Input low voltage (D_0-D_3, E_1, CHCLK)	V_{IL}			0.8	V	
Input high voltage (D_0-D_3, E_1, CHCLK)	V_{IH}	2.0			V	
Input low current (D_0-D_3, E_1, CHCLK)	I_{IL}			–0.25	mA	V_{IL} = 0.4V
Input high current (D_0-D_3, E_1, CHCLK)	I_{IH}			0.04	mA	V_{IH} = 2.4V
$\overline{DET}$ output low voltage	V_{OL}			0.4	V	I_{OL} = 0.8mA
$\overline{DET}$ output high voltage	V_{OH}	2.4			V	I_{OH} = 0.1mA
$\overline{DET}$ output, internal pull-up	R_{OUT}	10		20	kΩ	
Propagation delay, E_1 to $\overline{DET}$	t_{PD}			4	μs	$\overline{DET}$ 6.2kΩ to V_{CC}, 15pF to BGND
Loop detector make response time	t_{LM}			5	ms	Z_L = 0/600/1600Ω (V_{OL} < 0.45)
Loop detector break response time	t_{LB}			5	ms	Z_L = 0/600/1600Ω (V_{OL} > 2.35)
CHCLK input frequency	F_{CLK}		256		kHz	
CHCLK input minimum pulse width	T_{CLK}		500		ns	

Recommended Operating Range

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply voltage	V_{CC}	+4.75	5.0	+5.25	V	
Negative supply voltage	V_{EE}	– 4.75	– 5.0	– 5.25	V	
Battery supply voltage	V_{BAT}	– 40.5	– 62	– 64	V	See note 23
Battery ground voltage	V_{BGND}	– 0.1		+0.1	V	
Ambient temperature	T_{AMB}	0		+70	°C	

NOTE 23. Some parameters, shown thus: † in the Electrical Characteristics, degrade with battery voltages below 59V; the SL374 is optimised for performance with a battery supply of –62V.

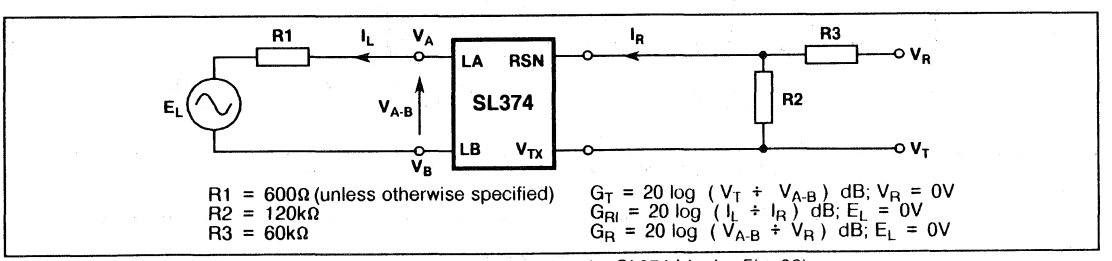


Fig.13 Test configuration (Note the SL374 block = Fig. 26).

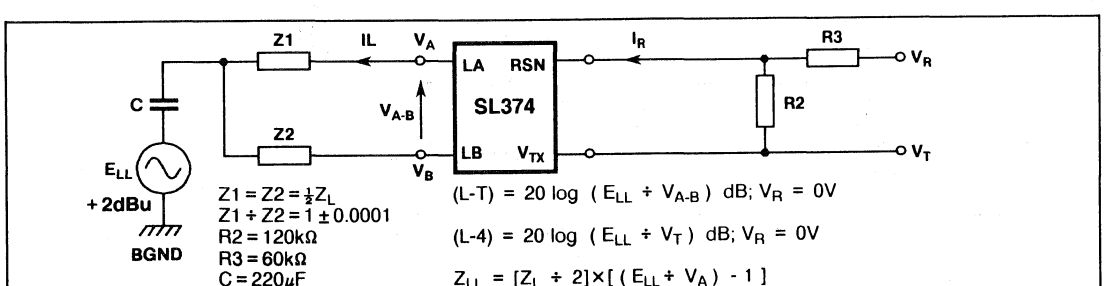


Fig.14 Test configuration (Note the SL374 block = Fig. 26).

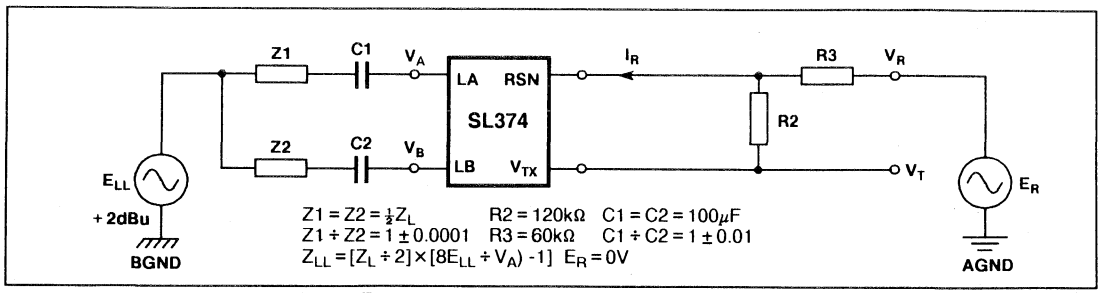


Fig.15 Test configuration (Note the SL374 block = Fig. 26).

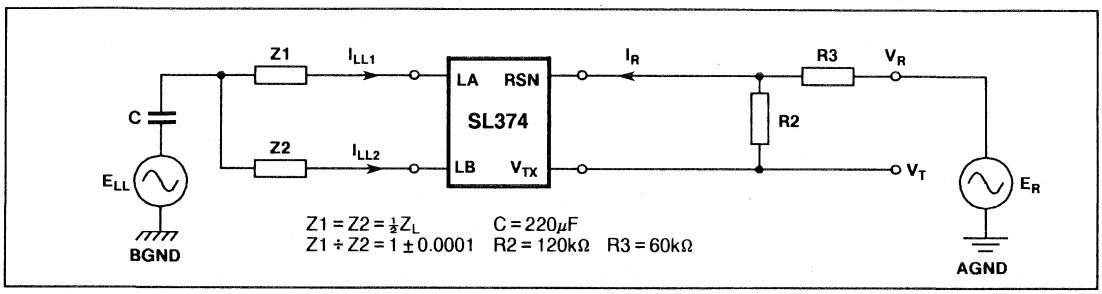


Fig.16 Test configuration (Note the SL374 block = Fig. 26).

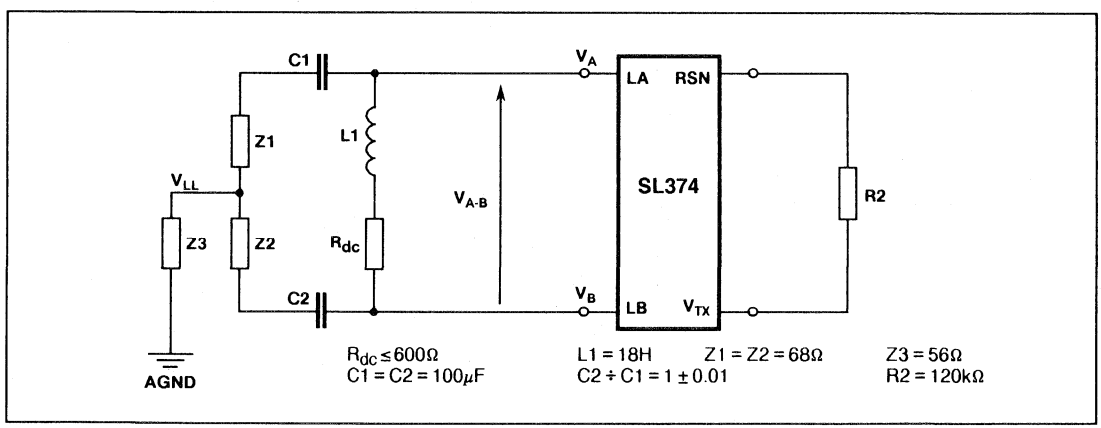


Fig.17 Test configuration (Note the SL374 block = Fig. 26).

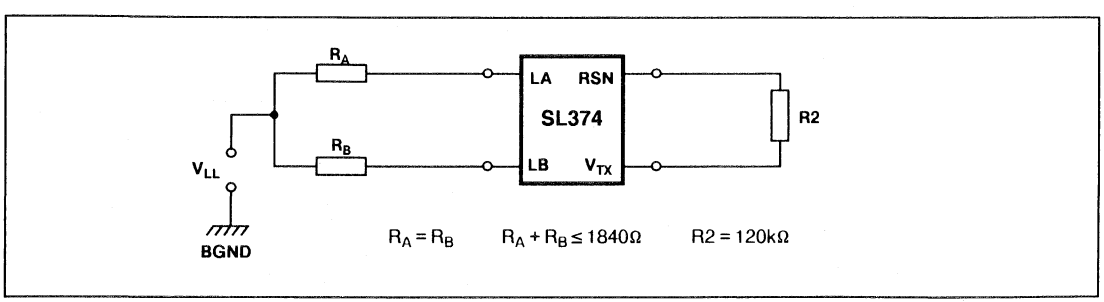


Fig.18 Test configuration (Note the SL374 block = Fig. 26).

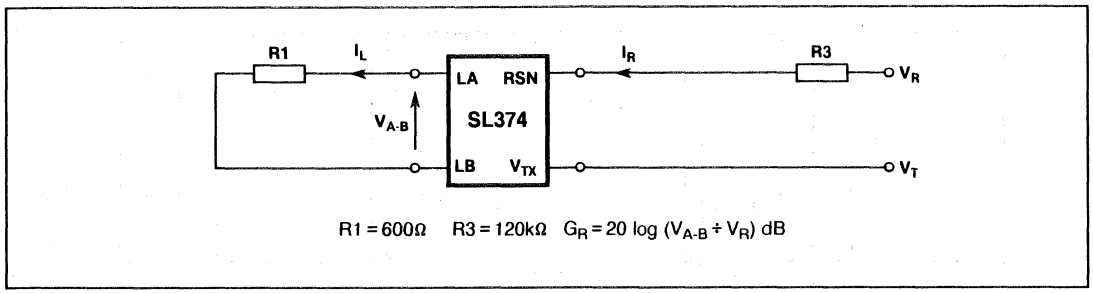


Fig.19 Test configuration (Note the SL374 block = Fig. 26)

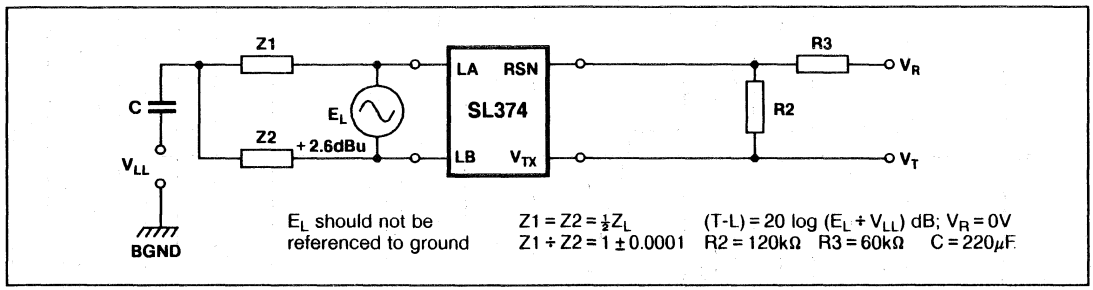


Fig.20 Test configuration (Note the SL374 block = Fig. 26)

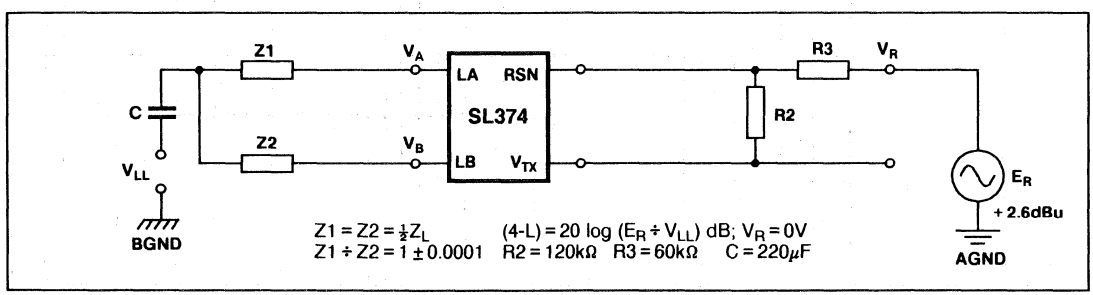
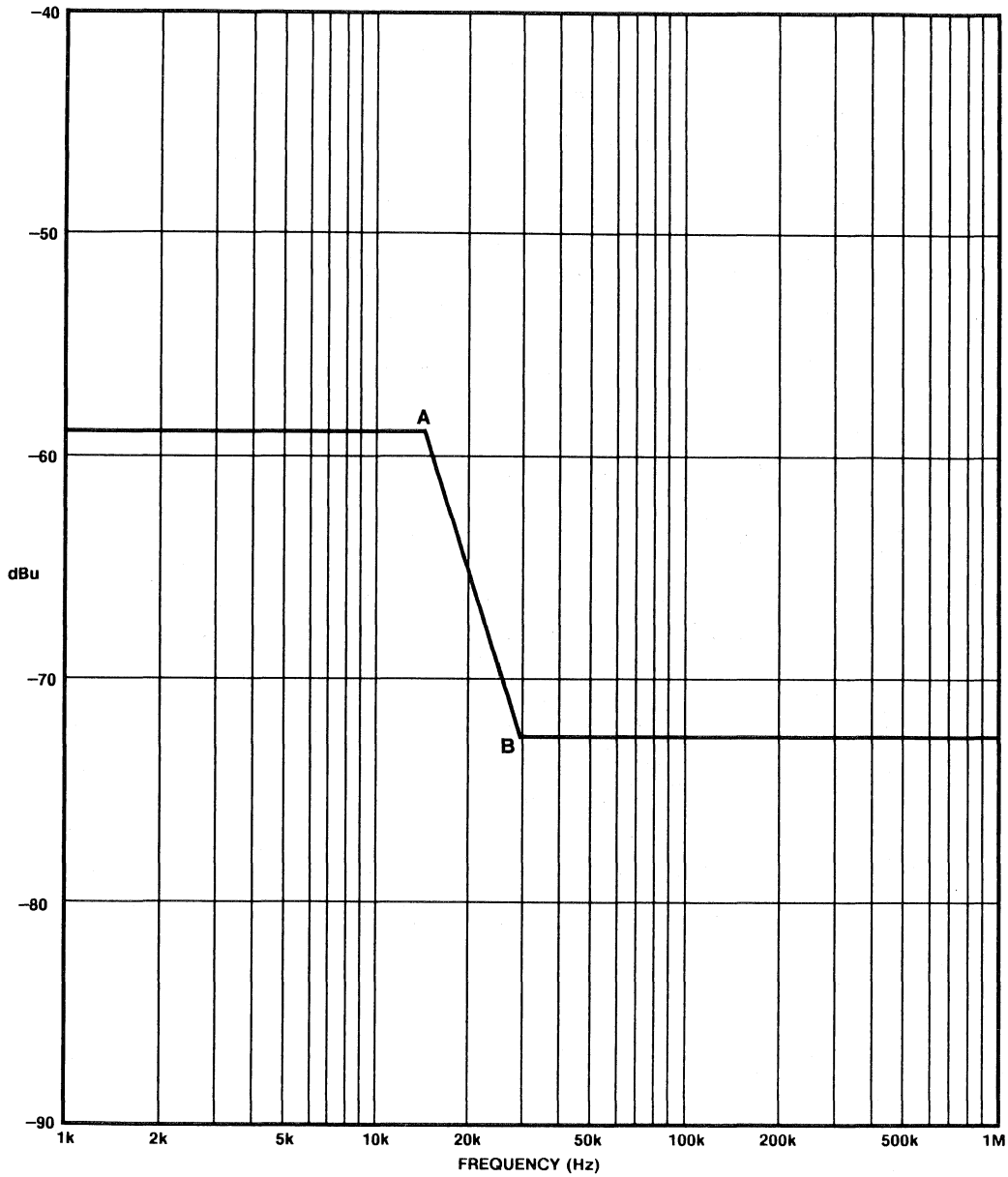


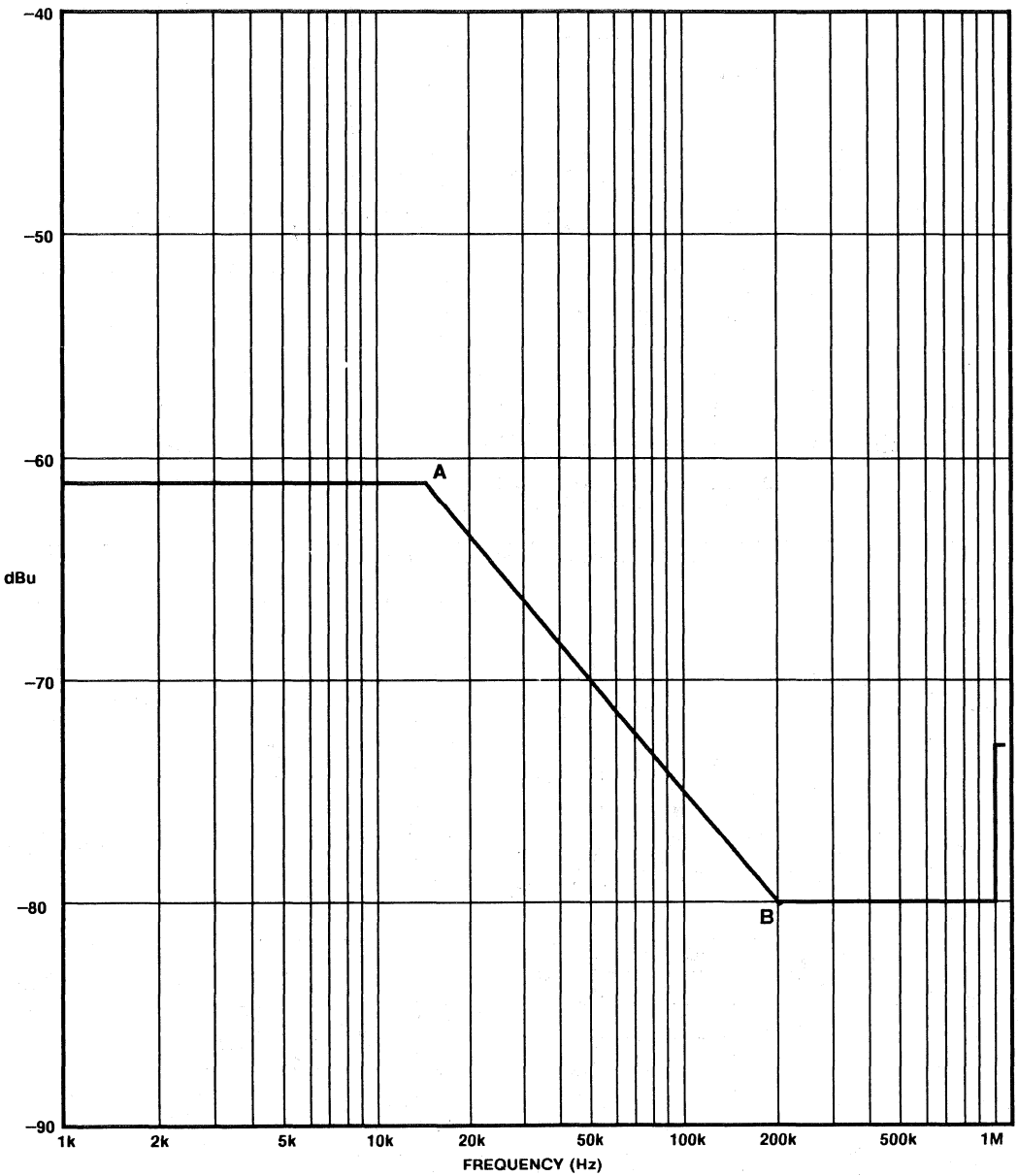
Fig.21 Test configuration (Note the SL374 block = Fig. 26).



FREQUENCY AT CENTRE OF BAND

A = 13.5kHz −59dBu
B = 30kHz −73dBu
Bandwidth = 3kHz Minimum Centre Frequency = 1.6kHz
V_{A-B} < −73dBu. f > 1MHz

Fig.22 2-Wire differential noise



FREQUENCY AT CENTRE OF BAND

A = 15kHz –61dBu
B = 200kHz –80dBu
Bandwidth = 3kHz
V_{LL} < –73dBu. f > 1MHz

Fig.23 2-Wire longitudinal noise

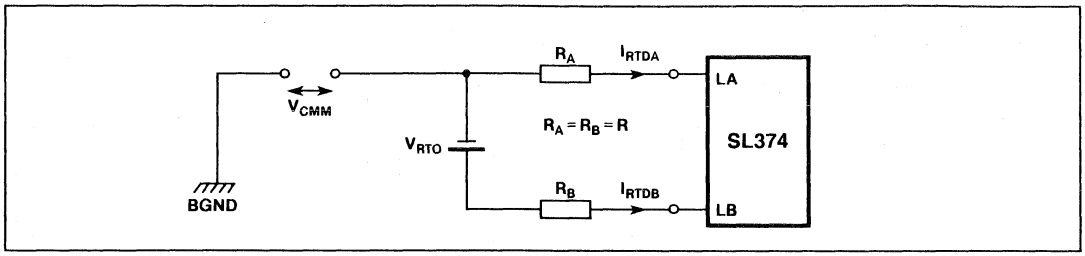


Fig.24 Test configuration (Note the SL374 block = Fig. 26)

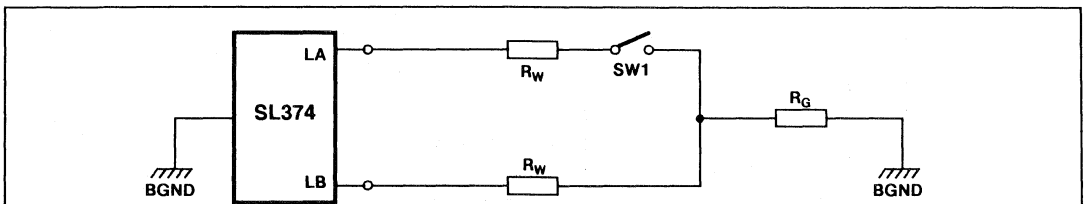
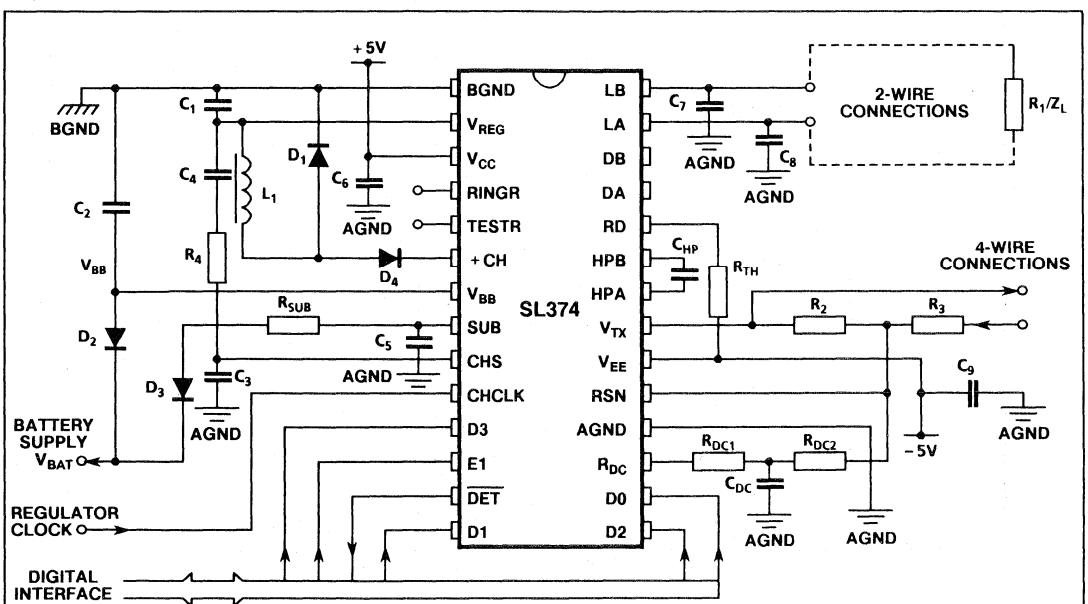


Fig.25 Test configuration (Note the SL374 block = Fig. 26)



C_1 = 470n	C_6 = 100n	C_{DC} = 390n	L_1 = 1mH, 47Ωcoil resistance	R_1 as Test Configuration
C_2 = 470n	C_7 = 2.2n	D_1 = 100V,100mA	R_{SUB} = 100Ω	R_2 as Test Configuration
C_3 = 1.5n	C_8 = 2.2n	D_2 = 100V,100mA	R_{TH} = 42.44kΩ (see Elec. Char.)	R_3 as Test Configuration
C_4 = 47n	C_9 = 100n	D_3 = 100V,100mA	$R_{DC1} = R_{DC2}$ = 6.25kΩ(see Elec. Char.)	R_4 = 910Ω
C_5 = 330n	C_{HP} = 330n	D_4 = 100V,100mA	Z_L = see Elec. Char.	

For all tests assume AGND = BGND.

Fig.26 Test circuit for Figs. 13-21 and 24-25

ABSOLUTE MAXIMUM RATINGS* - Voltages are with respect to Analog ground (V_{AGND})

Parameter	Symbol	Value		Units
		Min.	Max.	
Battery supply voltage	V_{BB}	– 70	+ 0.4	V
Continuous battery ground voltage	V_{BGNDC}	– 0.3	+ 0.3	V
Positive supply voltage	V_{CC}	– 0.4	+ 6.5	V
Negative supply voltage	V_{EE}	– 6.5	+ 0.4	V
Subscriber line voltage on LA, LB or both, continuous	V_{LC}	– 70.0	+ 1.0	V
Subscriber line voltage on LA, LB or both, non-repetitive				
50 s duration	V_{LR1}		+ 1.2	V
10 s duration	V_{LR2}		+ 1.5	V
2 s duration	V_{LR3}		+ 2.0	V
140 ms duration	V_{LR4}		+ 3.0	V
Differential DC line current	I_{LDC}		150	mA
Switched regulator voltage (off) transient peak	V_{CH}		+ 1.0	V
Switched regulator current (on) transient peak	I_{CH}		150	mA
Switched regulator input voltage	V_{RI}	V_{BB}	0.0	V
Relay drivers output supply voltage	V_{RLY}	V_{BAT}		V
Relay drivers output source current	I_{RLY}		30	mA
Ring-Trip input voltage (DA or DB)	V_{RT}	V_{BB}	0	V
Ring-Trip input current (non-repetitive 10 ms pulse)	I_{RT}	– 2.0	+ 2.0	mA
Digital input voltage	V_{ID}	– 0.4	V_{CC}	V
Digital input current (sink)	I_{ID}		5.0	mA
Digital output voltage (non-active)	V_{OD}	– 0.3	V_{CC}	V
Digital output current (source)	I_{OD}		3	mA
Storage temperature	T_{ST}	– 55	+ 125	°C
Operating junction temperature †	T_{JOP}		+ 140	°C
Package power dissipation (DG28)	P_{PDG28}		1.5	Watts

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

† Circuit includes thermal protection such that T_{PROT} (MIN) = + 140°C.

DS2304-1.0

SL376

METERING SUBSCRIBER LINE INTERFACE CIRCUIT

The SL376 is a Subscriber Line Interface Circuit (SLIC) for use at the telephone exchange or PABX end of a telephone line.

It provides power feed, transmits and receives voice signals, controls ringing and detects Ground Key or Off-Hook conditions. These functions can be programmed to provide the flexibility required for different telephone networks. In addition, the SL376 allows injection of high frequency Meter Pulse signals on to the telephone line.

The SL376 is fabricated using bipolar technology.

FEATURES

- Low Power Line Feed via Regulator
- Constant Voltage Feed/Programmable Resistive Feed Independent of Battery
- Programmable AC Termination Impedance
- Good Longitudinal Balance
- Ground Key and Ring Trip Detection
- Programmable Off-Hook Detection
- Disconnect and Low Power Standby Modes
- A-Leg Disconnect, B-Leg Standby Mode
- Normal or Reversed Line Polarity Operation
- Supports High Frequency Meter Pulse Injection
- Ring Relay Driver
- Thermal Shut-Down Protection

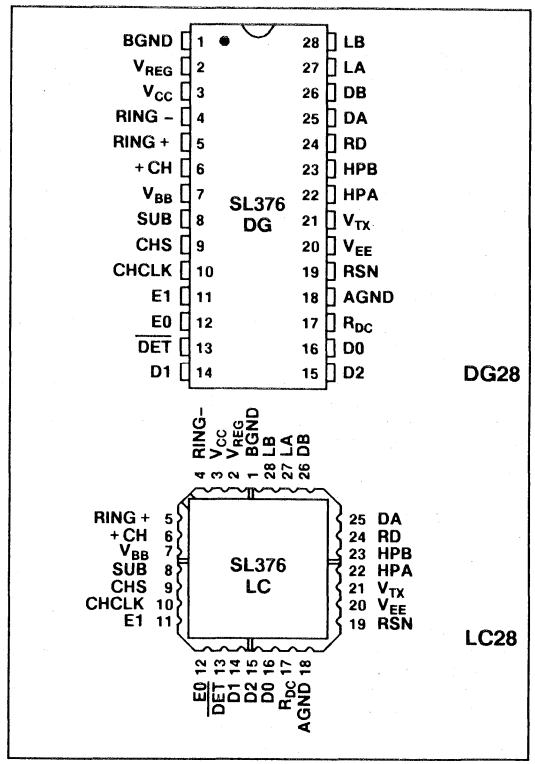


Fig. 1 Pin connections - top view (not to scale)

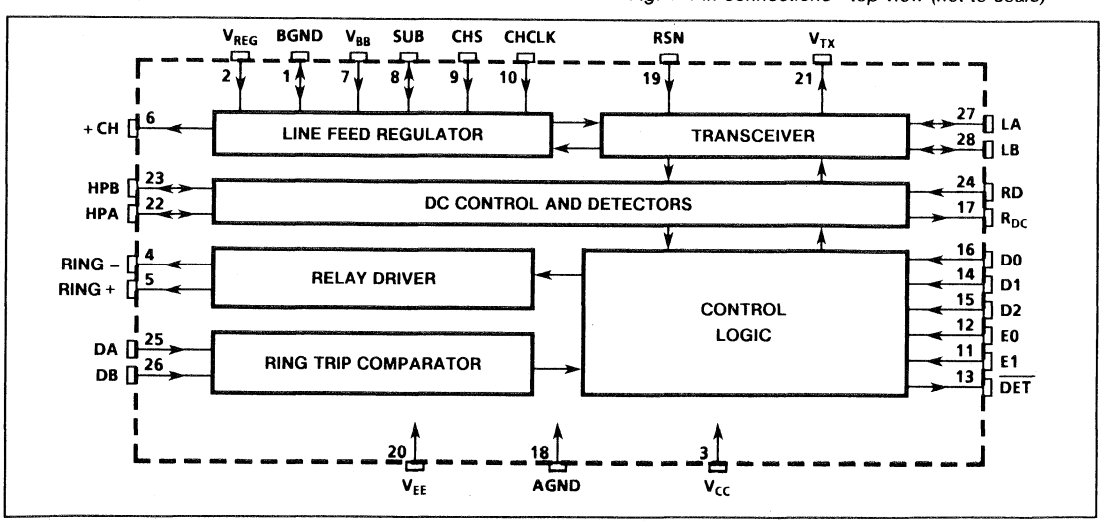


Fig. 2 : Functional Block Diagram

FUNCTIONAL OVERVIEW

The SL376 Metering Subscriber Line Interface Circuit (MSLIC), together with some external components, provides most of the line interface functions for ordinary or PABX line connections in a telephone network. It performs the interface between the two wire line and an ALAP (Analog Line Audio Processor)/COMBO, such as the GEC Plessey Semiconductors MV3010 PSLAC (Plessesy Subscriber Line Audio Circuit) DSP device.

The MSLIC circuit contains several functional blocks to achieve the design aims (Fig.2). Firstly, the Transceiver consists of the two wire port, pins LA and LB. These pins are fed from the 4-wire input (RSN) controlling AC conditions, and from the Line Feed Regulator and DC Control blocks, controlling DC conditions. The 2-wire transverse AC signal is fed onto the 4-wire transmit output, V_{TX}.

Power dissipation is minimised, under varying line conditions, by the Line Feed Regulator which adjusts the internal high voltage supply to that required for line feed. It consists of a switching regulator which can be synchronised to a 256kHz clock.

DC line conditions at the 2 wire interface are determined by the DC Control block. These DC conditions (modes of operation) are set by the Control Logic, which also monitors line status (On/Off-Hook) via the DC Control block detectors (Loop/Ground Key/Ring Trip). The control logic also controls the Ring Relay Driver for Ringing mode of operation.

A brief outline of the device functionality is given below, before a more detailed discussion of the MSLIC circuitry in the Functional Description section.

LINE FEED

Line loop (pins LA &LB) feeding is obtained from the battery supply (pin 7) by means of an internal power circuit, which can be set to different modes of operation (refer to Table 2). These modes are as follows:

Standby Mode

Standby mode is the MSLIC's low power mode in which the battery feed circuit limits the DC loop current to a level just sufficient to enable the MSLIC to detect current above the On/Off-Hook threshold. This mode is used when the subscriber is On-Hook, to save power, and is only used briefly when Off-Hook is detected (see Line Feed Regulator). Both the Loop and Ground Key detectors work in this mode.

Disconnect A and B Leg

This mode programs the SLIC such that the A and B leg output amplifiers are turned off, preventing current flow to the line.

Disconnect A, Standby B Leg

This is the MSLIC Standby mode with the A Leg amplifier turned off, so that current can only flow in the B Leg. In this state it is only possible to detect the application of a ground to the B Leg.

Active Mode

This is the normal operating mode with a call in progress. The MSLIC is used as a constant current feed device (unbalanced DC line feeding is performed), with the feed resistance being set by external resistors.

Polarity reversal

The polarity of the feeding voltage at the MSLIC can be reversed on command, in Active and Standby modes. All Active and Standby conditions apply equally to the respective reverse conditions. In these conditions the polarity of any DC parameter is reversed.

Ringing

This mode enables the Ring Relay output and selects the Ring Trip comparator. It does not provide DC line feed or AC ringing voltage which must be supplied externally (via the ring relay).

SUPERVISION

The MSLIC provides an Off-Hook (or loop) Detector (OHD), Ring Trip Detector (RTD) and a Ground Key Detector (GKD). These are described briefly below, in addition to the MSLIC on-chip thermal protection.

Off-Hook Detector

The Off-Hook Detector recognises the loop status by means of a threshold circuit. The OHD operates in Standby and Active modes (with or without polarity reversal), and in the presence of longitudinal currents. The detector threshold is nominally the same in Standby and Active modes, the actual level being externally programmable.

Ring Trip Detector

This detects when a subscriber goes off-hook during the application of a ringing signal (normally 25Hz) within a maximum delay of 150ms (determined by external components - see Applications section). The detector is active when the Ring Relay Driver is activated.

Ground Key Detector

The GKD circuit detects a current path from the A or B Leg to ground. It can be used in Standby, Active and Disconnect A Standby B modes.

Thermal Protection

In conditions which cause the chip temperature to rise above a critical level (around 140°C), the thermal protection will operate. This switches off the line current and therefore reduces power dissipation.

TRANSMISSION

The signal transmission functions include 2 to 4-wire and 4 to 2- wire conversions.

The 2-wire termination impedance of the MSLIC is programmed by external components. Transmit and Receive gain are fixed and are nominally –6dB and unity (0dB), respectively, with the 2-wire port terminated in a matched load.

All the transmission parameters apply when the MSLIC is operating in the presence of longitudinal currents, as specified in the Electrical Characteristics.

CONTROL

The MSLIC is provided with a digital interface for controlling the 2-wire line status and passing line status information to the line card/system hardware. The operating characteristics can be selected by hardware with external components (see Digital Interface).

SIGNALLING (METER PULSE INJECTION)

The injection of high frequency Meter Pulses (SPM) can be carried out through the MSLIC. This signal is added to the normal 4 wire receive signal at the RSN pin (pin 19). It could be externally switched into the receive path under control of an ALAP/PSLAC digital output.

The 4 wire transmit output, VTX, will include any meter pulse signalling. It may be necessary to add an external SPM notch filter in the final application solution, to prevent overload of the dynamic range of the ALAP/PSLAC analog input.

RINGING

The application of the ringing voltage to the subscriber line can be via a relay or suitable high voltage crosspoint, external to the MSLIC. This component is driven by the on-chip Ring Relay Driver. The relay is connected between RING+ and a +5V supply with RING– grounded, or between RING– and V_{BAT} with RING+ connected to a supply voltage between BGND and V_{CC}. When the MSLIC is set to RING mode, the Ring Relay Driver output will be activated to energise the ring relay. The relay should be connected so as to cause the line to be disconnected from the MSLIC and connected to a suitable ringing supply (continuous) voltage. Ring cadence can then be obtained by de-energising and re-energising the relay as required.

OVERVOLTAGE PROTECTION

Overvoltage protection is required to protect the SLIC from such line phenomena as lightning strikes, and induced AC signals from, or direct contact with, power lines. This protection can be realised with components external to the SL376 (refer to SL373/SL376 Application Note AN82).

TEST ACCESS

The testing of the subscriber line is achieved using components external to the SL376.

INTERFACES

The SL376 has three main interfaces to external circuitry. These are the 2-wire, 4-wire and Digital interfaces which are described below.

Subscriber Line Interface (2-wire port)

Pins LA and LB form the Subscriber Line Interface providing line feed, signalling supervision and voice transmission between the subscriber's apparatus and exchange. It exhibits very good balance about ground to minimise the crosstalk between adjacent pairs in the local cable and noise from longitudinal interference. The termination impedance is set externally by Z_{TX} (see Fig. 3 and Functional Description).

The 2-wire port is designed to offer a low impedance to any longitudinal signals that appear on the subscriber line and the resulting signal level at the 4-wire output port is minimised. It is able to handle longitudinal currents on the subscriber line in all modes of operation, except Disconnect, Ringing and Disconnect A Standby B modes when the MSLIC 2-wire port is no longer connected to the line.

Analog 4-wire interface

Two pins of the MSLIC (V_{TX} and RSN), together with associated grounds, provide the 4 wire interface to an ALAP or COMBO device. Both the transmit (V_{TX}) and receive (RSN) signals are unbalanced and have fixed gain settings. The V_{TX} pin has a low output impedance, whilst the RSN pin is a low impedance virtual earth input. The input current is normally a combination of the receive voice signal from the ALAP, line feed current programmed by the RDC pin (see Applications section), termination of the V_{TX} pin and injected Meter Pulse signals.

Hybrid Balancing is not provided on the SL376. This can be done by an ALAP such as the MV3010 PSLAC which uses DSP techniques, including an Adaptive Echo Cancellation feature.

Digital Interface

This is a parallel interface providing control of all the MSLIC operating modes and indication of line status information. It consists of the 6 pins as listed in Table 1, the functions of which are described in Table 2.

Pin designation	Pin description
D0	Data input
D1	Data input
D2	Data input
E0	Detector data output enable
E1	Detector select input
$\overline{DET}$	Detector data output

Table 1 Digital interface pin designation

Mode	D2	D1	D0	E0	$\overline{DET}$ output status (Note 2)	
					E1 = 0	E1 = 1
Disconnect A & B Legs	0	0	0	1	(Invalid)	(Invalid)
Ringing	0	0	1	1	Ring Trip (Note 3)	-
Active(non-ringing)	0	1	0	1	Loop Detect	Ground Key
Standby	0	1	1	1	Loop Detect	Ground Key
Disconnect A,standby B	1	0	0	1	Ground Key	(Invalid)
Reserved	1	0	1	1	-	-
Active, polarity reversed	1	1	0	1	Loop Detect	Ground Key
Standby, polarity reversed	1	1	1	1	Loop Detect	Ground Key
As selected by D2-D0,E1 (note 1)	0/1	0/1	0/1	0	1 (off)	1 (off)

NOTES

1. D2, D1, D0 still change MSLIC status even though $\overline{DET}$ output is forced to 1 (5V).
2. $\overline{DET}$ = 1 for On-Hook (high line impedance), $\overline{DET}$ = 0 for Off-Hook (low line impedance).
3. $\overline{DET}$ = 1 for Voltage DA > DB , $\overline{DET}$ = 0 for Voltage DA < DB.

Table 2 Digital interface functional description.

FUNCTIONAL DESCRIPTION

VOICE TRANSMISSION AND RECEPTION

It is conventional to assign the signal directions from the point of view of the served telephone set. The receive direction is towards the served telephone and the transmit direction is from it.

The basic voice circuit for the device is shown in Fig.3. The current which flows on the line, into LA and out of LB, is 1000 times the current which flows into RSN and through the device to AGND.

The AC voice current flowing into RSN is composed of the current from V_{RX} through Z_{GR}, which controls the signal received at the remote telephone and a current from V_{TX} through Z_{TX} which controls the termination impedance and a current from V_{MT} through Z_{GM} for injection of Meter Pulse signals. There is also a DC current at RSN which is analysed later in the discussion on DC line feed.

The 2-wire termination impedance is $Z_{AB} = (Z_{TX} \div \frac{1}{2}\alpha)$ where α ($\simeq 1000$) is the current gain between RSN and I_L (see Fig.3). This can be checked by setting V_{RX} to zero. The factor of $\frac{1}{2}$ is due to the nominal Transmit Voltage Gain of –6dB, which prevents overload of the dynamic range during Meter Pulse signalling.

The receive gain, for normal voice signals (at V_{RX}), is inversely proportional to Z_{GR}. The actual value, which is negative, can be obtained by setting $(V_L)_{ac}$ equal to zero in Fig.3. This gives:

AC voltage between LA and LB $(V_{LA}-V_{LB})_{ac}$

$$= (V_{LA} - V_{LB}) - (V_{HPA} - V_{HPB})$$

$$= (I_L)_{ac} \times \{Z_{AB} \| Z_L\}$$

$$= -\left(\frac{Z_L \times \frac{Z_{TX}}{\frac{1}{2}\alpha}}{Z_L + \frac{Z_{TX}}{\frac{1}{2}\alpha}}\right) \frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}$$

i.e. minus the ratio of the line and terminating impedances (Z_L and $Z_{TX} \div \frac{1}{2}\alpha$) in parallel, to the receive impedance divided by the current gain ($Z_{GR} \div \alpha$). This expression simplifies to :

$$= \frac{-2\alpha Z_L Z_{TX} V_{RX}}{(\alpha Z_L + 2Z_{TX})Z_{GR}}$$

To obtain receive gain for the meter pulse input, V_{MT}, this will have a similar expression except that Z_{GM} is substituted for Z_{GR}.

In the transmit direction, the voltage at V_{TX} is the superposition of the voltage from the line, with the voltage produced on the line from V_{RX}, i.e:

$$V_{TX} = \frac{1}{2}\left[\left(\frac{\frac{Z_{TX}}{\frac{1}{2}\alpha}}{Z_L + \frac{Z_{TX}}{\frac{1}{2}\alpha}}\right) V_L - \left(\frac{Z_L \times \frac{Z_{TX}}{\frac{1}{2}\alpha}}{Z_L + \frac{Z_{TX}}{\frac{1}{2}\alpha}}\right) \frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}\right]$$

This expression simplifies to :-

$$V_{TX} = \frac{[(V_L)_{ac} Z_{GR} - \alpha Z_L V_{RX}] Z_{TX}}{(\alpha Z_L + 2Z_{TX})Z_{GR}}$$

This equation can be used to determine the transmit gain from $(V_L)_{ac}$ to V_{TX}, by setting $V_{RX} = 0$, which gives $(Z_{TX}) \div (\alpha Z_L + 2Z_{TX})$. Alternatively, by setting $(V_L)_{ac} = 0$ we obtain the 4-wire to 4 wire gain, V_{RX} to V_{TX}, giving the expression $-\alpha Z_L Z_{TX} \div [(\alpha Z_L + 2Z_{TX})Z_{GR}]$. If fuse resistors are included in the 2-wire loop, then Z_L is modified to become $(Z_L + 2R_F)$ in the above equations.

The transmission circuitry also contains a longitudinal feedback circuit, such that the MSLIC appears as typically 25Ω resistors from LA and LB to a bias voltage (see DC Line feed section). This bias voltage comes from the DC feed circuitry. The feedback circuit attenuates longitudinal signals from the transmit path, and has no effect on transverse signals.

DC LINE FEED (Active Mode)

DC line feed (loop) current $I_L = \frac{1}{2}(|I_A - I_B|)$ is provided by the device when it is in non-ringing modes. In ringing mode, DC line feed and AC ringing voltage are normally applied through the ring relay which is controlled by the device. The line feed current is reduced during standby operation.

In Active mode, Power feed is controlled by the resistance R_{DC} between the R_{DC} pin and the RSN pin (Fig.4). Again, the current in the 2 wire loop will be 1000 times the current into RSN. Operation of the DC feed circuitry is described with reference to Fig.4, which shows a conceptual model.

For the normal line feed region, a voltage V_{DC}, of magnitude $(50 - |V_{DCT}|) \div 20$ (where $V_{DCT} = |V_{LA} - V_{LB}|$) is produced at the R_{DC} pin (Pin 17), the sign of which determines normal or reverse polarity operation. If negative, normal polarity is established and if positive, reverse polarity will occur (polarity is set by control logic - see Table 2). This normal line feed region exists when $|V_{BAT}| - |V_{DCT}| \geq V_{SG}$ ($V_{SG} = 15V$ nominally, $V_{DCT} = |V_{LA} - V_{LB}|$), else the Saturation Guard circuit is active (described later).

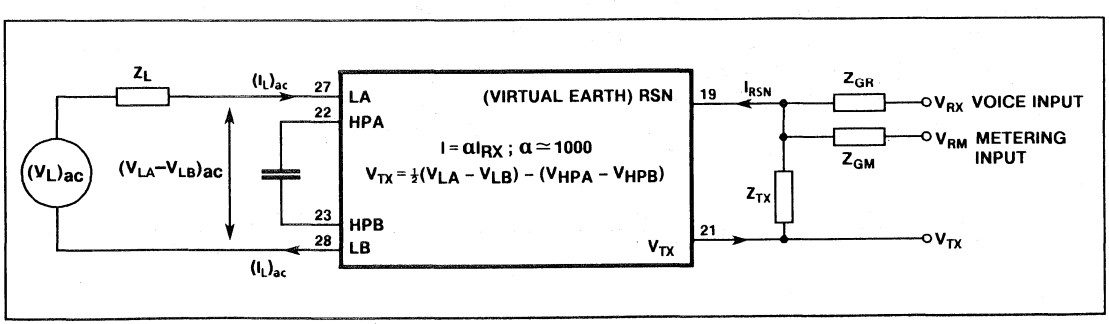


Fig.3 Voice circuit

Note that the internal resistors, R_{HP}, and external capacitor, C_{HP}, form a low pass filter network (this is discussed further in Application Note AN82, Applications General Considerations section). During the action of reversing polarity, the resistors R_{HP} are momentarily shorted to reduce the time taken for the DC voltage on C_{HP} to change sign.

The combination of the 1/20 Op Amp and the ×1000 virtual earth input current amplifier, means that the feed resistance is determined by ($R_{DC} \div 50$), i.e. $R_{FEED} = R_{DC} \div 50 = [(R_{DC1} + R_{DC2}) \div 50]$. If fuse resistors are included in the 2-wire loop, then the actual feed resistance will be:-

$$R_{FEEDTOT} = 2R_{FUSE} + R_{FEED} = 2R_{FUSE} + [(R_{DC}) \div 50]$$

As an example, to set $R_{FEEDTOT} = 840\Omega$, then if the resistors $R_{FUSE} = 20\Omega$, then $R_{DC1} = R_{DC2} = 20k\Omega$, since:-

$$(R_{DC1} + R_{DC2}) = [R_{FEEDTOT} - 2R_{FUSE}] \times 50$$
$$= [840 - 40] \times 50 = 40k\Omega$$

The values of R_{DC1} and R_{DC2} should be kept equal, forming a low pass filter network with C_{DC} to reduce chopper noise from the R_{DC} pin (see also discussion in AN82 Applications General Considerations section). The time constant of this network (C_{DC} and $R_{DC1} // R_{DC2}$) also affects the time taken for a polarity reversal, and it is normally ≈ 1.5ms.

The remaining circuitry models the action of the saturation guard circuit. This operates to reduce the voltage at the R_{DC} pin when:- $|V_{BAT}| - |V_{DCT}| < V_{SG}$. V_{SG} is a notional threshold voltage which is the headroom between the value of V_{DCT} and the battery voltage, at the point where Saturation Guard becomes active (this includes the diode drop in series with the V_{BAT} supply, D_2 Fig. 7). Thus, when the comparator determines the above condition, the magnitude of the difference is used to reduce the voltage at R_{DC}.

The total line feed characteristic is shown graphically in Fig. 6a and 6b.. The nearly constant voltage region (V_{DCT} constant) is due to the action of the saturation guard circuit. Fig. 6b plots the loop current value as a function of line resistance R_L. The example shown is that of an 800Ω feed resistance, the graphs being obtained by using the simple models of Figs. 5a and 5b (0Ω fuse resistors). Figs. 6a and 6b also show the action of V_{BAT} on the line characteristics.

With the saturation guard inactive, normal line feed conditions apply such that the feed and line/loop resistance determine I_L by the following relationship:

$$I_L = 50 \div (R_L + R_{FEEDTOT})$$

The line voltage is then simply determined by the relationship $V_L = I_L \times R_L$. This gives the example shown in Fig. 6a and 6b.

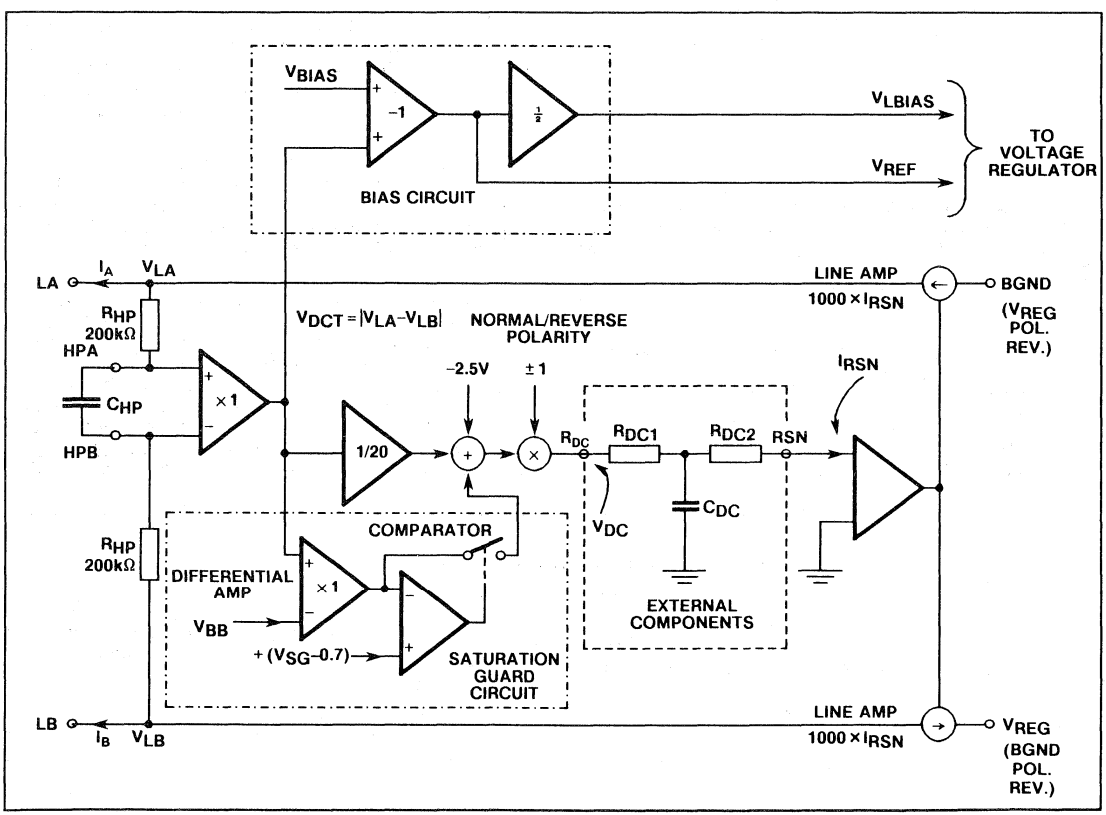


Fig.4 DC power feed circuit model.

When the saturation guard is active, then the line voltage is effectively held constant due to the reduction of the voltage at the R_{DC} pin. Thus, line conditions are set by the following:

$$I_L = [(|V_{BAT}|-V_{SG}) \div (R_L + 2R_{FUSE})]$$

To determine the line resistance (R_{LSG}) and current (I_{LSG}) at which the saturation guard becomes active, these parameters are obtained by equating the two expressions for Normal and Saturation Guard regions. Thus :-

$$I_{LSG} = 50\ (50 + V_{SG} - |V_{BAT}|) \div R_{DC}$$

$$R_{LSG} = \frac{(|V_{BAT}| - V_{SG})R_{DC}}{(50 + V_{SG} - |V_{BAT}|)50} - 2R_{FUSE}$$

The resultant line voltage (V_{LSG}) that occurs is obtained by the ohmic relationship of I_{LSG} & R_{LSG} (see Fig. 6a). This will become $V_{LSG} = (|V_{BAT}|-V_{SG})$ when $2R_{FUSE} = 0$. The open circuit line voltage $V_{LOC} \approx (|V_{BAT}|-V_{SG})$ at $R_L = \infty\Omega$ will always be greater than V_{LSG}, even when $2R_{FUSE} = 0\Omega$. This change in voltage between V_{LSG} and V_{LOC} will be greater at lower battery voltages. Fig. 6a shows the nominal effect.

DC LINE FEED (Standby Mode)

For Standby mode, the DC current is limited to a value just sufficient for the loop Detector to sense Off-Hook.

Normally this threshold (I_{DET}) is set externally by a resistor, R_{TH} (see Control and Signalling section). The limited loop current (I_{LIM}) is also determined by R_{TH} via a conversion factor K_{LIM} (nominally 1.7, see Electrical Characteristics) such that :

$$I_L \leq I_{LIM} = K_{LIM} \times I_{DET}$$

The slope impedance of this characteristic is almost a constant current, as shown in Fig. 6a. Since $K_{LIM} > 1$, the current level is still sufficient to detect the Off-Hook threshold (see Control and Signalling section).

LINE POLARITY

Normal polarity (in active or standby modes) consists of the LA pin DC voltage near BGND and the LB pin DC voltage near V_{BB}. Under these conditions, $I_L = +\frac{1}{2}(|I_A-I_B|)$ and the voltage at the RDC pin is negative. Reverse polarity will give the LA pin DC voltage near to V_{BB}, LB pin DC voltage near to BGND, $I_L = -\frac{1}{2}(|I_A-I_B|)$ and the RDC pin voltage is positive.

BIAS CIRCUIT

The Bias circuit (Fig. 4) produces two reference voltages, both referred to ground. These are V_{REF}, being related to the 2-wire transverse DC voltage and V_{LBIAS} approximately half V_{REF}.

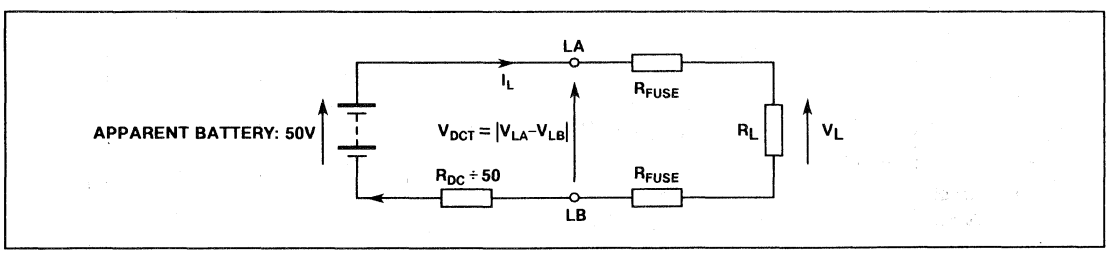


Fig. 5a Simple power feed model (normal line feed)

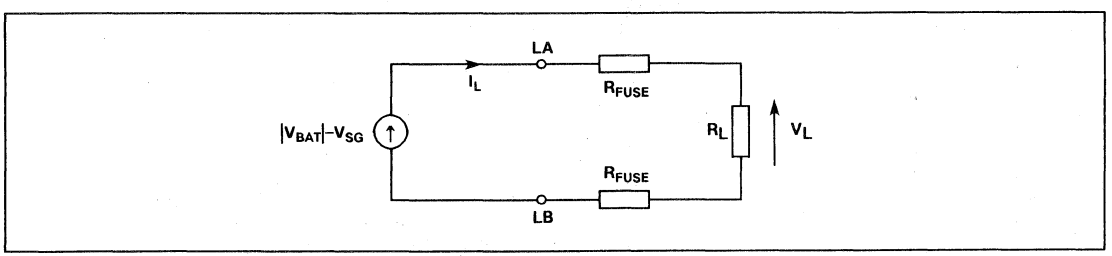


Fig. 5b Simple power feed model (saturation guard active)

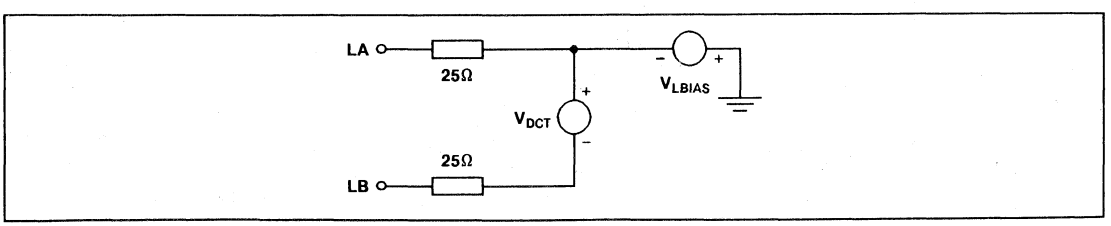


Fig. 5c Longitudinal bias circuit.

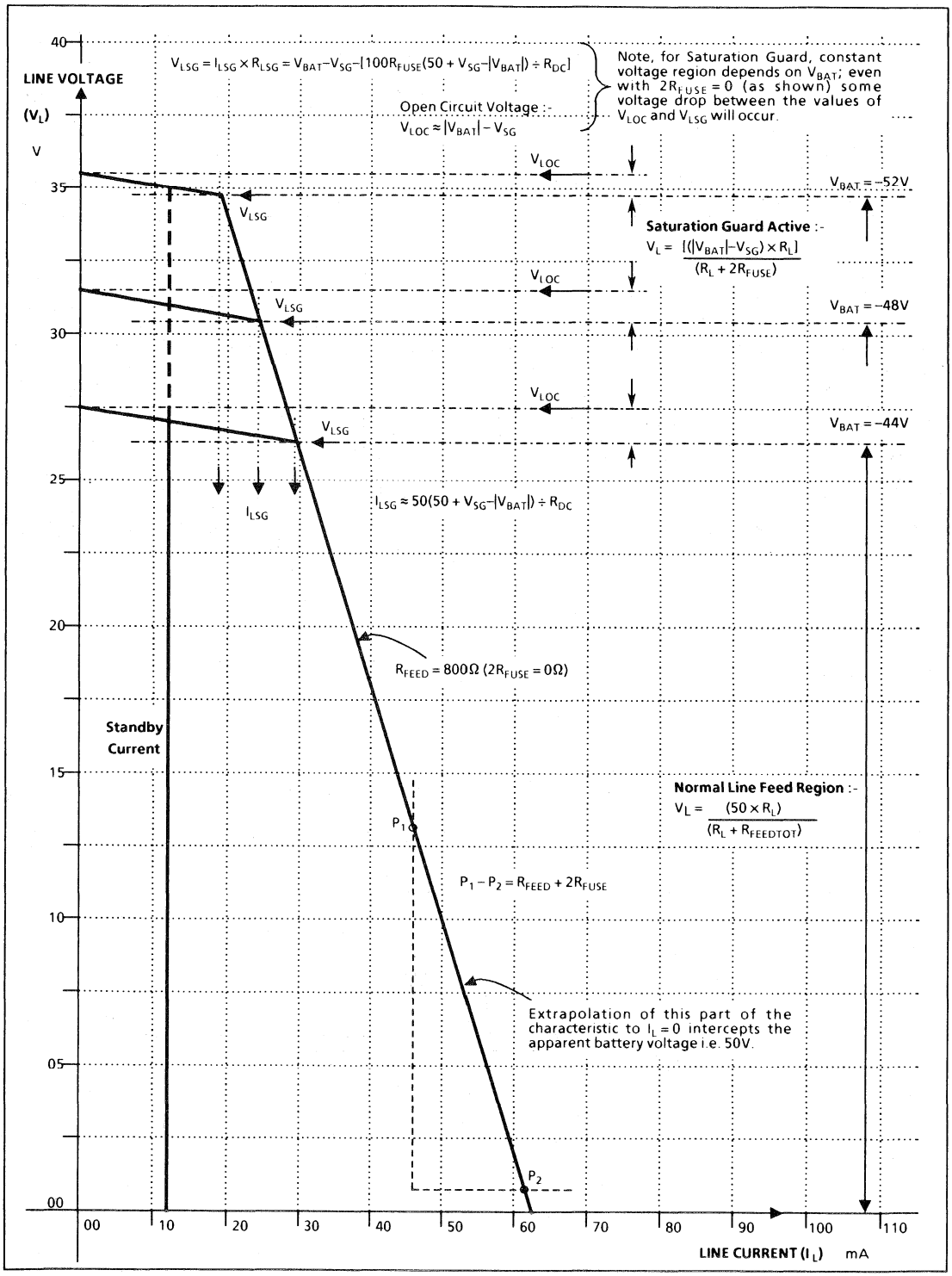


Fig. 6a : Line Feed Characteristic, V_L vs I_L.

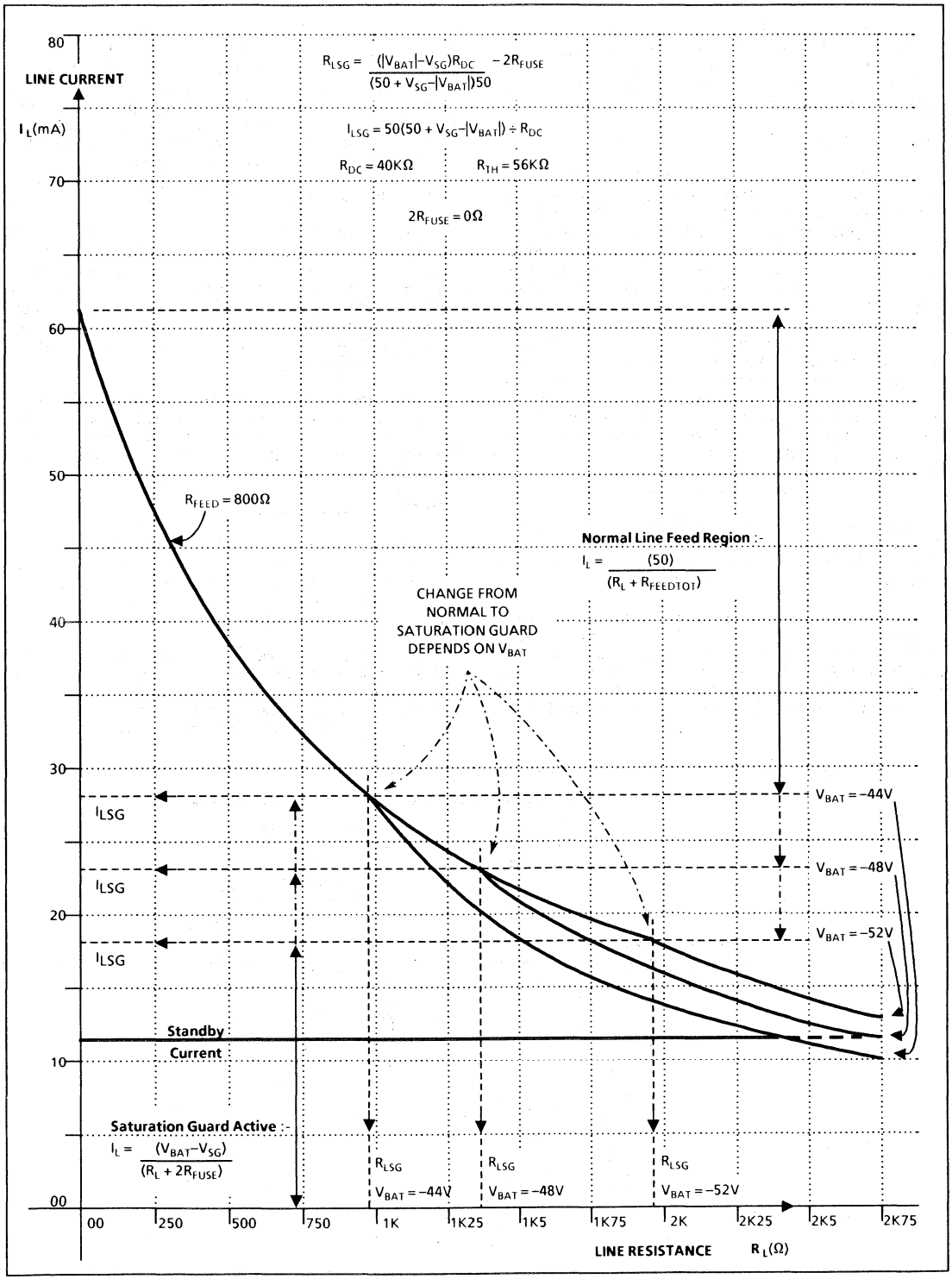


Fig. 6b : Line Feed Characteristic, I_L vs R_L.

V_{REF} controls the line feed regulator and V_{LBIAS} sets the 2-wire feed balance voltage (centre point voltage of the lines). The longitudinal control loop achieves an input impedance of approximately 25Ω per line for longitudinal signals, as shown in Fig. 5c.

LINE FEED REGULATOR

The DC voltage between LA and LB will vary with the DC loop resistance. Unless the voltage supplied to the chip can be varied to match that on the line there will be a voltage drop across the chip along the path taken by the feed current. This could cause significant power dissipation. The purpose of the line feed regulator is to minimise this power dissipation by regulating the voltage supplied to the line amplifiers.

Regulated voltage is supplied to the line amplifiers on V_{REG} and unregulated voltage is supplied on V_{BB}. The chip switches V_{BB} onto +CH when more power is required at the V_{REG} pin. V_{REG} is the voltage used by the device to power the 2-wire interface, and it is adjusted to follow a reference voltage V_{REF} (from Power Feed). This reference voltage is determined as follows:

$$V_{REF} = -\{ |V_{DCT}| + V_{BIAS} \}$$

and is such to set V_{REG} to the minimum required to power the line interface, thus minimising power dissipation. The voltage V_{BIAS} is needed to keep the amplifier response linear when audio signals are transmitted.

Fig. 7 shows the external components associated with the power supply aspect of the voltage regulator. +CH is the positive terminal of the regulator switch that connects to V_{BB}. When the switch is turned on, current in L_1 and C_1 increases, thus increasing stored energy. When the switch turns off, this stored energy sustains L_1 current which flows in D_1.

The voltage at +CH is thus a square wave of up to 50V p-p making this node sensitive to PCB layout. Note that the inductor should be capable of taking twice the line current without saturating. The regulator will work with a wide range of inductor resistance, although if this is too large, long line drive capability and regulator efficiency will be reduced. Since there are large current fluctuations from V_{BB} through the switch, C_2 provides filtering of the VBB pin, whilst D_2 isolates the V_{BAT} supply should the LA/LB pins be taken negative of the V_{BAT} supply.

The chip senses the voltage at V_{REG}, compares it to its requirements and switches power from V_{BB} to +CH, using the variable mark/space method, to give appropriate matching. The rate of switching can be governed by CHCLK (pin 10) or allowed to free run, its stability ensured by the network on CHS (pin 9), i.e. C_3, R_1, C_5. Since noise is produced by the switching, a decoupling node is provided at SUB (pin 8).

Note that the regulator is powered down in standby mode to further reduce power dissipation. It is intended that the SLIC will be put into active mode once Off-Hook has been detected, since in this state excessive power dissipation may result. This is discussed further in AN82.

CONTROL AND SIGNALLING

The mode of operation of the SL376 is determined by the digital interface pins, as described in Tables 1 and 2. These pins enable ringing or non-ringing modes of operation, controlling line status, line polarity, relay driver and selection of line detector.

The line status is selected by use of the D2..D0 pins, Table 2, to determine the modes as listed. The function of these modes has already been described in the 'Overview' and 'DC Line Feed' sections; more detail of the device detectors is given on the following page (refer to Fig. 8).

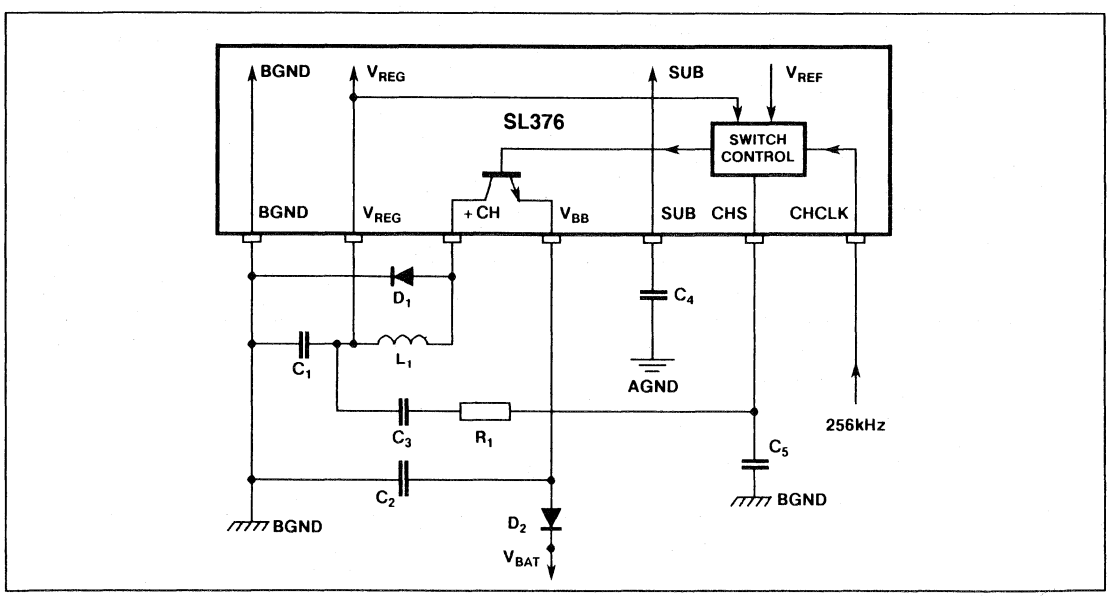


Fig.7 Voltage regulator power supply circuit.

Loop Detect

This detector is used in Active and Standby modes (with/without polarity reversal). The loop current at which the detector indicates the Off-Hook condition, is set by the comparator at pins 24 (RD) and 20 (V_{EE}). Normally a resistor, R_{TH}, is connected between these pins, such that Off-Hook line current threshold (I_{DET}) is set by:

$$I_{DET} = 350 \div R_{TH}$$

This is due to the fact that the current out of the RD pin is equal to the loop current $I_L = (\frac{1}{2}|I_A - I_B|)$ divided by ~280. This will create a voltage across R_{TH} at the RD pin. Off-Hook is given by a logic low at the $\overline{DET}$ output pin (when detector is selected) when this voltage rises above the internal 1.25V reference.

Ground Key Detector

This detector is selected by the E1 pin of the Digital Interface. It can be used in Active and Standby modes (with/without polarity reversal), as well as Disconnect A Standby B mode.

Operation of the detector is via an internal threshold and the longitudinal current $I_{LL} = I_A + I_B$ of the 2-wire loop. Ground Key detection is indicated when either the midpoint of the A and B legs is connected to ground, or the B leg (A leg, polarity reversed) is connected to ground. The resistance values for which Ground Key detection is valid are given in the Electrical Characteristics section.

Ring Trip Detector

This consists of a comparator connected to the DA and DB pins, and indicates Ring Trip when the voltage at DA < DB. Selection of Ringing mode operates the Ring Relay and enables the Ring Trip Detector. The external ringing supply must consist of DC line feed in addition to the AC ringing voltage. In order that the Ring Trip Detector senses Ring Trip in ringing mode, a resistance bridge network is used in association with pins DA, DB, line and ring source. This network is described in the Applications section and discussed further in AN82.

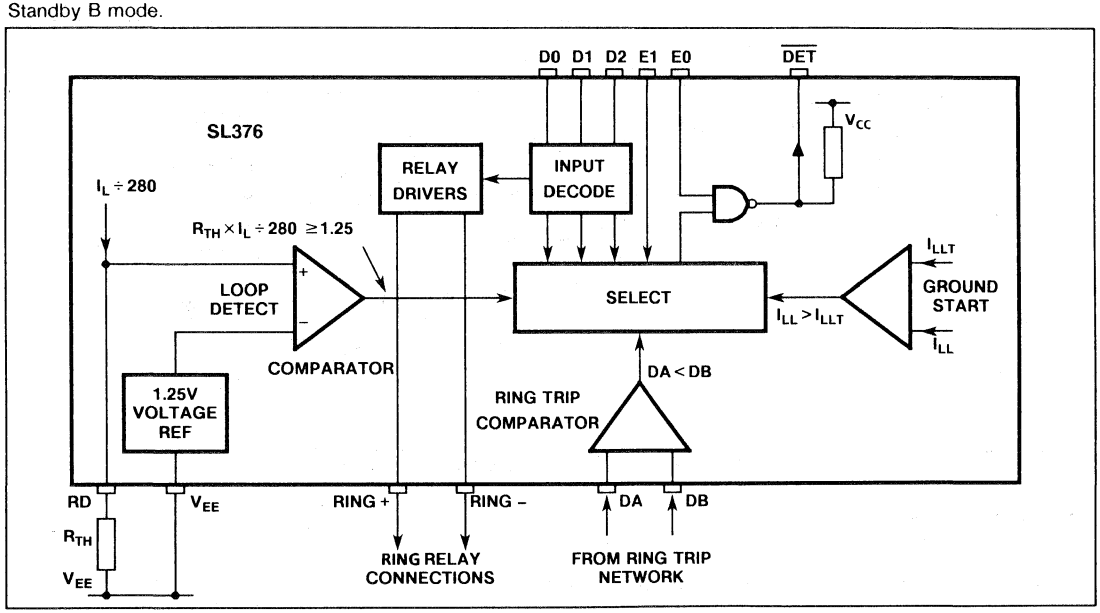


Fig.8 Detector circuits.

FUNCTIONAL PARAMETER SUMMARY

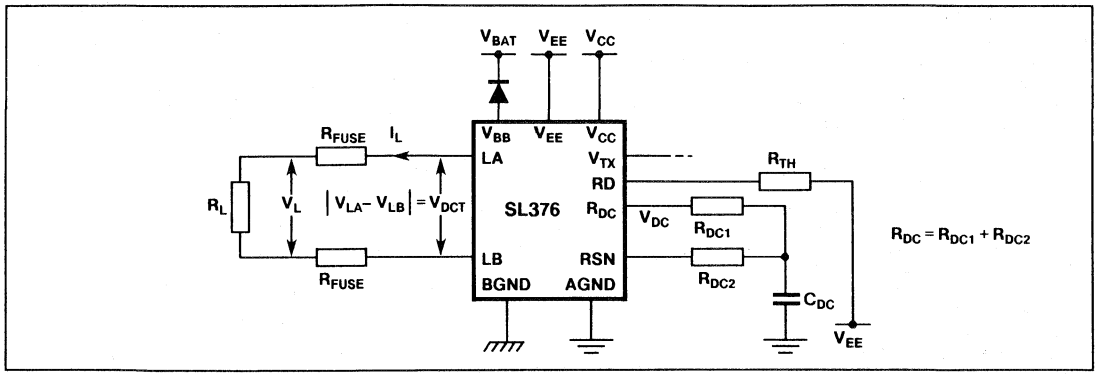


Fig.9 DC parameters and components for the SL376

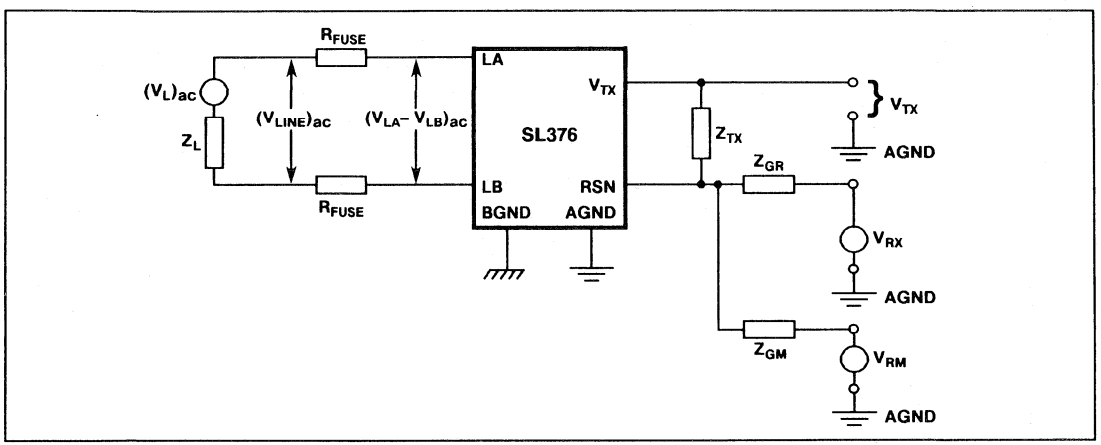


Fig.10 AC parameters and components for the SL376

LIST OF DEFINITIONS

1. Loop Current is defined as :- $I_L = \pm \frac{1}{2}|I_A - I_B|$

   I_A = current out of LA pin, I_B = current out of LB pin, + ⇒ normal line polarity and –⇒ reverse line polarity.

2. Longitudinal Current is defined as :- $ILL = (I_A + I_B)$

   I_A = current out of LA pin, I_B = current out of LB pin.

3. Normal Line Feed Region when $|V_{BAT}|-|V_{DCT}| > V_{SG}$ which gives :-

   $$I_L = I_{FEED} = 50 \div (R_L + R_{FEEDTOT}) \quad \text{where} \quad R_{FEEDTOT} = 2R_{FUSE} + (R_{DC} \div 50)$$

4. Saturation Guard Threshold when $|V_{BAT}|-|V_{DCT}| = V_{SG} = 16.5V$ such that :-

   $$I_L = I_{LSG} = 50(50 + V_{SG}-|V_{BAT}|) \div (R_{DC}) \text{ and}$$

   $$R_{LSG} = \frac{[(|V_{BAT}|-V_{SG}) \times (R_{DC})] - [2R_{FUSE}]}{(50 + V_{SG}-|V_{BAT}|)50} \quad V_{LSG} = I_{LSG} \times R_{LSG}$$ which will equal $|V_{BAT}|-V_{SG}$ with $2R_{FUSE} = 0$

LIST OF DEFINITIONS (continued)

5. Saturation Guard feed Region when $|V_{BAT}|-|V_{DCT}| < V_{SG}$ with $I_L = [|V_{BAT}|-V_{SG}] \div [R_L + 2R_{FUSE}]$

6. Note that V_{LSG} is referred to as the value of the line voltage, V_L, at the point where Saturation Guard becomes active. This will differ from the value of $|V_{LA}-V_{LB}|$ (i.e. V_{DCT}) if $2R_{FUSE} \neq 0$. V_{SG} is used as a notional threshold voltage which is the headroom between the $|V_{LA}-V_{LB}|$ voltage and the battery supply, at this same point (including the diode drop of D_2 Fig. 7).

7. Open Circuit Line Voltage V_{LOC} at $R_L = \infty\Omega$ such that :- $V_L = V_{LOC} \approx [|V_{BAT}|-V_{SG}]$

   V_{LOC} will be $\geq V_{LSG}$ even with $2R_{FUSE} = 0$. The voltage drop from V_{LOC} to the defined V_{LSG} point will be greater at lower values of V_{BAT}.

8. Standby Mode DC Feed Current $I_L \leq I_{LIM} = K_{LIM} \times I_{DET} \approx 600 \div R_{TH}$

9. 2-Wire Termination Impedance $Z_{AB} = (Z_{TX} \div \frac{1}{2}\alpha) = (Z_{TX} \div 500)$

   Note that Z_{TX} is normally set to $[\frac{1}{2}\alpha(Z_L + 2R_{FUSE})]$ where Z_L is the desired termination impedance.

10. Recieve Gain from V_{RX} to $(V_{LA}-V_{LB})_{ac}$ or $(V_{LINE})_{ac}$ is set by Z_{GR} after setting Z_{TX}. Thus, with $(V_L)_{ac} = 0$:-

$$\frac{(V_{LA}-V_{LB})_{ac}}{V_{RX}} = \frac{-2\alpha Z_L Z_{TX}}{[\alpha(Z_L) + 2Z_{TX}]Z_{GR}} \quad \text{with } 2R_{FUSE} = 0 \; ; \quad \frac{(V_{LINE})_{ac}}{V_{RX}} = \frac{-2\alpha Z_L Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + 2Z_{TX}]Z_{GR}} \quad \text{with } 2R_{FUSE} \neq 0$$

11. Resultant Transmit Gain is then :-

$$\frac{V_{TX}}{(V_L)_{ac}} = \frac{Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + 2Z_{TX}]} \quad \text{with } V_{RX} = 0$$

12. Resultant 4 Wire-4 Wire Gain is then :-

$$\frac{V_{TX}}{V_{RX}} = \frac{-\alpha(Z_L + 2R_{FUSE})Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + 2Z_{TX}]Z_{GR}} \quad \text{with } (V_L)_{ac} = 0$$

13. Metering Gain is determined by Z_{GM} in association with Z_{TX}, thus for the receive direction :-

$$\frac{(V_{LA}-V_{LB})_{ac}}{V_{RM}} = \frac{-2\alpha Z_L Z_{TX}(0.66)}{[\alpha(Z_L) + 2Z_{TX}]Z_{GM}} \quad \text{with } 2R_{FUSE} = 0 \; ; \quad \frac{(V_{LINE})_{ac}}{V_{RM}} = \frac{-2\alpha Z_L Z_{TX}(0.66)}{[\alpha(Z_L + 2R_{FUSE}) + 2Z_{TX}]Z_{GM}} \quad \text{with } 2R_{FUSE} \neq 0$$

and for the 4 wire to 4 wire path :-

$$\frac{V_{TX}}{V_{RM}} = \frac{-\alpha(Z_L + 2R_{FUSE})Z_{TX}(0.66)}{[\alpha(Z_L + 2R_{FUSE}) + 2Z_{TX}]Z_{GM}} \quad \text{with } (V_L)_{ac} = 0$$

Note that the factor of 0.66 is due to the device intrinsic gain at metering frequencies (12kHz-16kHz) and it will vary from this figure depending on PCB layout.

14. Off-Hook Threshold is set by R_{TH} at :- $I_L = I_{DET} = 350 \div R_{TH}$

15. Ring Trip Threshold is set by the bridge associated with pins 25 .. 28 and the 2-Wire Line, thus :-

    $R_L = R_{LTH} = R_{B4}(2R_F) \div (R_{B4}-R_{B1})$ assuming $R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$ and $R_{FEED1} = R_{FEED2}$ for the bridge components (balanced ringing). $R_{B1}..R_{B4} \approx$ a few 100KΩ and $R_{FEED1} \approx$ a few 100Ω.

16. AC ringing voltage at DA (DB by the same amount) is reduced by a factor of :- $[1 + (2\pi f_r t_r)^2]^{-\frac{1}{2}}$

    f_r is the ringing frequency and t_r is determined by the bridge components including C_B, thus :- $t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$

    for Balanced Ringing.

APPLICATIONS

The requirements for the subscriber line interface vary considerably from one telephone administration to another. The SL376 is designed to have the flexibility to meet these varying requirements. For simplicity, only a single example is given to illustrate how the device is connected. Fig. 11 shows the circuit which can be used to evaluate the device. Further Applications information is given in AN82 SL373/SL376 Applications Note.

The DA and DB pins are connected to a resistance bridge network (R_{B1} to R_{B4}). This allows the change in line resistance to be sensed when the remote telephone goes off-hook during ringing (Ring Trip). The details of this network (and C_B) are given later (see Ring Trip section). The resistors R_{FEED1} and R_{FEED2} provide feeding of the ringing source onto the line during ringing mode. The Ring Relay Driver is shown connected through a current limiting resistor.

Connections to the LA and LB pins are shown, and include the resistors R_{FUSE} in addition to the ring relay. These resistors have a value around 20 to 30 ohms, depending on the application, and provide current line protection.

Overvoltage and protection circuitry may consist of slew-limiting inductors between the pins and the line itself and a thyristor or zener protection network at the line. In many applications, especially in PBXs, the amount of protection circuitry can be reduced. The capacitors between LA, LB and ground, allow noise from the regulator to be decoupled.

The capacitor C_{HP} between HPA and HPB (pins 22 and 23) is used to filter out the AC component of the signal on the line. The voltage difference between the two pins should be effectively DC. Application Note AN82 contains a further discussion on this component.

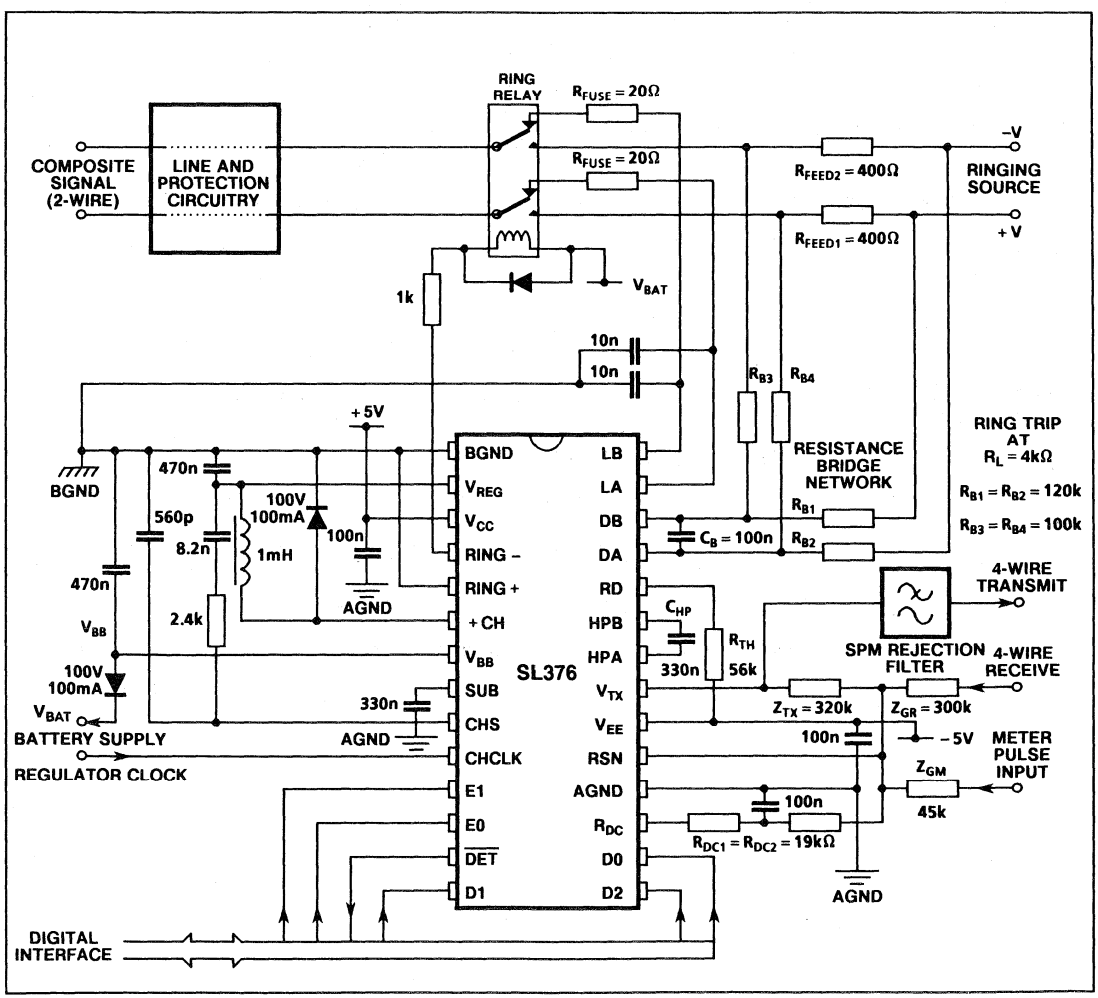


Fig. 11 Application circuit

The resistor, R_{TH}, between RD (pin 24) and V_{EE} (pin 20) programs the threshold current for the loop detector. A capacitor in parallel can be added to reduce the effect of the AC component of the line current, but this can cause instability in standby operation with highly inductive lines if it is too large.

The value of R_{TH} sets the current I_{DET} according to the relationship :

$$I_{DET} = 350 \div R_{TH}$$

The CHS pin (pin 9) is connected to BGND through a capacitor and to V_{REG} by a capacitor and resistor in series. This stabilises the regulator control loop. Operation of the regulator has been described earlier in the Functional Description section (pins 2,6 & 7).

It is recommended that the substrate (SUB) pin be decoupled to AGND. However, BGND may be used if this is sufficiently quiet, otherwise some degradation in noise performance may be experienced.

DC current flows between the R_{DC} (pin 17) and RSN (pin 19). This is used to set the line feed current. Any minor AC fluctuations are reduced by dividing the resistance R_{DC} equally such that $R_{DC1} = R_{DC2} = \frac{1}{2}R_{DC}$ and connecting a capacitor from the junction of R_{DC1} and R_{DC2} to AGND.

The network (Z_{TX}) between V_{TX} and RSN controls the 2 wire terminating impedance (Z_T). This can also be a complex impedance. The value of Z_{TX} can be calculated from the relationship :-

$$Z_{TX} = (\text{Required } Z_T) \times (\text{Receive Current Gain}) \times \tfrac{1}{2}$$

The Receive Gain is set by the network (Z_{GR}) which controls the receive current flowing into RSN. This can be a complex impedance network to allow for complex impedance terminations. Note that Meter Pulse Injection is achieved in the same way as for receive gain, but set by the network value Z_{GM} and taking into account an additional factor of 0.66. More details of these gain settings are given in AN82.

Control and status pins are TTL compatible. They are designed to give a simple interface to digital circuits and are directly compatible with the MV3010 PSLAC.

RING TRIP

Ring Trip detection operates by comparing the voltages on DA and DB and providing the output on $\overline{DET}$ when this function is enabled by the status input pins of the Digital Interface. A resistance bridge (R_{B1} to R_{B4}) must be connected to the line and the ringing voltage source to cause the differential voltage between DA and DB to change sign when the line resistance falls below the level associated with Ring Trip. Note that it is simplified by use of $R_{B1} = R_{B2}$ and $R_{B3} = R_{B4}$ (see discussion in AN82)

Ringing voltage is normally applied to the line through the Ring Relay which is activated by RING + and RING – (see Ring Relay Driver). The ringing voltage sources, including line feed, are connected to the line via ringing feed resistors, R_{FEED1} and R_{FEED2}. The resistance bridge operates by allowing the DC voltage dropped across the ringing feed resistors in the Off-Hook condition to reverse the polarity of the voltage on DA and DB (DA < DB). Since the AC ringing voltage is greater than the DC feed, the capacitor C_B (Fig. 12) will filter this out at the comparator inputs. The connection shown is suitable for balanced ringing only. For unbalanced ringing, separate capacitors from DA (C_{B1}) and DB (C_{B2}) to ground will be required to achieve the same result.

Fig. 12 shows how the resistance bridge is connected when used with balanced ringing. The circuit can operate correctly provided there is a DC feed in addition to the AC ringing voltage.

If R_{LTH} is the line resistance corresponding to the Ring Trip threshold (DA = DB), this can be determined from the values of R_F ($R_{FEED1} = R_{FEED2} = R_F$), R_{B1} and R_{B4} ($R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$) as:-

$$R_{LTH} = \frac{R_{B4}(2R_F)}{(R_{B1} - R_{B4})}$$

R_{B1} and R_{B4} should be a few hundred kΩ.

The amplitude of the AC ringing voltage at DA (DB by the same amount) is reduced by a factor of $[1 + (2\pi f_r t_r)^2]^{-\frac{1}{2}}$ where f_r is the ringing AC frequency and t_r is set by:-

$$t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$$

for balanced ringing. For $f_r \approx 20$Hz, t_r should be ≈ 50ms. For unbalanced ringing C_B will become $C_{B1}C_{B2} \div (C_{B1} + C_{B2})$ in the above equation. More detail on Balanced and Unbalanced ringing is given in AN82.

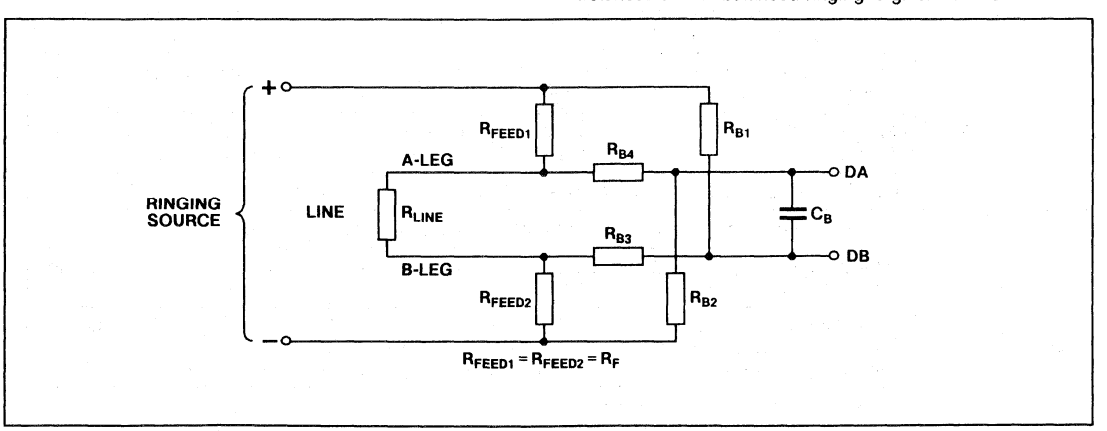


Fig. 12 Ring trip circuit (balanced ringing).

RING RELAY DRIVER

It is possible to drive the Ring Relay from the SL376 in one of two ways, as shown in Figs. 13a and 13b. Note that RING– is clamped from going below the substrate, and that V+ may be +30V (max.) if V_{BAT} = –50V (Absolute Maximum Voltage, RING + to V_{BAT} = 80V).

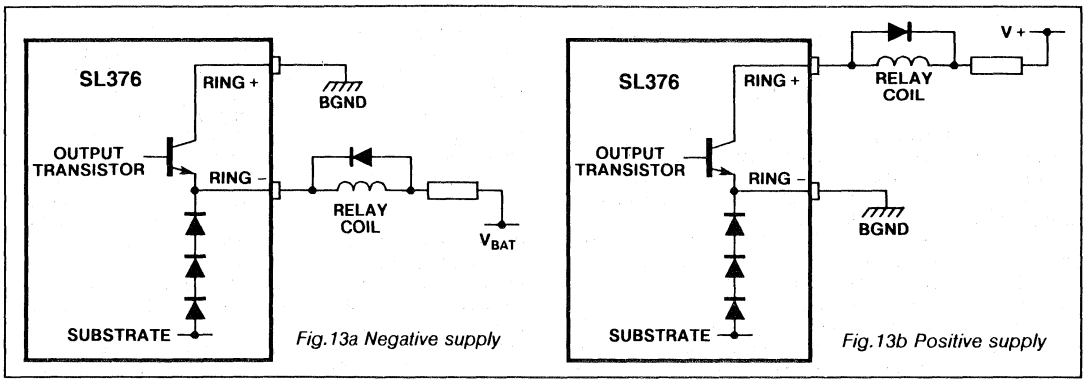


Fig.13a Negative supply *Fig.13b Positive supply*

Fig.13 Alternative relay drive configurations.

PIN DESCRIPTIONS

Symbol	Pin no.	Pin name and description
BGND	1	**Battery Ground (Power Input).** 0 Volts.
V_{REG}	2	**Regulated Voltage (Negative Power Input).** The voltage at this pin is compared to that required for line feed, and the result is used to control the voltage regulator.
V_{CC}	3	**Positive Supply (Power Input).** +5 Volts.
RING –	4	**Ring Relay Driver Output, Transistor Emitter.** This output is designed to drive a ring relay, when used together with RING +
RING +	5	**Ring Relay Driver Output, Transistor Collector.** This output is designed to drive a ring relay, when used together with RING –
+CH	6	**Switching Regulator (Chopper) Output (Negative Power Output).** Chopper switch transistor collector. An internal regulator controls the mark/space ratio of the switching waveform to maintain V_{REG} (pin 2) at the required voltage.
V_{BB}	7	**Battery Voltage (Negative Power Input).** This is the battery supply pin which connects to the V_{BAT} supply via an external diode, to the chopper switch emitter and via an on-chip resistor to SUB.
SUB	8	**Substrate (Decoupling Node).** An external decoupling capacitor (0.33μF) should be connected between this pin and AGND.
CHS	9	**Line Feed Regulator (Chopper) Stabilising Network.** This is the input to the voltage comparator which is used to control the switching regulator.
CHCLK	10	**Line Feed Regulator (Chopper) Clock (Digital Input).** This is the positive edge triggered, 256KHz clock input for the voltage regulator, which will free run in the absence of an input signal.
E1	11	**Detector Select (Digital Input).** Selects the line status detector (Loop or Ground Key).
E0	12	**Detector Data output Enable (Digital Input).** Enables the Detector data output ($\overline{DET}$).
$\overline{DET}$	13	**Detector Data output (Digital Output).** This pin outputs the status of the detector which has been selected by D0 - D2 and E1. It is enabled by the E0 pin.
D1 D2 D0	14 15 16	**Control Input (Digital Input).** **Control Input (Digital Input).** **Control Input (Digital Input).** These inputs determine the MSLIC operating mode, and control the ring relay, selection of ringing and non-ringing modes, line polarity, line status and line detector.
R_{DC}	17	**DC Reference Voltage (Voltage Output).** A reference voltage of $\pm(50-\lvert V_{LA}-V_{LB}\rvert)\div 20$ Volts (depending on line polarity), is output at this pin, excepting Saturation Guard operation.

PIN DESCRIPTIONS (continued)

Symbol	Pin no.	Pin name and description
AGND	18	**Analog Ground (Analog Reference Node).** This is the ground reference pin for the analog signals. It also provides a ground reference for the Digital Interface. Signal reference and decoupling connections should be separately run to this pin.
RSN	19	**Receive Summing Node (Current Input).** The current which is input on this pin is used to control the transverse current at LA and LB.
V_{EE}	20	**Negative Supply (Power Input).** – 5 Volts.
V_{TX}	21	**Transmit Voltage (Voltage Output).** The voltage output at this pin is equal to the difference between the voltage (V_{LA}–V_{LB}) and the differential DC voltage (V_{HPA}–V_{HPB}), multiplied by the 2 to 4 wire voltage gain.
HPA, HPB	22 23	**High Pass A, High Pass B - AC/DC separation (Voltage Inputs).** These inputs sense the DC feed voltages on the LA and LB pins respectively. Under normal operation they are connected to LA and LB respectively by internal resistors and should be connected as shown in Fig. 11.
RD	24	**Loop Detection Control (Current Output / Voltage Input).** This pin outputs a current which equals the transverse loop current through LA and LB divided by 280. Off-Hook is indicated via the $\overline{DET}$ pin when the voltage at this pin is $\geq (V_{EE} + 1.25)$ Volts.
DA DB	25 26	**Ring Trip Detector A, Ring Trip Detector B (Voltage Inputs).** These are the A and B inputs to the internal ring trip comparator. The output of the comparator controls the ring trip output on $\overline{DET}$.
LA LB	27 28	**A Line Transceiver, B Line Transceiver (Current Outputs / Voltage Inputs).** These two pins form the 2 wire port connecting to the subscriber loop.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Range - see page 3-71)

Test conditions (unless otherwise stated)

V_{CC} = +5.0V, V_{EE} = –5.0V, V_{BAT} = –50V (see note 2), $V_{AGND} = V_{BGND}$, T_{AMB} = +25°C, V_{IL} = 0.7V and V_{IH} = 2.0V. Test circuit Fig. 27. Voltages are measured with respect to analog ground (V_{AGND}). Typical figures are for design aid only; they are not guaranteed and are not subject to production testing.

Supply Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply (V_{CC}) current, disconnect mode	I_{CC1}			4	mA	
Positive supply (V_{CC}) current, standby mode	I_{CC2}			10	mA	On / Off-Hook, $I_L = 0$
Positive supply (V_{CC}) current, active mode	I_{CC3}			10	mA	On / Off-Hook, $I_L = 0$
Negative supply (V_{EE}) current, disconnect mode	I_{EE1}			2	mA	
Negative supply (V_{EE}) current standby mode	I_{EE2}			3	mA	On / Off-Hook, $I_L = 0$
Negative supply (V_{EE}) current active mode	I_{EE3}			3	mA	On / Off-Hook, $I_L = 0$
Battery supply (V_{BB}) current disconnect mode	I_{BB1}			1.0	mA	
Battery supply (V_{BB}) current standby mode	I_{BB2}			5	mA	On-Hook, $I_L = 0$
Battery supply (V_{BB}) current active mode	I_{BB3}			6	mA	On-Hook, $I_L = 0$
Positive supply (V_{CC}) rejection ratio (supply to 2-wire transverse)	P_{SRT}	20			dB	50mV on V_{CC} supply 300-3400Hz, $R_L = 600\Omega$
Positive supply (V_{CC}) rejection ratio (supply to 2-wire longitudinal)	P_{SRL}	17			dB	50mV on V_{CC} supply 300-3400Hz, $R_L = 600\Omega$
Negative supply (V_{EE}) rejection ratio (supply to 2-wire transverse)	N_{SRT}	20			dB	50mV on V_{EE} supply 300-3400Hz, $R_L = 600\Omega$
Negative supply (V_{EE}) rejection ratio (supply to 2-wire longitudinal)	N_{SRL}	20			dB	50mV on V_{EE} supply 300-3400Hz, $R_L = 600\Omega$
Battery supply (V_{BB}) rejection ratio (supply to 2-wire transverse)	B_{SRT}	20			dB	50mV on V_{BAT} supply 300-3400Hz, $R_L = 600\Omega$
Battery supply (V_{BB}) rejection ratio (supply to 2-wire longitudinal)	B_{SRL}	25			dB	50mV on V_{BAT} supply 300-3400Hz, $R_L = 600\Omega$
Power dissipation, active state	P_{WA1}			1.1	W	$Z_L = 600\Omega$
Power dissipation, active state	P_{WA2}		1.5		W	$Z_L = 0\text{-}\infty\Omega$
Power dissipation, standby state, on-hook	P_{WD1}			0.3	W	
Power dissipation, standby state, off-hook	P_{WD2}				W	See note 1

NOTES

1. Because the regulator is inhibited, only short term operation is envisaged in standby mode, off-hook.
2. Battery voltage V_{BAT} is generally defined. The corresponding V_{BB} voltage is assumed to be 0.7V more positive than V_{BAT} allowing for the diode drop in D_2, Fig. 7.

Analog Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
2-wire port, low freq overload level	V_{OAB}	– 6.0		+ 6.0	Volts (pk)	See Fig 14, note 3: E_R = 1000 Hz, E_L = 0V
2-wire port, longitudinal impedance, off hook	Z_{LL1}			35	Ω/wire	See Fig 15: f < 100 Hz Z_L = 600Ω
2-wire port, longitudinal impedance, on hook	Z_{LL2}			35	Ω/wire	See Fig 16: f < 100 Hz Z_L = 600Ω
Longitudinal current limit, active state	ILL_A	17.5			mA/wire (rms)	See Fig 17, note 4: E_R = – 10dBm 700-1100Hz
Longitudinal current limit, standby state	ILL_S	8.0			mA/wire (rms)	See Fig 17, note 4: E_R = – 10dBm 700-1100Hz
4-wire transmit port, overload level	V_{OT}	– 3.1		+ 3.1	V (pk)	See Fig 14, note 3: f = 1000 Hz 4 Wire Load ≥ 25kΩ, E_R = 0V
4-wire transmit port, offset voltage	V_{TOFF}	– 15		+ 15	mV	See Fig 14: E_R = 0
4-wire transmit port,output impedance	Z_T			10	Ω	See Fig 14: E_R = 0
Transmit (2 to 4-wire) voltage gain	G_T	– 6.03		– 5.73	dB	See Fig 14: E_R = 0, E_L = 0dBu (note 5) 1kHz
4-wire receive port, low impedance virtual earth input	Z_{RI}			20	Ω	See note 6
4-wire receive port, low freq voltage gain	G_{RL4}	– 0.15		+ 0.15	dB	See Fig 18: E_R = 2.6dBu 1kHz
4-wire receive port, high freq voltage gain (open loop)	G_{RH4}	G_{RH} – 0.6		G_{RH} + 0.6	dB	See Fig 18, note 7: E_R = 2.6dBu 15000Hz
4-wire receive port, current gain	G_{RI4}	59.8	60.0	60.2	dB	See Fig 14
4 to 4-wire voltage gain	$G_R \times G_T$	– 6.08		– 5.68	dB	
2-wire to 4-wire frequency response	F_{24}	– 0.1		+ 0.1	dB	See Fig 14, note 8: E_R = 0, E_L = 0dBu 200-3400 Hz
4-wire to 2-wire frequency response	F_{42}	– 0.1		+ 0.1	dB	See Fig 14, note 8: E_L = 0, E_R = 0dBu 200-3400 Hz
4-to 4-wire frequency response	$F_{44} = F_{24} \times F_{42}$	– 0.1		+ 0.1	dB	See note 8
Gain linearity, 2-wire to 4-wire	G_{L24}	– 0.05		+ 0.05	dB	See Fig 14, note 9: E_R = 0, E_L = + 7dBu to – 59dBu 1kHz
Gain linearity, 4-wire to 2-wire	G_{L42}	– 0.05		+ 0.05	dB	See Fig 14, note 9: E_L = 0, E_R = + 3dBu to – 64dBu 1kHz
4-wire idle channel noise (psophometric weighted)	N_{P4}			– 80.0	dBup	See Fig. 14: V_{BAT} = – 48V, $E_L = V_R$ = 0V
2-wire idle channel noise (psophometric weighted)	N_{P2}			– 75.0	dBup	See Fig. 14: V_{BAT} = – 48V, $E_L = V_R$ = 0V

NOTES
3. Overload occurs when distortion is 2% of total signal in the range 300-3400Hz.
4. E_{LL} = 50Hz. Amplitude is increased until signal-to-Distortion Ratio at V_T ≤ 20dB.
5. dBu is defined thus: 0dBu is equivalent to the voltage at 0dBm when loaded with 600Ω (0.775V_{RMS}).
6. Not tested in production. Figures are guaranteed by characterisation.
7. Very dependent on board layout. $G_{RH} \approx -3.6$dB
8. Response is measured with respect to 1kHz
9. Linearity is measured with respect to gain at 0dBu.

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
2-wire differential noise (wide band)	N_{D2}		Fig. 20			See Fig 19, note 6
2-wire longitudinal noise (wide band)	N_{L2}		Fig. 21			See Fig 19, note 6
Regulator noise 4-wire transmit single frequency	N_{R4}		– 55.0		dBu	See Fig 19, note 6
Regulator noise 2-wire transverse single frequency	N_{RT}		– 50.0		dBu	See Fig 19, note 6
Regulator noise 2-wire longitudinal single frequency	N_{RL}		– 50.0		dBu	See Fig 19, note 6
Longitudinal balance, longitudinal-transverse	B_{L-T}	50			dB	See Fig 15: $Z_L = 600\Omega$, $E_R = 0$, E_{LL} = + 2dBu 40-4000 Hz
Longitudinal balance, trans-long + long-trans	B_{T-L} + B_{L-T}	98			dB	See Fig 15 & Fig 22: $Z_L = 600\Omega$, $E_R = 0$, E_{LL} = + 2dBu 300-800Hz
Longitudinal signal rejection, long to 4-wire	RJ_{L-4}	50	60		dB	See Fig 15: $Z_L = 600\Omega$, $E_R = 0$, E_{LL} = + 2dBu 40-4000 Hz
Longitudinal signal generation, 4-wire to long	GN_{4-L}	40			dB	See Fig 23: E_R = 2.6dBu f = 300-800Hz, $Z_L = 600\Omega$ or 1.6kΩ
Harmonic distortion, 4 to 2-wire	T_{HD1}			– 50.0	dB	See Fig 14, Note 10: E_R = 0dBu 1kHz
High frequency harmonic distortion, 4 to 2-wire,on-hook	T_{HD2}			– 35.0	dB	See Fig 24, Note 11: V_{A-B} = 2.2V rms, 16kHz
Intermodulation distortion	ID_{A-B1}			– 40.0	dB	See Fig 14, Note 12: $E_R = f_1 + f_2$, $f_1 = f_2$ = – 4 to – 21dBu
50Hz intermodulation distortion	ID_{A-B2}			– 49.0	dB	Note 6
Loop current, active state	I_{ACT1}	32.7		38.7	mA	See Fig. 27 : $Z_L = 600\Omega$ note 13
Loop current, active state	I_{ACT2}	16.5		21	mA	See Fig. 27 : $Z_L = 1.8k\Omega$ note 13
2-wire current, disconnected state	I_{DCT}			1.0	mA	LA to LB or Ground, or both LA and LB to Ground
Loop current, standby state, normal(+) or reverse(–)	I_{LIM}	10.0		12.8	(±) mA	See Fig. 27 : $Z_L = 600\Omega$ note 14
Loop detector, current threshold	I_{TH}	I_{TH} – 20%	I_{TH}	I_{TH} + 20 %	A	See Fig. 27 : $I_{TH} = 350 \div R_{TH}$
Ring trip detector offset voltage	V_{RTO}	– 50		+ 50	mV	See Fig. 25 : $V_{BB} < V_{CMM} < -2V$
Ring trip detector bias current	I_{RTB}			1.0	µA	See Fig 25 : $I_{RTB} = \frac{1}{2}(I_{RTDA} + I_{RTDB})$

NOTES
10. Distortion measured in the bandwidth 300-3400Hz.
11. Distortion measured in the bandwidth 20Hz-100kHz.
12. f_1 & f_2 in the range 300-3400Hz, $f_1 \div f_2$ = non-integer. Measure $(2f_1-f_2)$ relative to f_1 or f_2 level.
13. Feed resistance is (40k ÷ 50)Ω i.e. R_{DC} = 40kΩ. Nominal apparent battery = – 50V.
14. Constant current in standby mode is approximately $(600 \div R_{TH})$mA.

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Ground key active state	R_{G1}	900		10	kΩ	See Fig 26 : SW1 Closed RW = 300Ω, notes 15 & 16
Ground key active state	R_{G2}	1.7		10	kΩ	See Fig 26 : SW1 Open RW = 0Ω, notes 15 & 16
Earth call, disconnect A, standby B	R_{G3}	1.7		10	kΩ	See Fig 26 : SW1 Open RW = 0Ω, note 16
Relay driver, saturation voltage (active)	V_{SAT}			1.8	V	I = 60mA drawn from external positive supply
Relay driver, leakage current (non-active)	I_{LK}			0.1	mA	RING – = 0V, RING + = + 6V
Relay driver, clamp voltage	V_{CL-}	V_{BAT}–3.0			V	I = 25mA from RING –

NOTES
15. For polarity-reversed state, connections to LA and LB are reversed.
16. 'Must Detect' and 'Must Not Detect' are indicated in the Min. and Max. columns, respectively.

Digital Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Input low voltage (D0-D2,E0,E1,CHCLK)	V_{IL}			0.8	V	
Input high voltage (D0-D2,E0,E1,CHCLK)	V_{IH}	2.0			V	
Input low current (D0-D2,E0,E1,CHCLK)	I_{IL}			– 0.25	mA	V_{IL} = 0.4V
Input high current (D0-D2,E0,E1,CHCLK)	I_{IH}			0.04	mA	V_{IH} = 2.4V
$\overline{DET}$ output low voltage	V_{OL}			0.4	V	I_{OL} = 0.8mA
$\overline{DET}$ output high voltage	V_{OH}	2.4			V	I_{OH} = 0.1mA
$\overline{DET}$ output, internal pull-up	R_{OUT}	10		20	kΩ	
Propagation delay, E1 to $\overline{DET}$	t_{PD}			4	μs	$\overline{DET}$ 6.2kΩ to V_{CC}, 15pF to AGND
Loop Detector make response time	t_{LM}			3	ms	Z_L = 2kΩ
Loop Detector break response time	t_{LB}			3	ms	Z_L = 2kΩ
CHCLK input frequency	F_{CLK}		256		kHz	
CHCLK min. pulse width	T_{CLK}		500		ns	

Recommended Operating Range

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply voltage	V_{CC}	4.75	5.0	5.25	V	
Negative supply voltage	V_{EE}	– 4.75	– 5.0	– 5.25	V	
Battery supply voltage	V_{BAT}	– 44	– 48	– 52	V	
Battery ground voltage	V_{BGND}	– 0.3		+ 0.3	V	
Ambient temperature	T_{AMB}	0		70	°C	

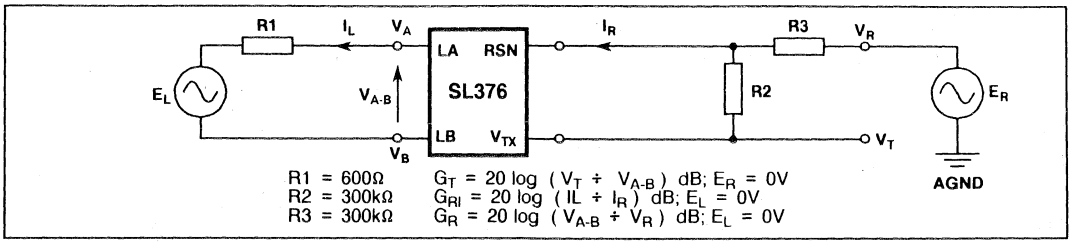


Fig.14 Test configuration (Note the SL376 block = Fig. 27).

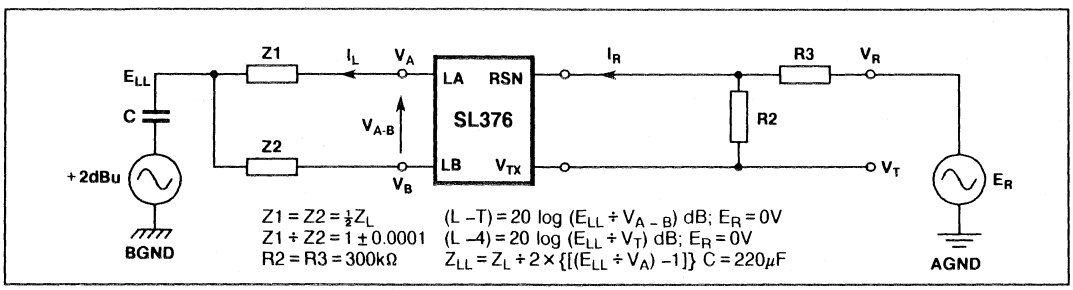


Fig.15 Test configuration (Note the SL376 block = Fig. 27).

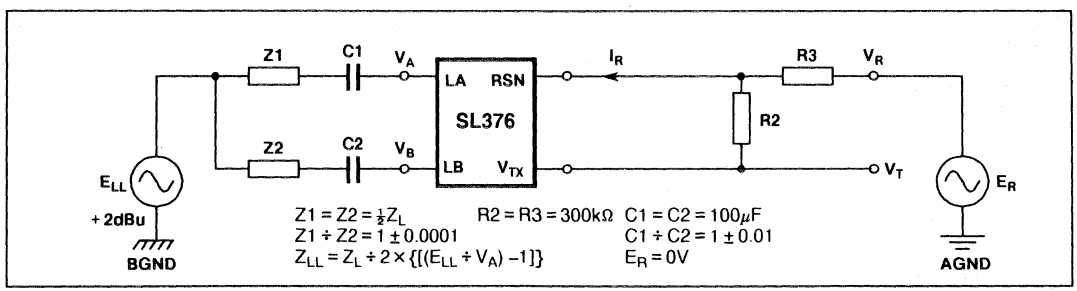


Fig.16 Test configuration (Note the SL376 block = Fig. 27).

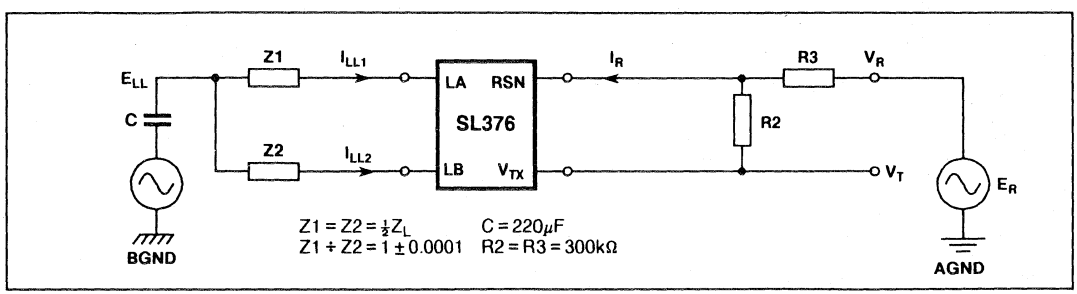


Fig.17 Test configuration (Note the SL376 block = Fig. 27).

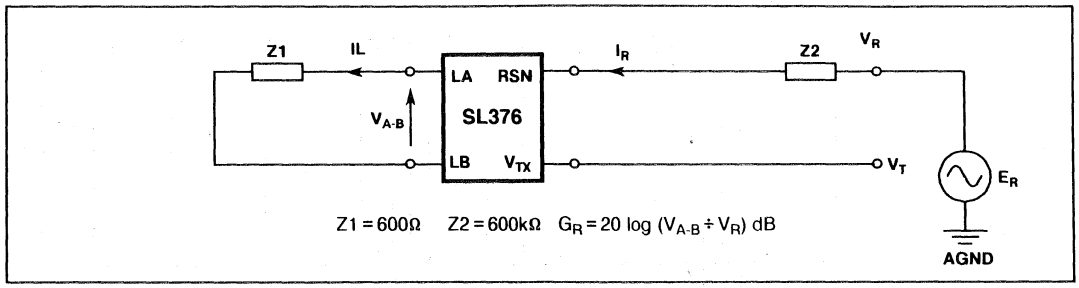


Fig.18 Test configuration (Note the SL376 block = Fig. 27)

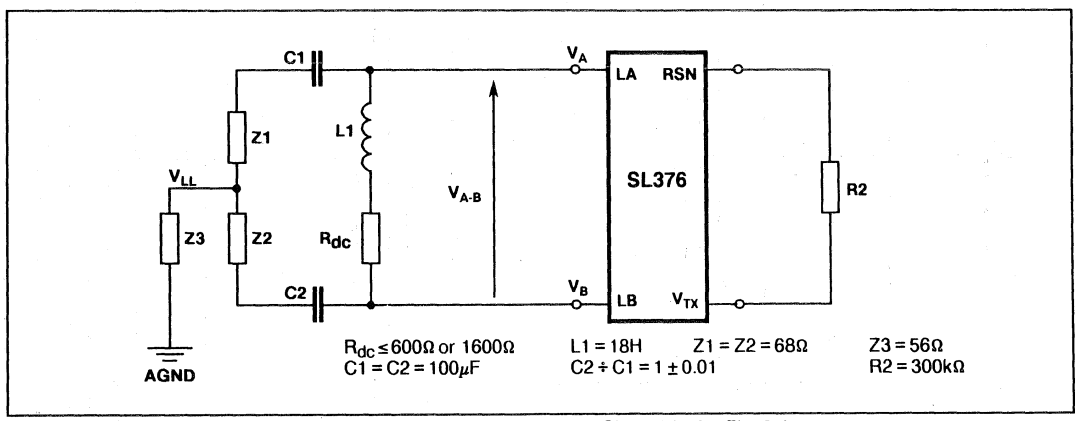
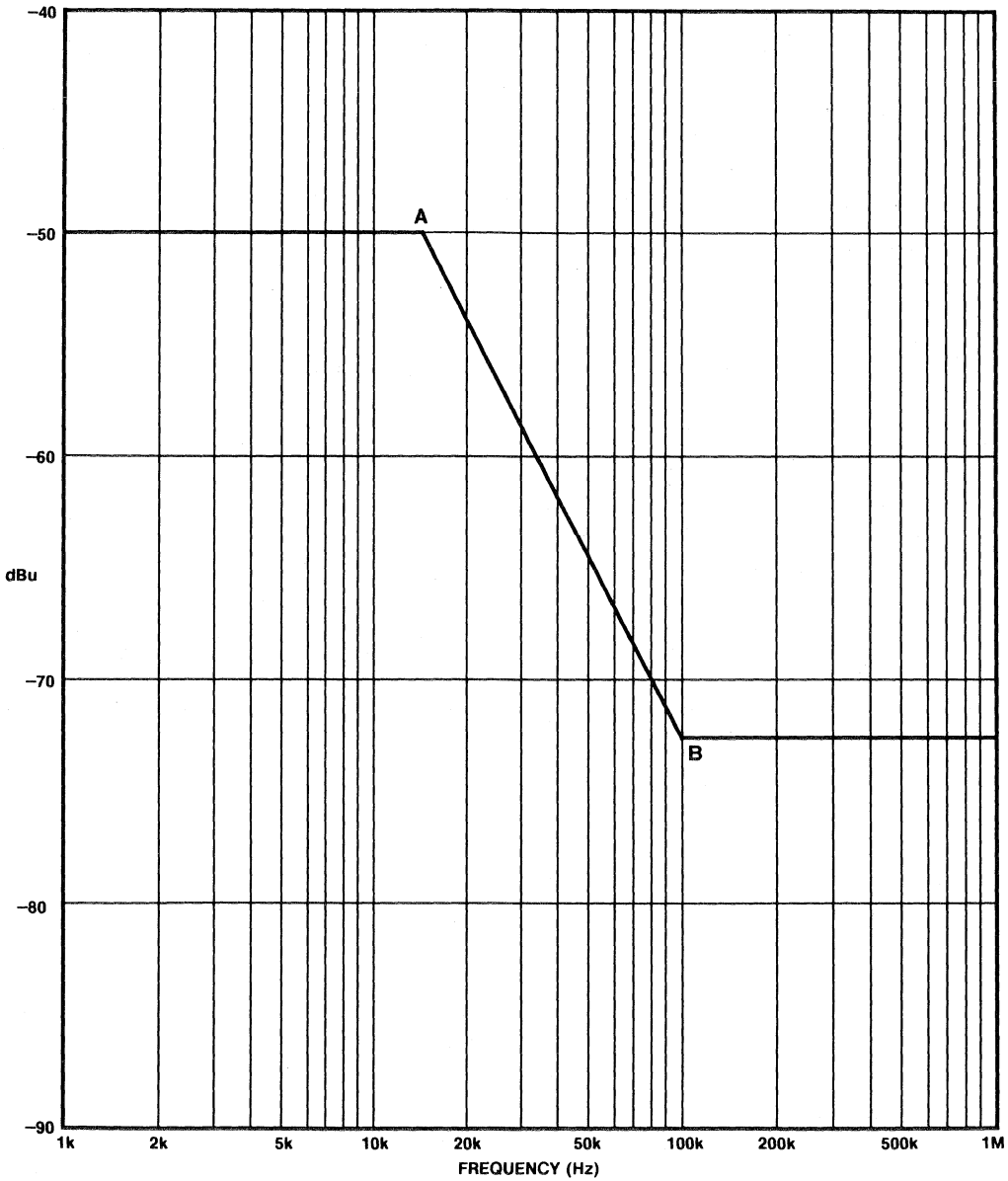


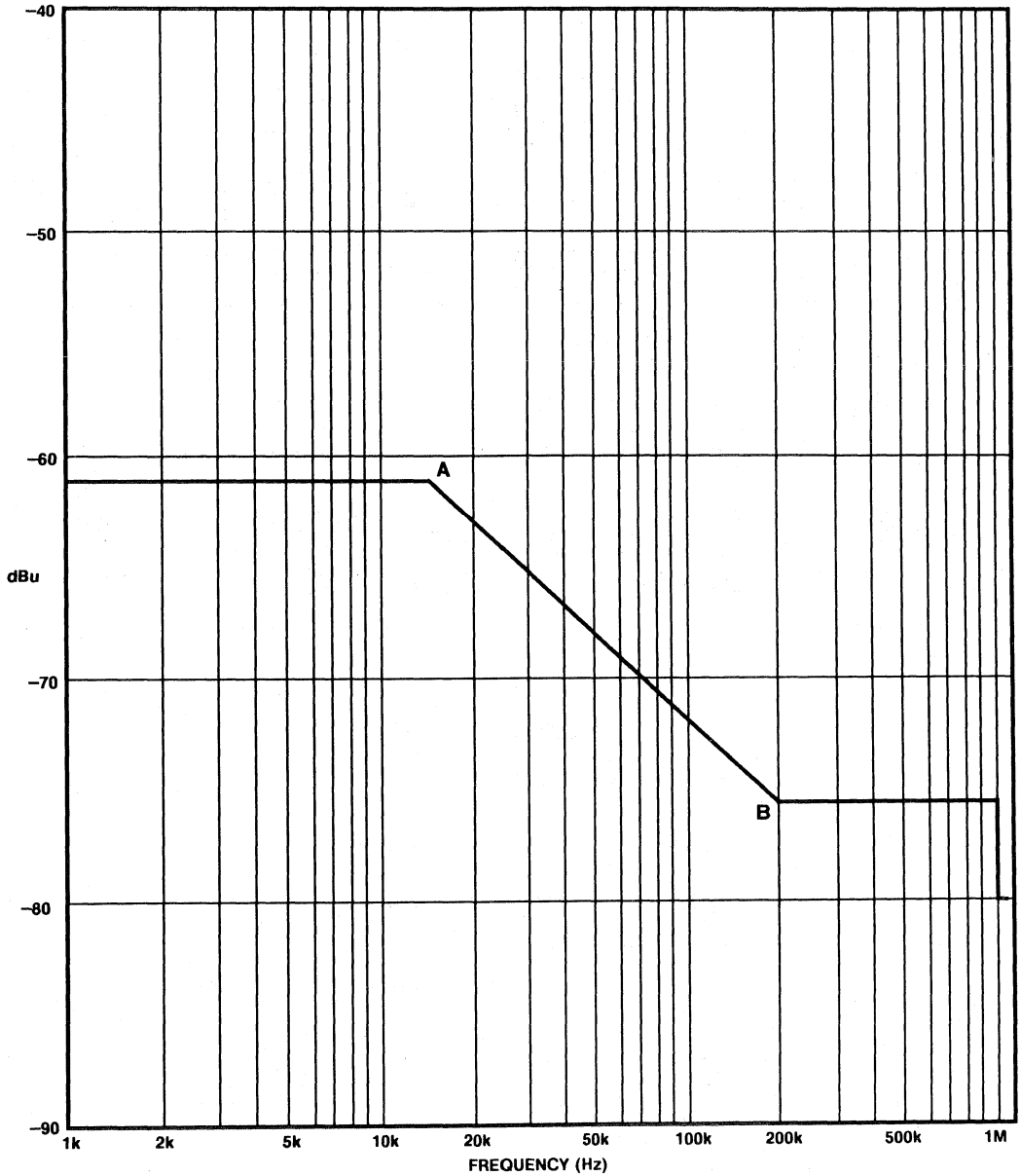
Fig.19 Test configuration (Note the SL376 block = Fig. 27).



FREQUENCY AT CENTRE OF BAND

A = 15kHz –50dBu
B = 100kHz –73dBu
Bandwidth = 3kHz Minimum Centre Frequency = 1.6kHz
V_{A-B} < –73dBu. f > 1MHz

Fig.20 2-Wire differential noise



FREQUENCY AT CENTRE OF BAND

A = 15kHz –61dBu
B = 200kHz –75dBu
Bandwidth = 3kHz
V_{LL} < –80dBu. f > 1MHz

Fig.23 2-Wire longitudinal noise

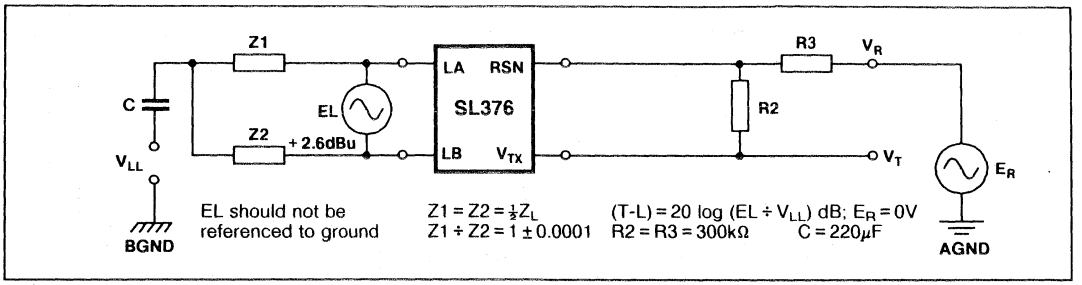


Fig.22 Test configuration (Note the SL376 block = Fig. 27)

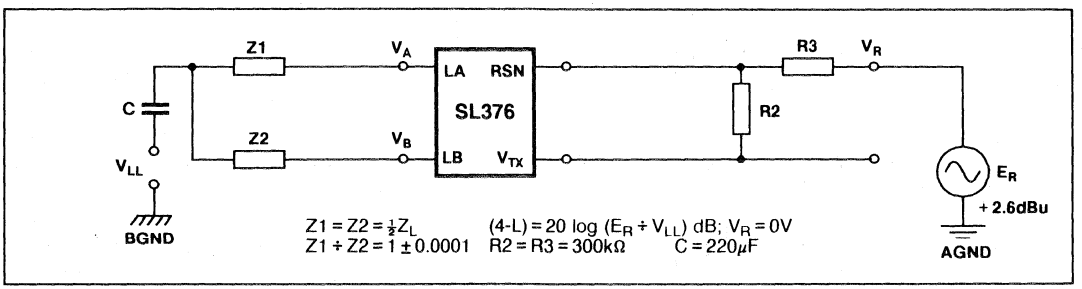


Fig.23 Test configuration (Note the SL376 block = Fig. 27).

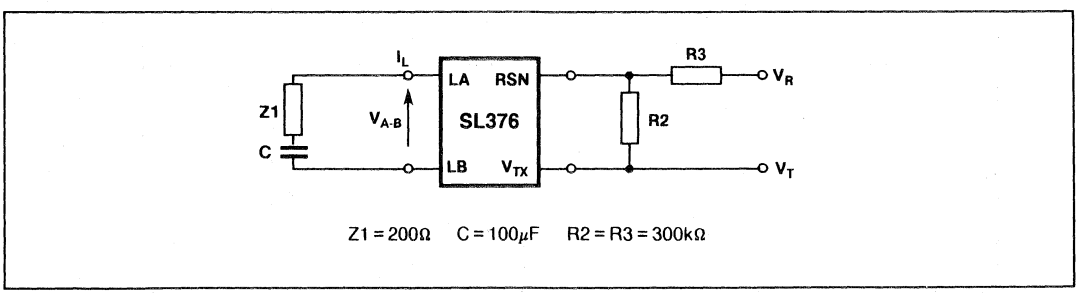


Fig.24 Test configuration (Note the SL376 block = Fig. 27).

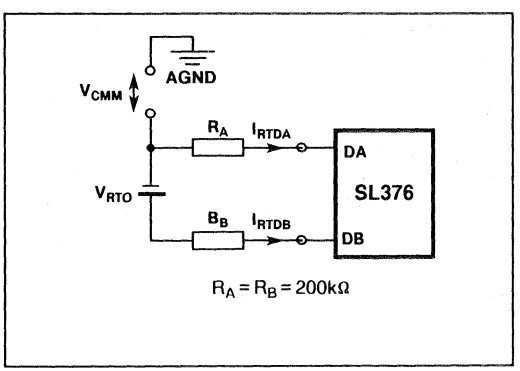


Fig.25 Test configuration (Note the SL376 block = Fig. 27).

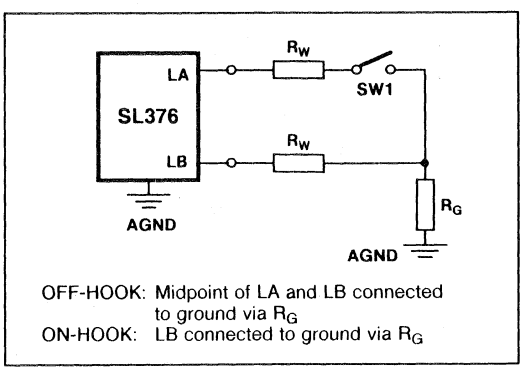
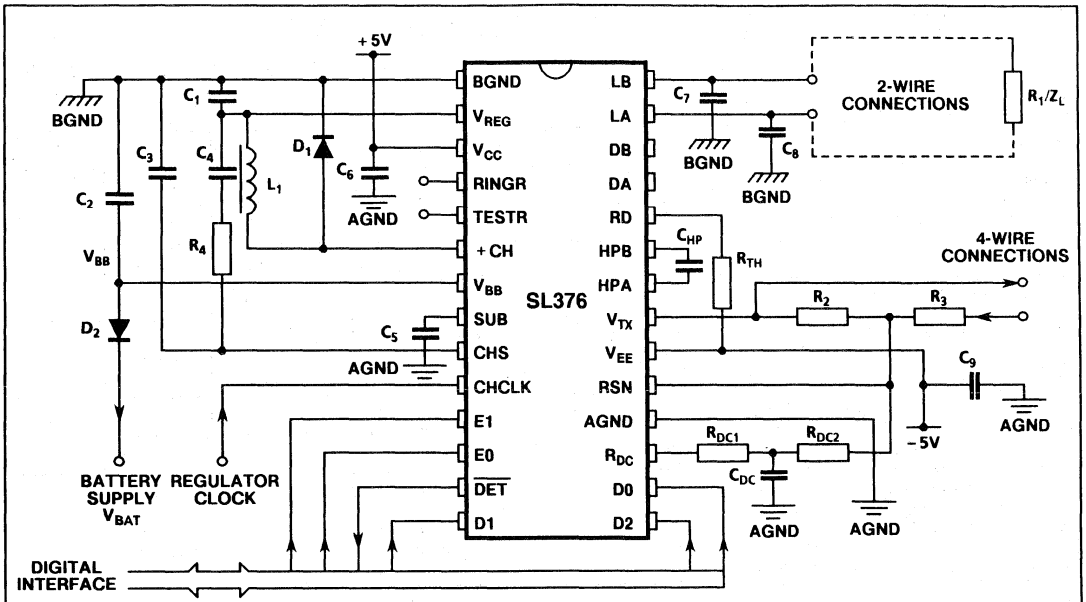


Fig.26 Test configuration (Note the SL376 block = Fig. 27).



C_1 = 470n	C_6 = 100n	C_{DC} = 100n	R_{TH} = 56kΩ
C_2 = 470n	C_7 = 2.2n	D_1 = 100V,100mA	$R_{DC1} = R_{DC2} = \frac{1}{2}R_{DC}$ = 20kΩ
C_3 = 560p	C_8 = 2.2n	D_2 = 100V,100mA	R_2 as Test Configuration
C_4 = 8.2n	C_9 = 100n	L_1 = 1mH	R_3 as Test Configuration
C_5 = 330n	C_{HP} = 330n	R_4 = 2.4kΩ	Z_L: See Electrical Characteristics

For all tests assume AGND = BGND.

Fig.27 Test circuit for Figs. 14-19 and 22-26

ABSOLUTE MAXIMUM RATINGS* - Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value		Units
		Min.	Max.	
Battery supply voltage	V_{BB}	– 70	+ 1.0	V
Battery voltage, rate of change	V_{BBR}	– 0.4	+ 0.4	V/µs
Continuous battery ground voltage	V_{BGNDC}	– 2.0	+ 2.0	V
Intermittent (10µs) battery ground voltage	V_{BGNDI}	– 4.0	+ 4.0	V
Positive supply voltage	V_{CC}	– 0.4	+ 7.0	V
Negative supply voltage	V_{EE}	– 7.0	+ 0.4	V
Subscriber line voltage on LA, LB or both, continuous	V_{LC}	– 75.0	+ 1.0	V
Subscriber line voltage on LA, LB or both, 10ms duration, f = 0.1Hz rate	V_{LR1}	– 70.0	+ 5.0	V
Subscriber line voltage on LA, LB or both, 1µs duration, f = 0.1Hz rate	V_{LR2}	– 90.0	+ 10.0	V
Subscriber line voltage on LA, LB or both, 250ns duration, f = 0.1Hz rate	V_{LR3}	– 120.0	+ 15.0	V
Switched regulator voltage (off)	V_{CH}	V_{BB}	+ 1.0	V
Switched regulator current (on)	I_{CH}		150	mA
RING + to RING – relay driver voltage	$V_{RING\pm}$		+ 70	V
RING to V_{BAT}	$V_{RINGVBAT}$	V_{BAT}	+ 80	V
Relay source current	I_{RING}		60	mA
Ring-Trip input voltage (DA or DB)	V_{RT}	V_{BB}	0	V
Ring-Trip input current (non-repetitive 10 ms pulse)	I_{RT}	– 2.0	+ 2.0	mA
Digital input voltage	V_{ID}	– 0.4	V_{CC}	V
Digital input current (sink)	I_{ID}		– 5.0	mA
Digital output voltage	V_{OD}	– 0.3	V_{CC}	V
Digital output current (source)	I_{OD}		3	mA
Storage temperature	T_{ST}	– 55	+ 150	°C
Operating junction temperature	T_{JOP}		+ 150	°C
Package power dissipation (DG28 package)	P_{PDG28}		1.5	W
Package power dissipation (LC28 package)	P_{PLC28}		1.2	W

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

SL7950

SUBSCRIBER LINE INTERFACE CIRCUIT

The SL7950 is a Subscriber Line Interface Circuit (SLIC) for use at the telephone exchange or PABX end of a telephone line.

It provides power feed, transmits and receives voice signals, controls ringing, supports line testing and detects Ring Trip or Off-Hook conditions. These functions can be programmed to provide the flexibility required for different telephone networks.

The SL7950 is fabricated using bipolar technology.

FEATURES

- Low Power Line Feed via Regulator
- Constant Voltage Feed/Programmable Resistive Feed Independent of Battery
- Programmable AC Termination Impedance
- Good Longitudinal Balance
- Ring Trip Detection
- Programmable Off-Hook Detection
- Disconnect and Low Power Standby Modes
- A-Leg Disconnect, B-Leg Standby Mode
- Normal or Reversed Line Polarity Operation
- Thermal Shut-Down Protection
- Ring and Test Relay Drivers
- Direct Replacement for Am7950

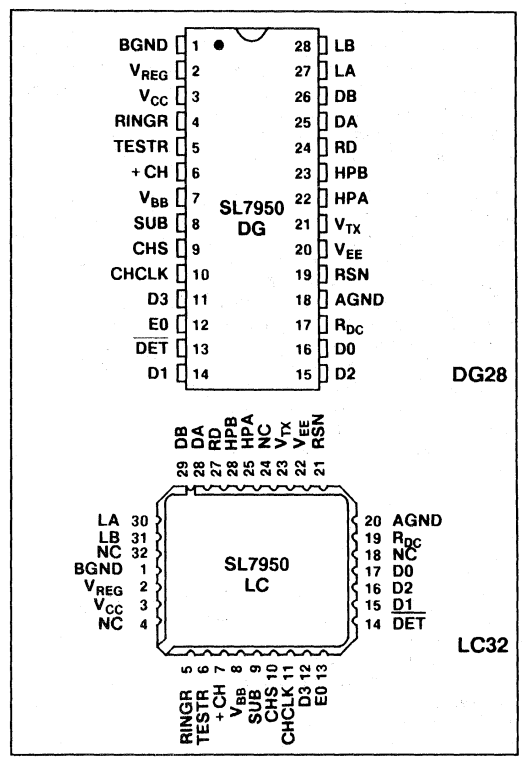


Fig. 1 Pin connections - top view (not to scale)

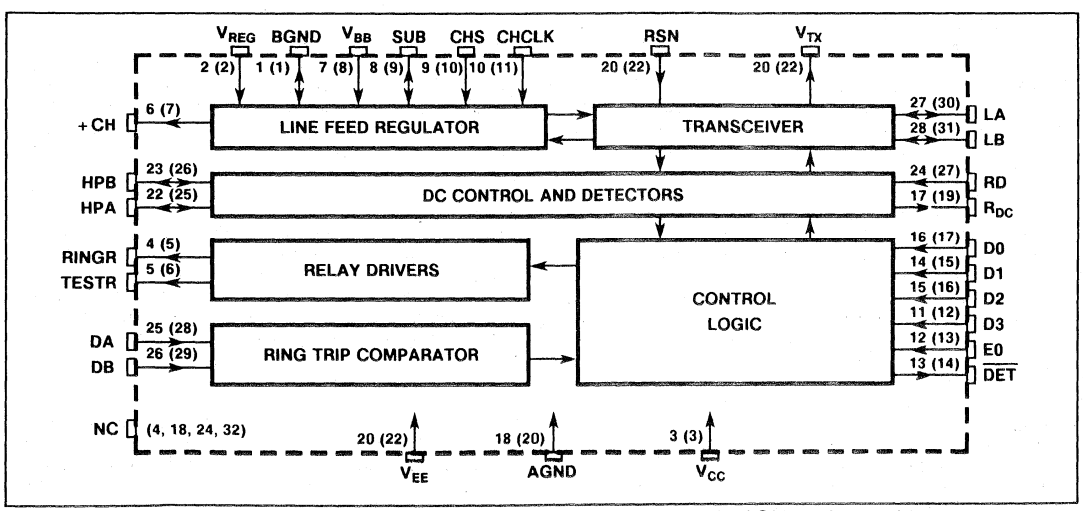


Fig. 2 : Functional block diagram (pin numbers in brackets are for LC32 package only)

FUNCTIONAL OVERVIEW

The SL7950 Subscriber Line Interface Circuit (SLIC), together with some external components, provides most of the line interface functions for ordinary or PABX line connections in a telephone network. It performs the interface between the two wire line and an ALAP (Analog Line Audio Processor)/COMBO, such as the GEC Plessey Semiconductors MV3010 PSLAC (Plessesy Subscriber Line Audio Circuit) .

The SLIC circuit contains several functional blocks to achieve the design aims (Fig.2). Firstly, the Transceiver consists of the two wire port, pins LA and LB. These pins are fed from the 4 wire input (RSN) controlling AC conditions, and from the Line Feed Regulator and DC Control blocks, controlling DC conditions. The 2 wire transverse AC signal is fed onto the 4 wire transmit output, V_{TX}.

Power dissipation is minimised, under varying line conditions, by the Line Feed Regulator which adjusts the internal high voltage supply to that required for line feed. It consists of a switching regulator which can be synchronised to a 256kHz clock.

DC line conditions at the 2 wire interface are determined by the DC Control block. These DC conditions (modes of operation) are set by the Control Logic, which also monitors line status (On/Off-Hook) via the DC Control block detectors (Loop/Ring Trip). The control logic also controls the Ring and Relay Driver for Ringing mode of operation and an undedicated Test Relay driver.

A brief outline of the device functionality is given below, before a more detailed discussion of the SLIC circuitry in the Functional Description section.

LINE FEED

Line loop (pins LA & LB) feeding is obtained from the battery supply V_{BB} by means of an internal power circuit, which can be set to different modes of operation (refer to Table 2). These modes are as follows:

Standby Mode

Standby mode is the SLIC's low power mode in which the battery feed circuit limits the DC loop current to a level just sufficient to enable the SLIC to detect current above the On/Off-Hook threshold. This mode is used when the subscriber is Off-Hook and no call is in progress, or if On-Hook, to save power.

Disconnect A and B Leg

This mode programs the SLIC such that the A and B leg output amplifiers are turned off, preventing current flow to the line.

Disconnect A, Standby B Leg

This is the SLIC Standby mode with the A Leg amplifier turned off, so that current can only flow in the B Leg. In this state it is only possible to detect the application of a ground to the B Leg.

Active Mode

This is the normal operating mode with a call in progress. The SLIC is used as a resistive feed device (unbalanced DC line feeding is performed), with the feed resistance being set by external resistors.

Polarity reversal

The polarity of the feeding voltage at the SLIC can be reversed on command, in Active and Standby modes. All Active and Standby conditions apply equally to the respective reverse conditions. In these conditions the polarity of any DC parameter is reversed.

Ringing

This mode enables the Ring Relay output and selects the Ring Trip comparator. It does not provide DC line feed or AC ringing voltage which must be supplied externally (via the ring relay).

Test Mode

Testing of the line is not performed by the SLIC. This mode enables external access to the telephone line by directly driving the test relay.

SUPERVISION

The SLIC provides an Off-Hook (or loop) Detector (OHD) and a Ring Trip Detector (RTD). These are described below, in addition to the SLIC on-chip thermal protection.

Off-Hook Detector

The Off-Hook Detector recognises the loop status by means of a threshold circuit. The OHD operates in Standby and Active modes (with or without polarity reversal), and in the presence of longitudinal currents. The detector threshold is nominally the same in Standby and Active modes, the actual level being externally programmable.

Ring Trip Detector

This detects when a subscriber goes off-hook during the application of a ringing signal (normally 25Hz) within a maximum delay of 150ms (determined by external components - see Applications section). The detector is active when the Ring Relay Driver is activated.

Thermal Protection

In conditions which cause the chip temperature to rise above a critical level (~150°C), the thermal protection will operate. This switches off the line current and therefore reduces the power dissipation.

TRANSMISSION

The signal transmission functions include 2 to 4-wire and 4 to 2- wire conversions.

The 2-wire termination impedance of the SLIC is programmed by external components. Transmit and Receive Gain are fixed and are nominally both unity (0dB), with the 2- wire port terminated in a matched load.

All the transmission parameters apply when the SLIC is operating in the presence of longitudinal currents, as specified in the Electrical Characteristics.

CONTROL

The SLIC is provided with a digital interface for controlling the 2-wire line status and passing line status information to the line card/system hardware. The operating characteristics can be selected by hardware with external components (see Digital Interface).

SIGNALLING (METER PULSE INJECTION)

Injection of high amplitude high frequency meter pulses is not supported by the SL7950. If this function is required, then the GPS SL376 Metering SLIC can be used instead (refer to separate Data Sheet). However, RSN is a convenient summing point should the addition of low level signals be desired.

RINGING

The application of the ringing voltage to the subscriber line can be via a relay or suitable high voltage crosspoint, external to the SLIC. This component is driven by the on-chip Ring Relay Driver. The relay is connected between RINGR and V_{BAT} (the external battery supply), via a current-limiting resistor if necessary, with current being sourced internally from V_{CC}.

When the SLIC is set to RING mode, the Ring Relay Driver output will be activated to energise the ring relay. The relay should be connected so as to cause the line to be disconnected from the SLIC and connected to a suitable ringing supply (continuous) voltage. Ring cadence can then be obtained by de-energising and re-energising the relay as required.

OVERVOLTAGE PROTECTION

Overvoltage protection is required to protect the SLIC from such line phenomena as lightning strikes, and induced AC signals from, or direct contact with, power lines. This protection can be realised with components external to the SLIC. A suitable form of protection for the SL7950 is described in the SL373/SL376 Application Note AN82.

INTERFACES

The SLIC has three main interfaces to external circuitry. These are the 2-wire, 4-wire and Digital interfaces which are described below.

Subscriber Line Interface (2-wire port)

Pins LA and LB form the Subscriber Line Interface providing line feed, signalling supervision and voice transmission between the subscriber's apparatus and exchange. It exhibits very good balance about ground to minimise the crosstalk between adjacent pairs in the local cable and noise from longitudinal interference. The termination impedance is set externally by Z_{TX} (see Fig. 3 and Functional Description).

The 2-wire port is designed to offer a low impedance to any longitudinal signals that appear on the subscriber line and the resulting signal level at the 4-wire output port is minimised. It is able to handle longitudinal currents on the subscriber line in all modes of operation, except Disconnect, Ringing and Disconnect A Standby B modes when the SLIC 2-wire port is no longer connected to the line.

Analog 4-wire interface

Two pins of the SLIC (V_{TX} and RSN), together with associated grounds, provide the 4 wire interface to an ALAP or COMBO device. Both the transmit (V_{TX}) and receive (RSN) signals are unbalanced and have fixed gain settings. The V_{TX} pin has a low output impedance, whilst the RSN pin is a low impedance virtual earth input. The input current is a combination of the receive voice signal from the ALAP, line feed current programmed by the R_{DC} pin (see Applications section) and termination of the V_{TX} pin.

Hybrid Balancing is not provided on the SLIC. This can be done by an ALAP such as the MV3010 PSLAC which uses DSP techniques, including an Adaptive Echo Cancellation feature.

Digital Interface

This is a parallel interface providing control of all the SLIC operating modes and indication of line status information. It consists of the 6 pins as listed in Table 1, the functions of which are described in Table 2.

Pin designation	Pin description
D0	Data Input
D1	Data Input
D2	Data Input
D3	Test Select Input
E0	Detector Data Output Enable
$\overline{DET}$	Detector Data Output

Table 1 Digital interface pin designation

Mode	D3	D2	D1	D0	E0	$\overline{DET}$ output status (note 3)	Test relay driver
Disconnect A & B legs		0	0	0	1	Ring Trip (note 4)	
Ringing		0	0	1	1	Ring Trip (note 4)	
Active (non-ringing)		0	1	0	1	Loop Detect	
Standby		0	1	1	1	Loop Detect	
Disconnect A, Standby B		1	0	0	1	Loop Detect	
Reserved		1	0	1	1	-	
Active, polarity reversed		1	1	0	1	Loop Detect	
Standby, polarity reversed		1	1	1	1	Loop Detect	
As selected by D2-D0 (note 1)		0/1	0/1	0/1	0	1 (Off)	
Test On	0	0/1	0/1	0/1	0/1	Invalid (note 2)	Enabled
Test Off	1	0/1	0/1	0/1	0/1	Invalid (note 2)	Disabled

NOTES

1. D2, D1 and D0 still change SLIC status even though $\overline{DET}$ output is forced to 1 (5V)
2. D2, D1 and D0 still change SLIC status; depending on the application, the $\overline{DET}$ output may be invalid.
3. $\overline{DET}$ = 1 for On-Hook (high line impedance), $\overline{DET}$ = 0 for Off-Hook (low line impedance).
4. $\overline{DET}$ = 1 for Voltage DA > DB , $\overline{DET}$ = 0 for Voltage DA < DB.

Table 2 Digital interface functional designation

FUNCTIONAL DESCRIPTION

VOICE TRANSMISSION AND RECEPTION

It is conventional to assign the signal directions from the point of view of the served telephone set. The receive direction is towards the served telephone and the transmit direction is from it.

The basic voice circuit for the device is shown in Fig.3. The current which flows on the line, into LA and out of LB, is 1000 times the current which flows into RSN and through the device to AGND.

The AC voice current flowing into RSN is composed of the current from V_{RX} through Z_{GR}, which controls the signal received at the remote telephone and a current from V_{TX} through Z_{TX} which controls the termination impedance. There is also a DC current at RSN which is analysed later in the discussion on DC line feed.

The 2-wire termination impedance is $Z_{AB} = (Z_{TX} \div \alpha)$ where α ($\simeq 1000$) is the current gain between RSN and I_L (see Fig.3). This can be checked by setting V_{RX} to zero.

The receive gain, for normal voice signals (at V_{RX}), is inversely proportional to Z_{GR}. The actual value, which is negative, can be obtained by setting $(V_L)_{ac}$ equal to zero in Fig.3. This gives:

AC voltage between LA and LB $(V_{LA}-V_{LB})_{ac}$

$$= (V_{LA} - V_{LB}) - (V_{HPA} - V_{HPB})$$
$$= (I_L)_{ac} \times \{Z_{AB} \| Z_L\}$$
$$= -\left(\frac{Z_L \times \frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right) \frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}$$

i.e. minus the ratio of the line and terminating impedances (Z_L and $Z_{TX} \div \alpha$) in parallel, to the receive impedance divided by the current gain ($Z_{GR} \div \alpha$). This expression simplifies to :

$$= \frac{-V_{RX}\alpha Z_L Z_{TX}}{(\alpha Z_L + Z_{TX})Z_{GR}}$$

In the transmit direction, the voltage at V_{TX} is the superposition of the voltage from the line, with the voltage produced on the line from V_{RX}, i.e:-

$$V_{TX} = \left[\left(\frac{\frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right) V_L - \left(\frac{Z_L \times \frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right) \frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}\right]$$

This expression simplifies to :

$$V_{TX} = \frac{[Z_{GR}(V_L)_{ac} - \alpha Z_L V_{RX}]Z_{TX}}{(\alpha Z_L + Z_{TX})Z_{GR}}$$

This equation can be used to determine the transmit gain, from $(V_L)_{ac}$ to V_{TX}, by setting $V_{RX} = 0$ which gives $Z_{TX} \div (\alpha Z_L + Z_{TX})$ and also The 4-wire to 4-wire gain, V_{RX} to V_{TX}, by setting $(V_L)_{ac} = 0$, which gives us the alternative result $-\alpha Z_L Z_{TX} \div [(\alpha Z_L + Z_{TX})Z_{GR}]$. If fuse resistors are included in the 2-wire loop, then Z_L is modified to become $(Z_L + 2R_F)$ in the above equations.

The transmission circuitry also contains a longitudinal feedback circuit, such that the SLIC appears as typically 25Ω resistors from LA and LB to a bias voltage (see DC Line feed section). This bias voltage comes from the DC feed circuitry. The feedback circuit attenuates longitudinal signals from the transmit path, and has no effect on transverse signals.

DC LINE FEED (Active Mode)

DC line feed (loop) current $I_L = \frac{1}{2}(|I_A - I_B|)$ is provided by the device when it is in non-ringing modes. In ringing mode, DC line feed and AC ringing voltage are normally applied through the ring relay which is controlled by the device. The line feed current is reduced during standby operation.

In Active mode, Power feed is controlled by the resistance R_{DC} between the R_{DC} pin and the RSN pin (Fig.4). Again, the current in the 2-wire loop will be 1000 times the current into RSN. Operation of the DC feed circuitry is described with reference to Fig.4, which shows a conceptual model.

For the normal line feed region, a voltage, V_{DC}, of magnitude $(50 - |V_{DCT}|) \div 20$ (where $V_{DCT} = |V_{LA} - V_{LB}|$) is produced at the R_{DC} pin, the sign of which determines normal or reverse polarity operation. If negative, normal polarity is established and if positive, reverse polarity will occur (polarity is set by control logic - see Table 2). This normal line feed region exists when $|V_{BAT}| - |V_{DCT}| \geq V_{SG}$ ($V_{SG} = 15V$ nominally, $V_{DCT} = |V_{LA} - V_{LB}|$), else the saturation guard circuit is active (described later).

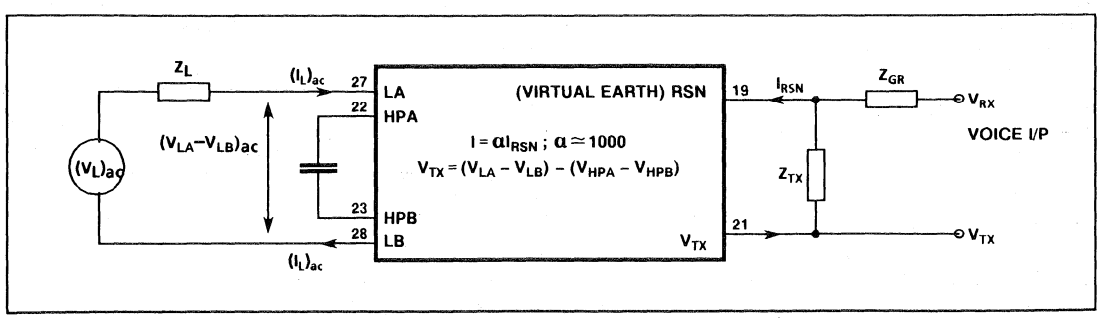


Fig.3 Voice circuit (pin numbers are for DG28 package)

Note that the internal resistors, R_{HP}, and external capacitor, C_{HP}, form a low pass filter network (the discussed furtherion on C_{HP} in Application Note AN82, Applications General Considerations section is also valid for the SL7950). During the action of reversing polarity, the resistors R_{HP} are momentarily shorted to reduce the time taken for the DC voltage on C_{HP} to change sign.

The combination of the 1/20 Op Amp and the ×1000 virtual earth input current amplifier, means that the feed resistance is determined by ($R_{DC} \div 50$), i.e. $R_{FEED} = R_{DC} \div 50 = [(R_{DC1} + R_{DC2}) \div 50]$. If fuse resistors are included in the 2-wire loop, then the actual feed resistance will be:

$$R_{FEEDTOT} = 2R_{FUSE} + R_{FEED} = 2R_{FUSE} + [(R_{DC}) \div 50]$$

As an example, to set $R_{FEEDTOT} = 840\Omega$, then if the resistors $R_{FUSE} = 20\Omega$, then $R_{DC1} = R_{DC2} = 20k\Omega$, since:-

$$(R_{DC1} + R_{DC2}) = [R_{FEEDTOT} - 2R_{FUSE}] \times 50$$
$$= [840 - 40] \times 50 = 40k\Omega$$

The values of R_{DC1} and R_{DC2} should be kept equal, forming a low pass filter network with C_{DC} to reduce chopper noise from the R_{DC} pin (see also discussion in AN82 Applications General Considerations section). The time constant of this network (C_{DC} and $R_{DC1}//R_{DC2}$) also affects the time taken for a polarity reversal, and it is normally ≈ 1.5ms.

The remaining circuitry models the action of the saturation guard circuit. This operates to reduce the voltage at the R_{DC} pin when $|V_{BAT}|-|V_{DCT}| < V_{SG}$. V_{SG} is a notional threshold voltage which is the headroom between the value of V_{DCT} and the battery voltage, at the point where saturation guard becomes active (this includes the diode drop in series with V_{BAT}, D_2 Fig. 7). Thus, when the comparator determines the above condition, the magnitude of the difference is used to reduce the voltage at R_{DC}.

The total line feed characteristic is shown graphically in Fig. 6a and 6b.. The nearly constant voltage region (V_{DCT} constant) is due to the action of the saturation guard circuit. The slope of this region will increase with any fuse resistance. Fig. 6b plots the loop current value as a function of line resistance R_L. The example shown is that of an 800Ω feed resistance, the graphs being obtained by using the simple models of Figs. 5a and 5b (0Ω fuse resistors). Figs. 6a and 6b also show the action of V_{BB} on the line characteristics.

With the saturation guard inactive, normal line feed conditions apply such that the feed and line/loop resistance determine I_L by the following relationship:

$$I_L = 50 \div (R_L + R_{FEEDTOT})$$

The line voltage is then simply determined by the relationship $V_L = I_L \times R_L$. This gives the example shown in Fig. 6a and 6b.

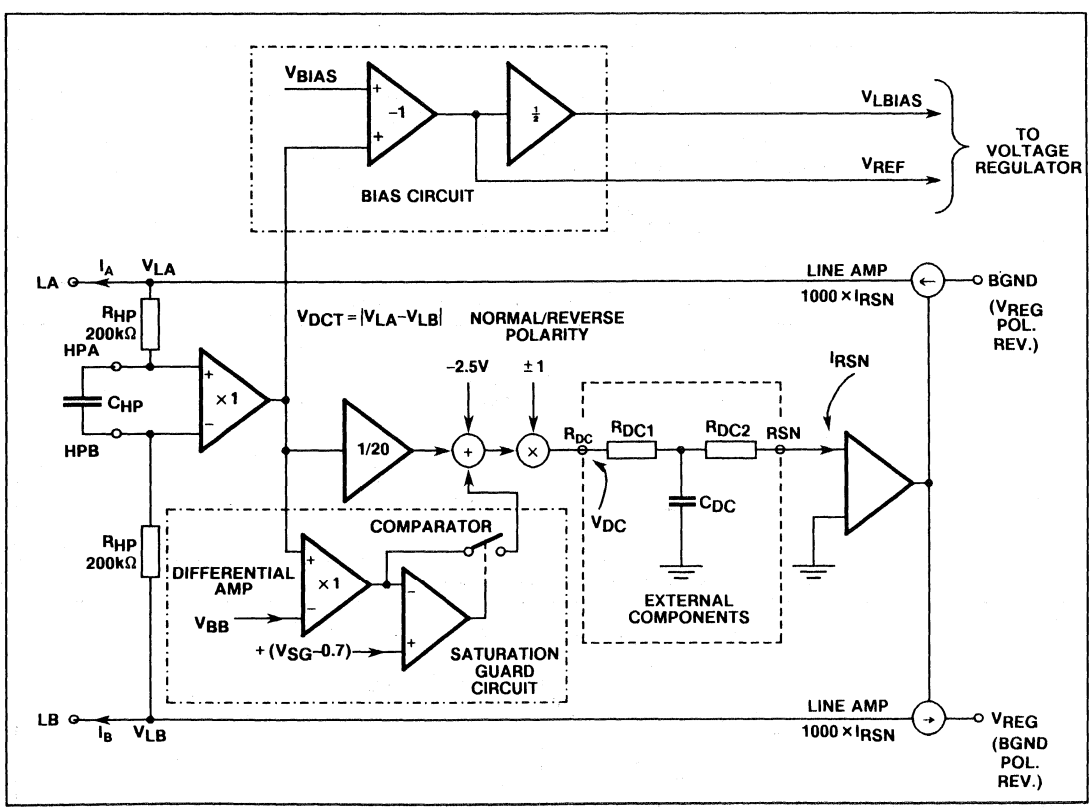


Fig.4 DC power feed circuit model.

When the saturation guard is active, then the line voltage is effectively held constant due to the reduction of the voltage at the R_{DC} pin. Thus, line conditions are set by the following:

$$I_L = [(|V_{BAT}|-V_{SG}) \div (R_L + 2R_{FUSE})]$$

To determine the line resistance (R_{LSG}) and current (I_{LSG}) at which the saturation guard becomes active, these parameters are obtained by equating the two expressions for Normal and Saturation Guard regions. Thus :

$$I_{LSG} = 50\ (50 + V_{SG} - |V_{BAT}|) \div R_{DC}$$

$$R_{LSG} = \frac{(|V_{BAT}| - V_{SG})R_{DC}}{(50 + V_{SG} - |V_{BAT}|)50} - 2R_{FUSE}$$

The resultant line voltage (V_{LSG}) that occurs is obtained by the ohmic relationship of I_{LSG} and R_{LSG} (see Fig. 6a). This will become $V_{LSG} = (|V_{BAT}|-V_{SG})$ when $2R_{FUSE} = 0$. The open circuit line voltage $V_{LOC} \approx (|V_{BAT}|-V_{SG})$, at $R_L = \infty\Omega$, will always be greater than V_{LSG}, even when $2R_{FUSE} = 0$. This change in voltage between V_{LSG} and V_{LOC} will be greater at lower battery voltages. Fig. 6a shows the nominal effect.

DC LINE FEED (Standby Mode)

For Standby mode, the loop current is limited to just sufficient for the Loop Detector to sense Off-Hook. Normally this threshold (I_{DET}) is set externally by a resistor, R_{TH} (see Control and Signalling section). The limited loop current (I_{LIM}) is also determined by R_{TH} via a conversion factor K_{LIM} (nominally 1.7, see Electrical Characteristics) such that :

$$I_L \leq I_{LIM} = K_{LIM} \times I_{DET}$$

The slope impedance of this characteristic is almost a constant current, as shown in Fig. 6a. Since $K_{LIM} > 1$, the current level is still sufficient to detect the Off-Hook threshold (see Control and Signalling section).

LINE POLARITY

Normal polarity (in active or standby modes) consists of the LA pin DC voltage near BGND and the LB pin DC voltage near V_{BB}. Under these conditions, $I_L = +\frac{1}{2}|I_A-I_B|$ and the voltage at the R_{DC} pin is negative. Reverse polarity will give the LA pin DC voltage near to V_{BB}, LB pin DC voltage near to BGND, $I_L = -|I_A-I_B|$ and the R_{DC} pin voltage is positive.

BIAS CIRCUIT

The Bias circuit produces two reference voltages, both referred to ground. These are V_{REF}, being related to the 2-wire transverse DC voltage, and V_{LBIAS} approximately half V_{REF}.

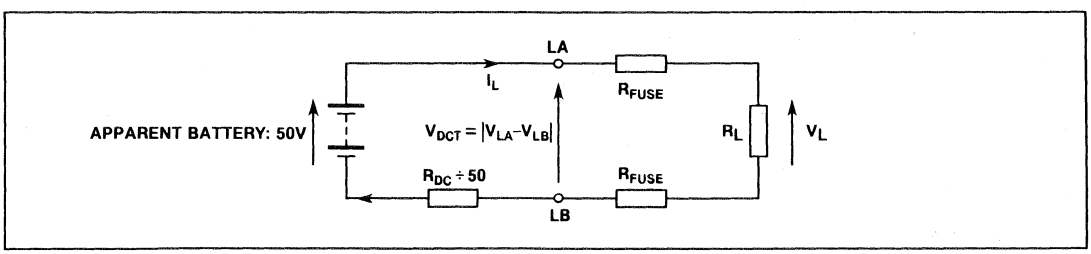


Fig. 5a Simple power feed model (normal line feed)

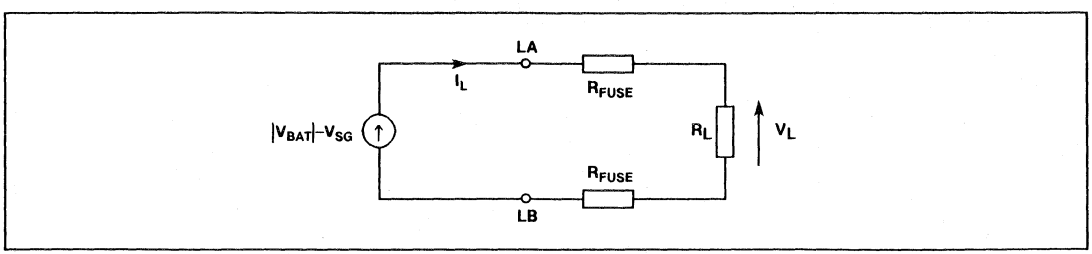


Fig. 5b Simple power feed model (saturation guard active)

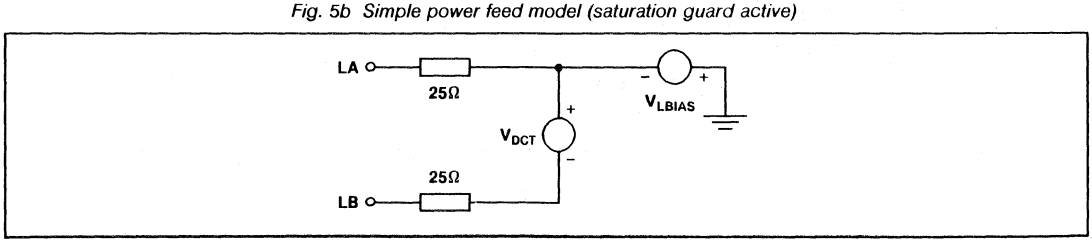


Fig. 5c Longitudinal bias circuit.

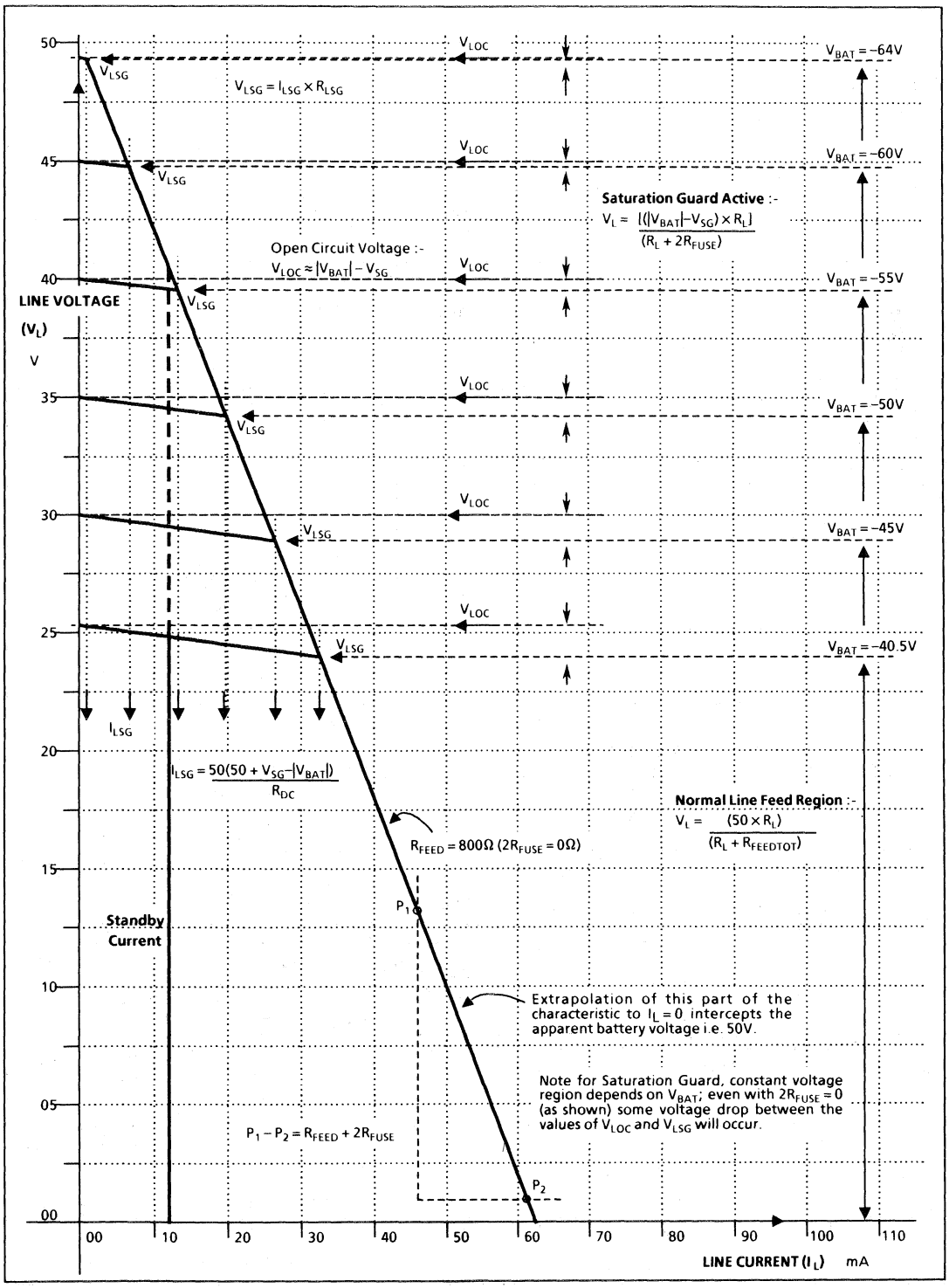


Fig. 6a Line feed characteristic, V_L vs I_L.

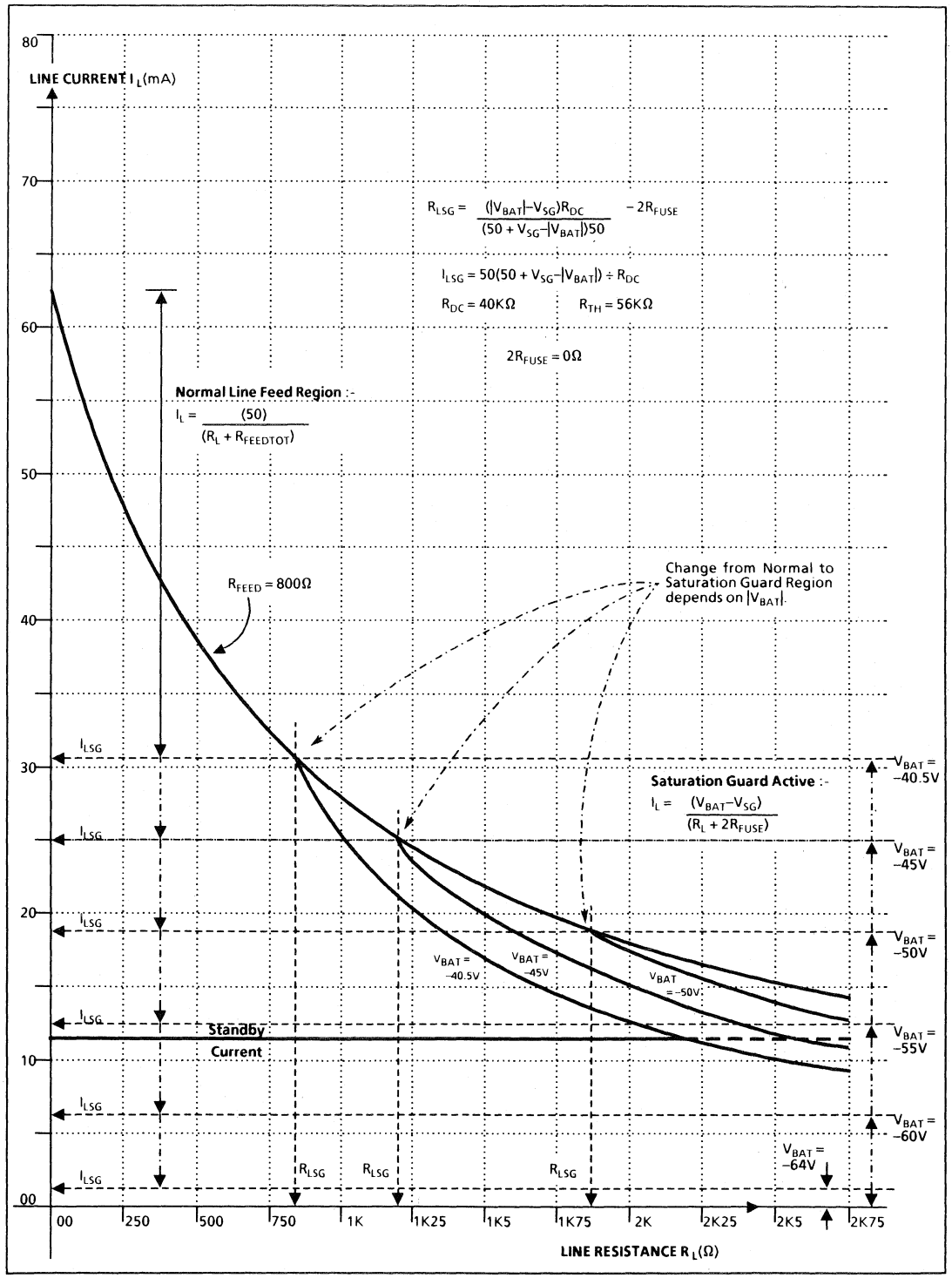


Fig. 6b : Line Feed Characteristic, I_L vs R_L.

V_{REF} controls the line feed regulator and V_{LBIAS} sets the 2-wire feed balance voltage (centre point voltage of the lines). The longitudinal control loop achieves an input impedance of approximately 25Ω per line for longitudinal signals, as shown in Fig. 5c.

LINE FEED REGULATOR

The DC voltage between LA and LB will vary with the DC loop resistance. Unless the voltage supplied to the chip can be varied to match that on the line there will be a voltage drop across the chip along the path taken by the feed current. This could cause significant power dissipation. The purpose of the line feed regulator is to minimise this power dissipation by regulating the voltage supplied to the line amplifiers.

Regulated voltage is supplied to the line amplifiers on V_{REG} and unregulated voltage is supplied on V_{BB}. The chip switches V_{BB} onto +CH when more power is required at the V_{REG} pin. V_{REG} is the voltage used by the device to power the 2-wire interface, and it is adjusted to follow a reference voltage V_{REF} (from Power Feed). This reference voltage is determined as follows:

$$V_{REF} = -\{ | V_{DCT} | + V_{BIAS} \}$$

and as such will set V_{REG} to the minimum required to power the line interface, thus minimising power dissipation. The voltage V_{BIAS} is needed to keep the amplifier response linear when audio signals are transmitted.

Fig. 7 shows the external components associated with the power supply aspect of the voltage regulator. +CH is the positive terminal of the regulator switch that connects to V_{BB}.

When the switch is turned on, current in L_1 and C_1 increases, thus increasing stored energy. When the switch turns off, this stored energy sustains L_1 current which flows in D_1. The voltage at +CH is thus a square wave of up to 50V p-p making this node sensitive to PCB layout. Note that the inductor should be capable of taking twice the line current without saturating. The regulator will work with a wide range of inductor resistance, although if this is too large, long line drive capability and regulator efficiency will be reduced. Since there are large current fluctuations from V_{BB} through the switch, C_2 provides filtering of the VBB pin, whilst D_2 isolates the V_{BAT} supply should the LA/LB pins be taken negative of the V_{BAT} supply.

The chip senses the voltage at V_{REG}, compares it to its requirements and switches power from V_{BB} to +CH, using the variable mark/space method, to give appropriate matching. The rate of switching can be governed by CHCLK or allowed to free run, its stability ensured by the network on CHS, i.e. C_3, R_1, C_5. Since noise is produced by the switching, a decoupling node is provided at SUB.

CONTROL AND SIGNALLING

The mode of operation of the SL7950 is determined by the digital interface pins, as described in Tables 1 and 2. These pins enable ringing or non-ringing modes of operation, controlling line status, line polarity, relay driver and selection of line detector.

The line status is selected by use of the D2..D0 pins, Table 2, to determine the modes as listed. The function of these modes has already been described in the 'Overview' and 'DC Line Feed' sections; more detail of the device detectors is given on the following page (refer to Fig. 8).

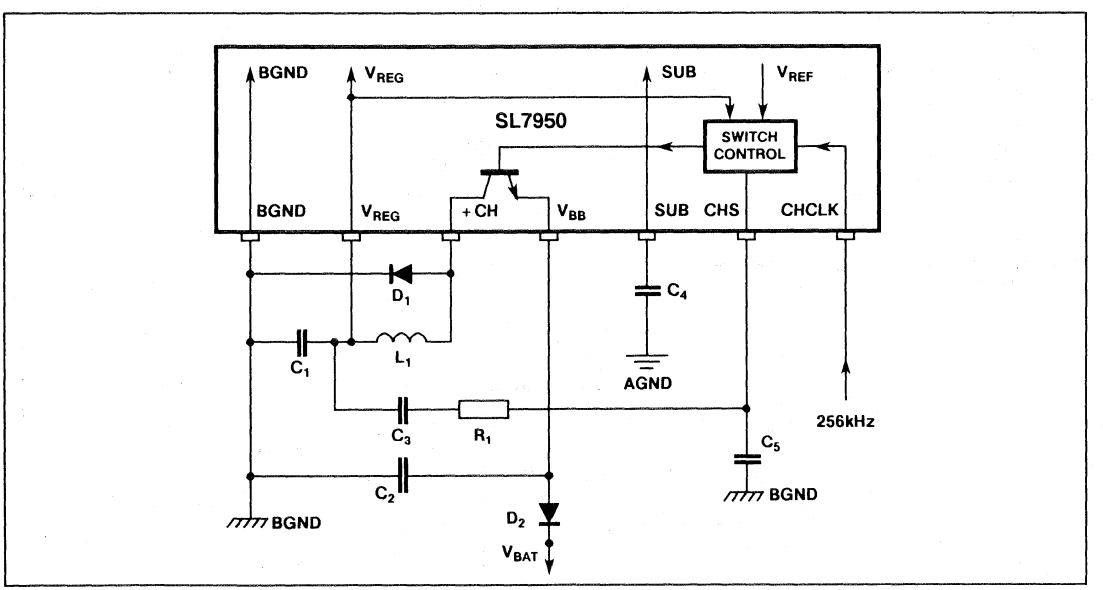


Fig.7 Voltage regulator power supply circuit.

Loop Detect

This detector is used in Active and Standby modes (with/without polarity reversal). The loop current at which the detector indicates the Off-Hook condition, is set by the comparator at pins 24 (RD) and 20 (V_{EE}). Normally a resistor, R_{TH}, is connected between these pins, such that Off-Hook line current threshold (I_{DET}) is set by:

$$I_{DET} = 350 \div R_{TH}$$

This is due to the fact that the current out of the RD pin is equal to the loop current $I_L = (\frac{1}{2}|I_A - I_B|)$ divided by ~280. This will create a voltage across R_{TH} at the RD pin. Off-Hook is given by a logic low at the $\overline{DET}$ output pin (when detector is selected) when this voltage rises above the internal 1.25V reference.

Ground Key Detector

This is facilitated by provision of the Disconnect A Standby B mode of the SLIC. In this mode, only a ground connection to the B line (LB) is detected via the $\overline{DET}$ output.

Ring Trip Detector

This consists of a comparator connected to the DA and DB pins, and indicates Ring Trip when the voltage at DA < DB. Selection of Ringing mode operates the Ring Relay and enables the Ring Trip Detector. The external ringing supply must consist of DC line feed in addition to the AC ringing voltage. In order that the Ring Trip Detector senses Ring Trip in ringing mode, a resistance bridge network is used in association with pins DA, DB, line and ring source. This network is described in the Applications section and discussed further in AN82 (the SL7950 contains the same detector circuit for Ring Trip as the SL373/SL376 SLICs).

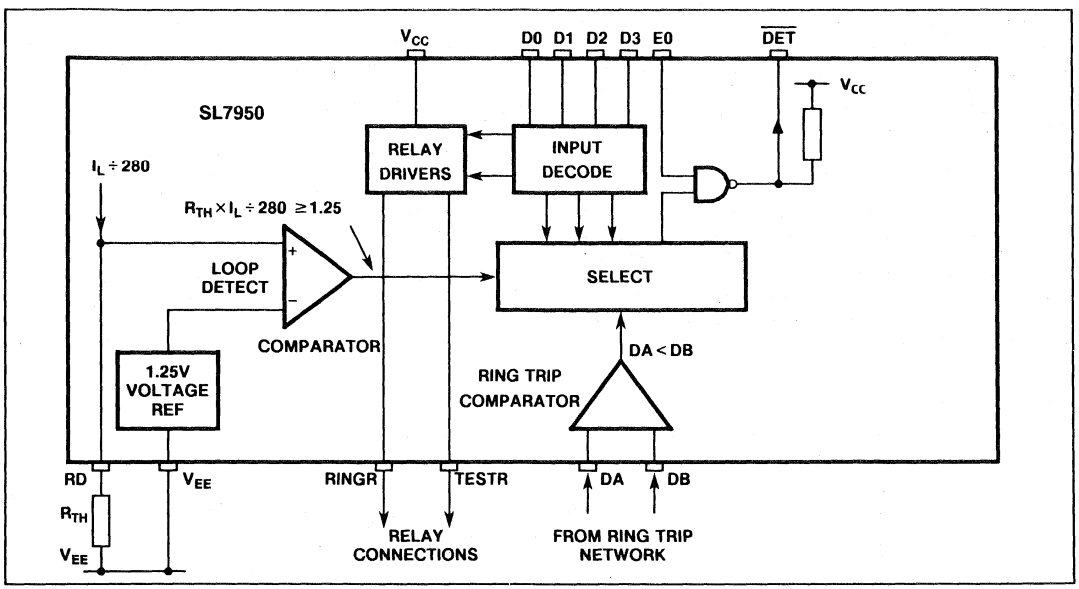


Fig.8 Detector circuits.

FUNCTIONAL PARAMETER SUMMARY

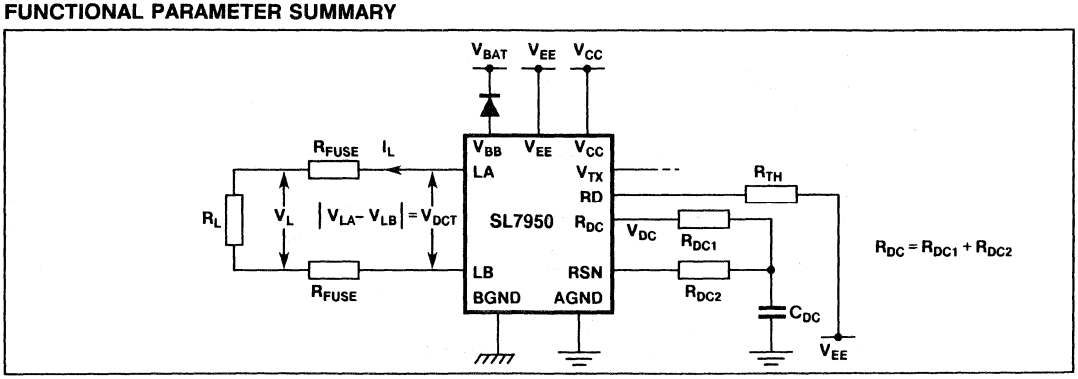


Fig.9 DC parameters and components for the SL7950

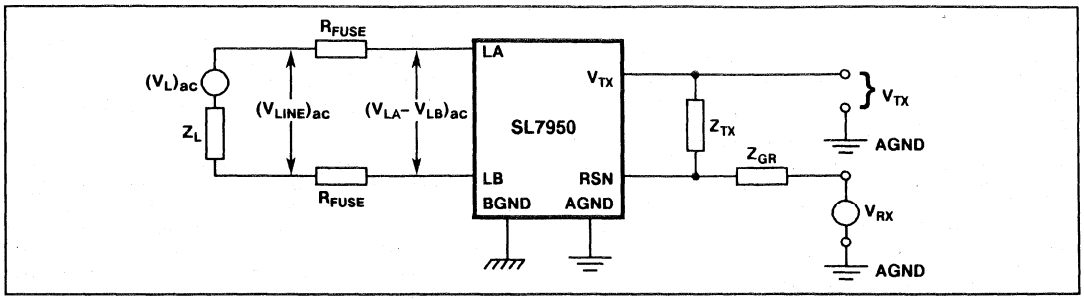


Fig.10 AC parameters and components for the SL7950

LIST OF DEFINITIONS

1. Loop Current is defined as :- $I_L = \pm\frac{1}{2}|I_A - I_B|$
   I_A = current out of LA pin, I_B = current out of LB pin, $+\Rightarrow$ normal line polarity and $-\Rightarrow$ reverse line polarity.
2. Normal Line Feed Region when $|V_{BAT}|-|V_{DCT}| > V_{SG}$ which gives :-
   $I_L = I_{FEED} = 50 \div (R_L + R_{FEEDTOT})$ where $R_{FEEDTOT} = 2R_{FUSE} + (R_{DC} \div 50)$
3. Saturation Guard Threshold when $|V_{BAT}|-|V_{DCT}| = V_{SG} = 15.0V$ such that :-
   $I_L = I_{LSG} = 50(50 + V_{SG}-|V_{BAT}|) \div (R_{DC})$
   and $R_{LSG} = \frac{[(|V_{BAT}|-V_{SG}) \times (R_{DC})] - [2R_{FUSE}]}{(50 + V_{SG}-|V_{BAT}|)50}$ $V_{LSG} = I_{LSG} \times R_{LSG}$ which will equal $|V_{BAT}|-V_{SG}$ with $2R_{FUSE} = 0$
4. Saturation Guard feed Region when $|V_{BAT}|-|V_{DCT}| < V_{SG}$ with $I_L = [|V_{BAT}|-V_{SG}] \div [R_L + 2R_{FUSE}]$
5. Note that V_{LSG} is referred to as the value of the line voltage, V_L, at the point where Saturation Guard becomes active. This will differ from the value of $|V_{LA}-V_{LB}|$ (i.e. V_{DCT}) if $2R_{FUSE} \neq 0$. V_{SG} is used as a notional threshold voltage which is the internal headroom between the $|V_{LA}-V_{LB}|$ voltage and the battery supply, at this same point.
6. Open Circuit Line Voltage V_{LOC} at $R_L = \infty\Omega$ such that :- $V_L = V_{LOC} \approx [|V_{BAT}|-V_{SG}]$
   V_{LOC} will be $\geq V_{LSG}$ even with $2R_{FUSE} = 0$. The voltage drop from V_{LOC} to the defined V_{LSG} point will be greater at lower values of V_{BAT}.
7. Standby Mode DC Feed Current $I_L \leq I_{LIM} = K_{LIM} \times I_{DET} \approx 600 \div R_{TH}$
8. 2 Wire Termination Impedance $Z_{AB} = (Z_{TX} \div \alpha) = (Z_{TX} \div 1000)$
   Note that Z_{TX} is normally set to $[\alpha(Z_L + 2R_{FUSE})]$ where Z_L is the desired termination impedance.
9. Recieve Gain from V_{RX} to $(V_{LA}-V_{LB})_{ac}$ or $(V_{LINE})_{ac}$ is set by Z_{GR} after setting Z_{TX}. Thus, with $(V_L)_{ac} = 0$:-
   $\frac{(V_{LA}-V_{LB})_{ac}}{V_{RX}} = \frac{-\alpha Z_L Z_{TX}}{[\alpha(Z_L) + Z_{TX}]Z_{GR}}$ with $2R_{FUSE} = 0$; $\frac{(V_{LINE})_{ac}}{V_{RX}} = \frac{-\alpha Z_L Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]Z_{GR}}$ with $2R_{FUSE} \neq 0$
10. Resultant Transmit Gain is then :- $\frac{V_{TX}}{(V_L)_{ac}} = \frac{Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]}$ with $V_{RX} = 0$
11. Resultant 4 Wire-4 Wire Gain is then :- $\frac{V_{TX}}{V_{RX}} = \frac{-\alpha(Z_L + 2R_{FUSE})Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]Z_{GR}}$ with $(V_L)_{ac} = 0$
12. Off-Hook Threshold is set by R_{TH} at :- $I_L = I_{DET} = 350 \div R_{TH}$
13. Ring Trip Threshold is set by the bridge associated with pins 25 .. 28 and the 2-Wire Line, thus :-
    $R_L = R_{LTH} = R_{B4}(2R_F) \div (R_{B4}-R_{B1})$ assuming $R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$ and $R_{FEED1} = R_{FEED2}$ for the bridge components (balanced ringing). $R_{B1}..R_{B4} \approx$ a few 100kΩ and $R_{FEED1} \approx$ a few 100Ω.
14. AC ringing voltage at DA (DB by the same amount) is reduced by a factor of :- $[1 + (2\pi f_r t_r)^2]^{-\frac{1}{2}}$
    f_r is the ringing frequency and t_r is determined by the bridge components including C_B, thus :- $t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$ for Balanced Ringing.

APPLICATIONS

The requirements for the subscriber line interface vary considerably from one telephone administration to another. The SL7950 is designed to have the flexibility to meet these varying requirements. For simplicity, only a single example is given to illustrate how the device is connected. Fig. 11 shows the circuit which can be used to evaluate the device. Further Applications information, as given in SL373/SL376 Application Note AN82, is valid for the SL7950 as indicated at relevant points in this section of the data sheet.

The DA and DB pins are connected to a resistance bridge network (R_{B1} to R_{B4}). This allows the change in line resistance to be sensed when the remote telephone goes off-hook during ringing (ring trip). The details of this network (and C_B) are given later (see Ring Trip section). The resistors R_{FEED1} and R_{FEED2} provide feeding of the ringing source onto the line during ringing mode. The Ring and Test Relay coils are connected through current limiting resistors.

Connections to the LA and LB pins are shown, and include the resistors R_{FUSE} in addition to the ring relay. These resistors have a value around 20 to 30 ohms, depending on the application, and provide current line protection.

Overvoltage and protection circuitry may consist of slew-limiting inductors between the pins and the line itself and a thyristor or Zener protection network at the line. In many applications, especially in PBXs, the amount of protection circuitry can be reduced. The capacitors between LA, LB and ground, allow noise from the regulator to be decoupled.

The capacitor C_{HP} between HPA and HPB is used to filter out the AC component of the signal on the line. The voltage difference between the two pins should be effectively DC. Application Note AN82 contains a further discussion on this component.

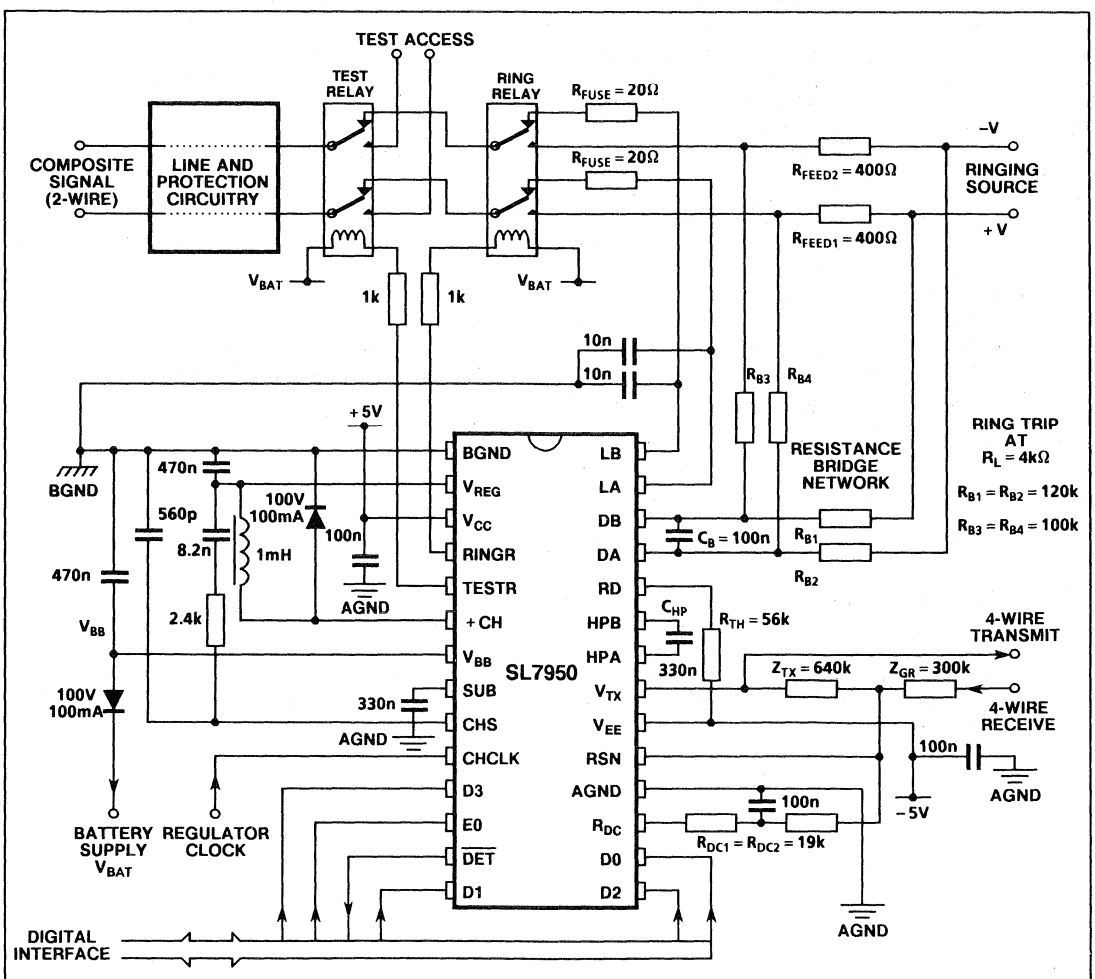


Fig. 11 Application circuit

The resistor, R_{TH}, between RD and V_{EE} programs the threshold current for the loop detector. A capacitor in parallel can be added to reduce the effect of the AC component of the line current, but this can cause instability on standby operation with highly inductive lines if it is too large. The value of R_{TH} sets the current I_{DET} according to the relationship:-

$$I_{DET} = 350 \div R_{TH}$$

CHS is connected to BGND through a capacitor and to V_{REG} by a capacitor and resistor in series. This stabilises the regulator control loop.

It is recommended that the substrate (SUB) is decoupled to AGND. However, BGND may be used if this is sufficiently quiet, else some degradation in noise performance may be experienced. The on-chip decoupling resistor between pins V_{BB} and SUB is approximately 140Ω.

DC current flows between R_{DC} and RSN. This is used to set the line feed current. Any minor AC fluctuations are reduced by dividing the resistance R_{DC} equally such that $R_{DC1} = R_{DC2} = \frac{1}{2}R_{DC}$ and connecting a capacitor from the junction of R_{DC1} and R_{DC2} to AGND.

The network (Z_{TX}) between V_{TX} and RSN controls the AC terminating impedance. The value of Z_{TX} can be calculated from the relationship :-

$$Z_{TX} = (\text{Required } Z_T) \times (\text{Receive current gain})$$

The receive gain is set by the network (Z_{GR}) which controls the receive current flowing into RSN. This can be a complex impedance network to allow for complex impedance terminations. More details of these gain settings are given in AN82.

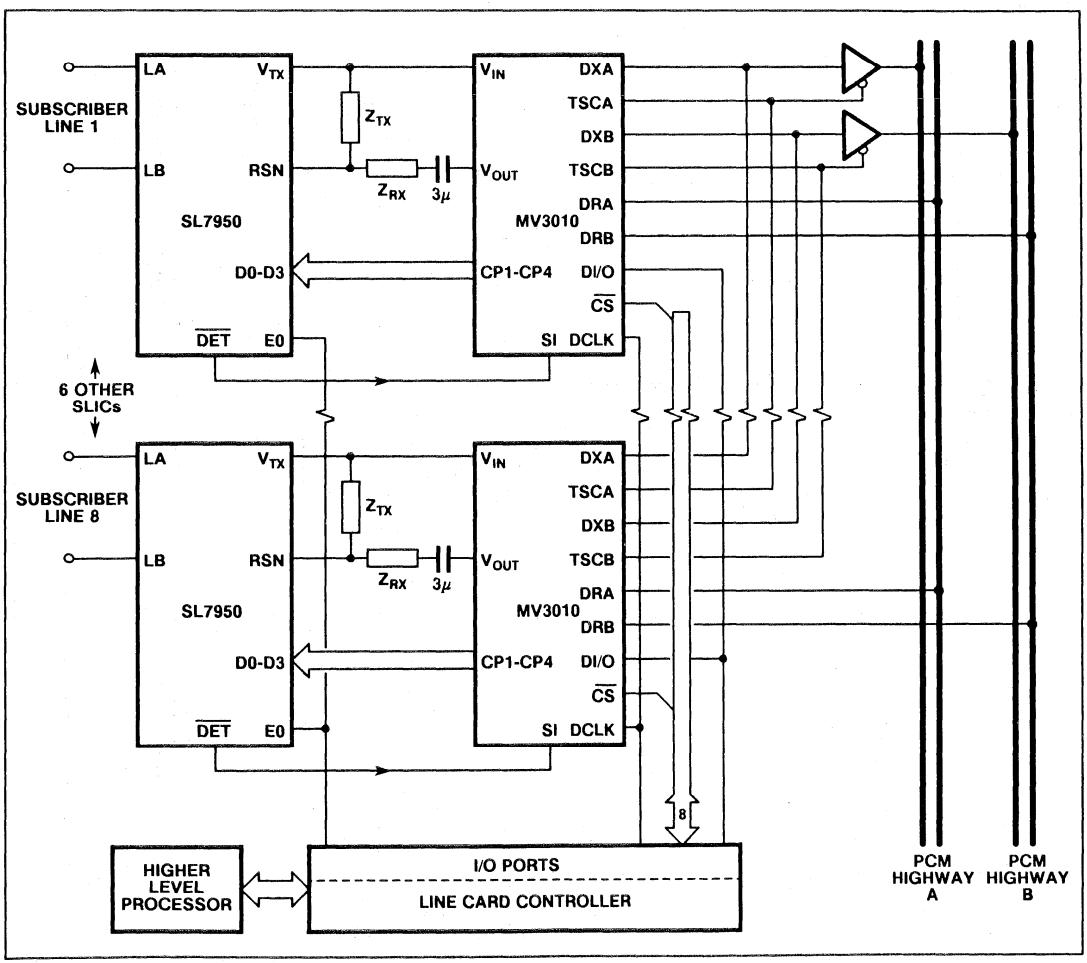


Fig.12a SLIC/PSLAC line interface card

Both the control and status pins are TTL compatible. They are designed to give a simple interface to digital circuits and are directly compatible with the GEC Plessey Semiconductors' MV3010 PSLAC (Plessey Subscriber Line Audio Circuit - see separate data).

The circuits of Fig. 12a and 12b show different ways of connecting the SLIC to the MV3010 to form an 8-channel subscriber line card architecture. For Fig. 12a, each PSLAC is controlled via a serial interface consisting of the common DI/O line, DCLK line and one of 8 $\overline{CS}$ lines. The PSLAC accepts/inputs data when the line card controller pulls the associated $\overline{CS}$ pin low and toggles DCLK (may be continuous). One of the control instructions of the PSLAC sets its CP1-CP5 I/O latches to outputs, whilst a further code writes data to each output. Four of these lines (CP1-CP4) are used to control the SLIC status (CP5 is not used). In addition to the output of data via CP1-CP4, a PSLAC control code monitors the status of the dedicated SI input.

Consequently the line card controller gains access to the SLIC $\overline{DET}$ status via the PSLAC. Action to control the SLIC is then taken accordingly by the higher level processor that is controlling the line card.

Fig. 12b shows an optional interconnect to the SLIC, making use of the E0 control input. When this input is high, all 8 $\overline{DET}$ outputs can be read simultaneously, and the higher level software can then write to the necessary PSLAC associated with each low of the 8-bit port. This writing of data can be done simultaneously to those PSLACs required, by toggling DCLK and DI/O together with the selected $\overline{CS}$ inputs. Note that E0 must be set low to disable the $\overline{DET}$ outputs during this action, thus avoiding contention on this '$\overline{DET}$ bus'.

More data on the PSLAC device, interface circuitry and controller, can be found by reference to the MV3010 data and to Application Notes AN42, AN84, AN101, AN103, AN104 and AN111.

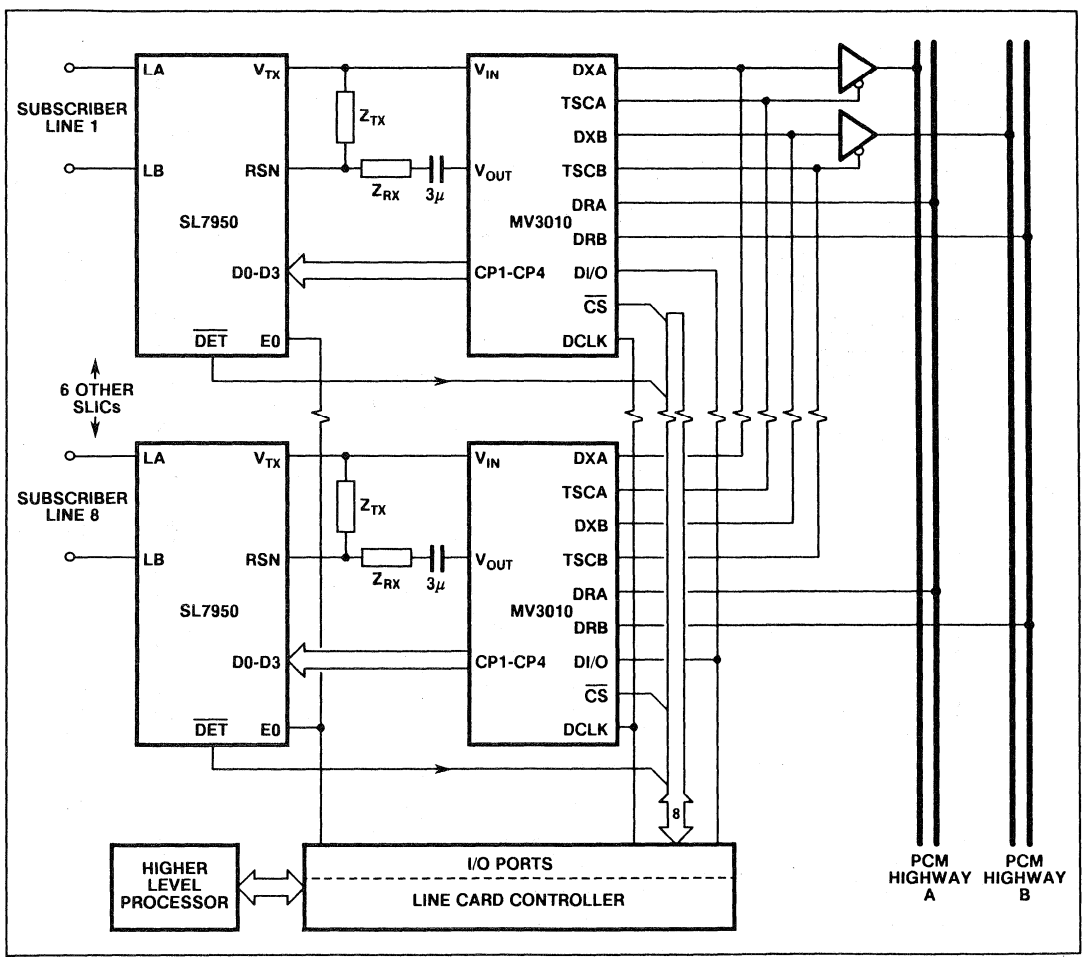


Fig.12b AlternativeSLIC/PSLAC line interface card

RING TRIP

Ring Trip detection operates by comparing the voltages on DA and DB and providing the output on $\overline{DET}$ when this function is enabled using the status input pins of the Digital Interface. A resistance bridge (R_{B1} to R_{B4}) must be connected to the line and to the ringing voltage sources to cause the differential voltage between DA and DB to change sign when the line resistance falls below the level associated with Ring Trip. Note that it is simplified by use of $R_{B1} = R_{B2}$ and $R_{B3} = R_{B4}$ (see discussion in AN82).

Ringing voltage is normally applied to the line through the ring relay which is activated via RINGR in Ringing Mode. The ringing voltage sources, including line feed, are connected via ringing feed resistors, R_{FEED1} and R_{FEED2}. The resistance bridge operates by allowing the DC voltage dropped across the ringing feed resistors in the Off-Hook condition to reverse the polarity of the voltage on DA and DB (DA < DB). Since the AC ringing voltage is greater than the DC feed, the capacitor C_B (Fig. 13) will filter this out at the comparator inputs. The connection shown is suitable for balanced ringing only. For unbalanced ringing, separate capacitors from DA (C_{B1}) and DB (C_{B2}) to ground will be required to achieve the same result.

Fig. 13 shows how the resistance bridge is connected when used with balanced ringing. The circuit can operate correctly provided there is a DC feed in addition to the AC ringing voltage.

If R_{LTH} is the line resistance corresponding to the Ring Trip threshold (DA = DB), this can be determined from the values of R_F ($R_{FEED1} = R_{FEED2} = R_F$), R_{B1} and R_{B4} ($R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$) as:-

$$R_{LTH} = \frac{R_{B4}(2\ R_F)}{(R_{B1} - R_{B4})}$$

R_{B1} and R_{B4} should be a few hundred kΩ.

The amplitude of the AC ringing voltage at DA (DB is by the same amount) is reduced by a factor of $(1 + 4\pi^2 f_r^2 t_r^2)^{-\frac{1}{2}}$ where f_r is the ringing AC frequency and t_r is set by:-

$$t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$$

for balanced ringing. For $f_r \approx 20$Hz, t_r should be ≈ 50ms. For unbalanced ringing C_B will become $C_{B1}C_{B2} \div (C_{B1} + C_{B2})$ in the above equation.

The circuit for balanced ringing is analysed in more detail in the SL373/SL376 Applications Note AN82, along with that for unbalanced operation. This information is also valid for the SL7950, since the Ring Trip Detection circuitry is the same for all devices.

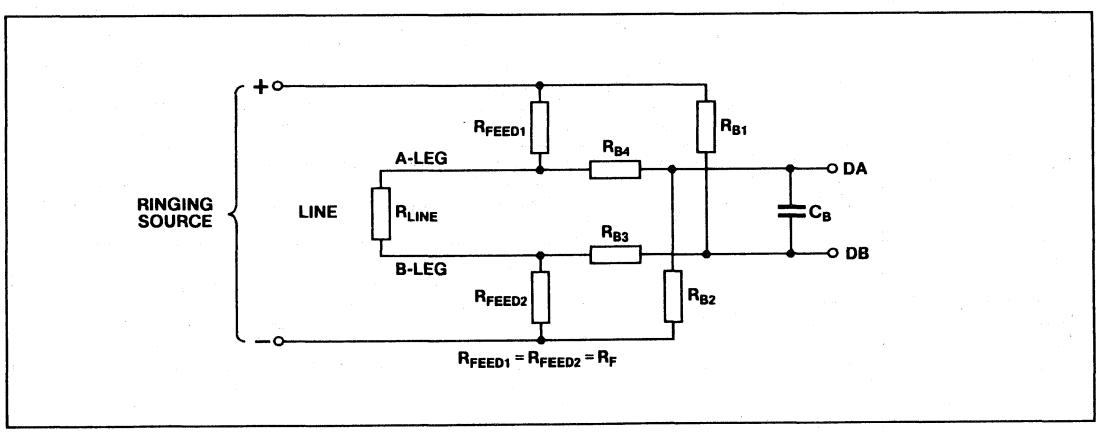


Fig. 13 Ring trip circuit

PIN DESCRIPTIONS

Symbol †	Pin no.*	Pin name and description
BGND [BGND]	1 (1)	**Battery Ground (Power Input).** 0 Volts.
V_{REG} [V_{REG}]	2 (2)	**Regulated Voltage (Negative Power Input).** The voltage at this pin is compared to that required for line feed, and the result is used to control the voltage regulator.
V_{CC} [V_{CC}]	3 (3)	**Positive Supply (Power Input).** +5 Volts.
NC	- (4)	**(No Connection)**
RINGR [RINGOUT]	4 (5)	**Ring Relay Driver Output, Transistor Emitter.** This output is designed to drive a relay, when used together with the V_{BAT} supply. The driver collector connects to the V_{CC} pin.
TESTR [TESTOUT]	5 (6)	**Test Relay Driver Output, Transistor Emitter.** This output is designed to drive a relay, when used together with the V_{BAT} supply. The driver collector connects to the V_{CC} pin.
+ CH [L]	6 (7)	**Switching Regulator (Chopper) Output (Negative Power Output).** Chopper switch transistor collector. An internal regulator controls the mark/space ratio of the switching waveform to maintain V_{REG} (pin 2) at the required voltage.
V_{BB} [V_{BAT}]	7 (8)	**Battery Voltage (Negative Power Input).** This is the negative voltage battery supply pin which connects to the V_{BAT} supply via an external diode. It is connected to the chopper switch emitter, and via an on-chip resistor to SUB.
SUB [Q_{BAT}]	8 (9)	**Quiet Battery, Substrate (Decoupling Node).** An external decoupling capacitor (0.33µF) should be connected between this pin and AGND. An internal resistor connects to the V_{BB} pin.
CHS [CHS]	9 (10)	**Line Feed Regulator (Chopper) Stabilising Network.** This is the input to the voltage comparator which is used to control the switching regulator.
CHCLK [CHCLK]	10 (11)	**Line Feed Regulator (Chopper) Clock (Digital Input).** This is the external clock input for the voltage regulator. The frequency is 256kHz (nominal), triggered on the rising edge. The regulator will free run in the absence of an input signal.
D3 [C_4]	11 (12)	**Control Input (Digital Input).** Enables the Test Relay Driver output pin.
E0 [E_0]	12 (13)	**Detector Data output Enable (Digital Input).** Enables the Detector data output pin ($\overline{DET}$).
$\overline{DET}$ [$\overline{DET}$]	13 (14)	**Detector Data output (Digital Output).** This pin outputs the status of the detector which has been selected by D0 - D2. It is enabled by the E0 pin.
D1 [C_2] D2 [C_3] D0 [C_1]	14 (15) 15 (16) 16 (17)	**Control Input (Digital Input).** **Control Input (Digital Input).** **Control Input (Digital Input).** These inputs determine the SLIC operating mode, and control the ring relay status, selection of ringing and non-ringing Modes, line polarity, line status and line detector.
NC	- (18)	**(No Connection)**
R_{DC} [R_{DC}]	17 (19)	**DC Reference Voltage (Voltage Output).** A reference voltage which is equal to ±(50–|V_{LA}–V_{LB}|)÷20 Volts (±depending on line polarity), is output at this pin, excepting Saturation Guard region.
AGND [AGND]	18 (20)	**Analog Ground (Analog Reference Node).** This is the ground reference pin for the analog signals. It also provides a ground reference for the Digital Interface. Signal reference and decoupling connections should be separately run to this pin.
RSN [RSN]	19 (21)	**Receive Summing Node (Current Input).** The current which is input on this pin is used to control the transverse current at LA and LB.
V_{EE} [V_{EE}]	20 (22)	**Negative Supply (Power Input).** – 5 Volts.

† Pin names for the Am7950 are shown thus : [XXX]; note that the functionallity is identical.
* Pin numbers in parentheses are for the LC32 package only.

PIN DESCRIPTIONS

Symbol †	Pin no.*	Pin name and description
VTX [V_{TX}]	21 (23)	**Transmit Voltage (Voltage Output).** The voltage output at this pin is equal to the difference between the voltage (V_{LA}–V_{LB}) and the differential DC voltage (V_{HPA}–V_{HPB}), multiplied by the 2 to 4-wire voltage gain.
NC	- (24)	**(No Connection)**
HPA [HPA] HPB [HPB]	22 (25) 23 (26)	**High Pass A, High Pass B - AC/DC separation (Voltage Inputs).** These inputs sense the DC feed voltages on the LA and LB pins respectively. Under normal operation they are connected to LA and LB respectively by internal resistors and should be connected as shown in Fig. 11.
RD [R_D]	24 (27)	**Loop Detection Control (Current Output / Voltage Input).** This pin outputs a current which equals the transverse loop current through LA and LB divided by 280. Off-Hook is indicated via the $\overline{DET}$ pin when the voltage at this pin is $\geq (V_{EE} + 1.25)$ Volts.
DA [DA] DB [DB]	25 (28) 26 (29)	**Ring Trip Detector A, Ring Trip Detector B (Voltage Inputs).** These are the A and B inputs to the internal ring trip comparator. The output of the comparator controls the ring trip output on $\overline{DET}$.
LA [AX(TIPX)] LB [BX(RINGX)]	27 (30) 28 (31)	**A Line Transceiver, B Line Transceiver (Current Outputs / Voltage Inputs).** These two pins form the 2-wire port connecting to the subscriber loop.
NC	- (32)	**(No Connection)**

† Pin names for the Am7950 are shown thus : [XXX]; note that the functionallity is identical.
* Pin numbers in parentheses are for the LC32 package only.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Range - see page 3-99)

Test conditions (unless otherwise stated)

V_{CC} = +5.0V, V_{EE} = -5.0V, V_{BAT} = -50V (see note 4), $V_{AGND} = V_{BGND}$, T_{AMB} = +25°C, $V_{AGND} = V_{BGND}$, V_{IL} = 0.7V and V_{IH} = 2.0V. Test circuit Fig. 25. Voltages are measured with respect to analog ground (V_{AGND}). Typical figures are for design aid only; they are not guaranteed and are not subject to production testing.

Supply Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply (V_{CC}) current, disconnect mode	I_{CC1}			4	mA	
Positive supply (V_{CC}) current, standby mode	I_{CC2}			10	mA	On / Off-Hook, I_L = 0
Positive supply (V_{CC}) current, active mode	I_{CC3}			10	mA	On / Off-Hook, I_L = 0
Negative supply (V_{EE}) current, disconnect mode	I_{EE1}			2	mA	
Negative supply (V_{EE}) current standby mode	I_{EE2}			3	mA	On / Off-Hook, I_L = 0
Negative supply (V_{EE}) current active mode	I_{EE3}			3	mA	On / Off-Hook, I_L = 0
Battery supply (V_{BB}) current disconnect mode	I_{BB1}			1	mA	
Battery supply (V_{BB}) current standby mode	I_{BB2}			5	mA	On-Hook, I_L = 0
Battery supply (V_{BB}) current active mode	I_{BB3}			6	mA	On-Hook, I_L = 0
Positive supply (V_{CC}) rejection ratio (low frequency), supply to 2-wire longitudinal/transverse	P_{SRL}	12			dB	15mV on V_{CC} supply, 50-5000Hz, $Z_L \leq 600\Omega$, see notes 1 and 2
Positive supply (V_{CC}) rejection ratio (high frequency), supply to 2-wire longitudinal/transverse	P_{SRH}	12			dB	15mV on V_{CC} supply, 5kHz-50kHz, $Z_L \leq 600\Omega$, see notes 1 and 3
Negative supply (V_{EE}) rejection ratio (low frequency), supply to 2-wire longitudinal/transverse	N_{SRL}	17			dB	15mV on V_{EE} supply, 50-5000Hz, $Z_L \leq 600\Omega$, see notes 1 and 2
Negative supply (V_{EE}) rejection ratio (high frequency), supply to 2-wire longitudinal/transverse	N_{SRH}	7			dB	15mV on V_{EE} supply, 5kHz-50kHz, $Z_L \leq 600\Omega$, see notes 1 and 3
Battery supply (V_{BB}) rejection ratio (low frequency), supply to 2-wire longitudinal/transverse	B_{SRL}	27			dB	15mV on V_{BAT} supply, 50-5000Hz, $Z_L \leq 600\Omega$, see notes 1 and 2
Battery supply (V_{BB}) rejection ratio (high frequency), supply to 2-wire longitudinal/transverse	B_{SRH}	12			dB	15mV on V_{BAT} supply, 5kHz-50kHz, $Z_L \leq 600\Omega$, see notes 1 and 3
Power dissipation, active state	P_{WA1}		0.7	1.0	W	$Z_L = 600\Omega$, V_{BAT} = -60V
Power dissipation, active state	P_{WA2}		0.3	0.425	W	$Z_L = \infty$, V_{BAT} = -60V
Power dissipation, standby state	P_{WD1}		0.18	0.3	W	On-Hook
Power dissipation, disconnect A standby B	P_{WD2}		0.05	0.14	W	See note 3

NOTES

1. This parameter will degrade when the saturation guard is active i.e. $|V_{BAT}|-|V_{DCT}| < 15.0V$ (i.e. V_{SG}).
2. Tested at 1kHz in productrion. Performance at other frequencies guaranteed by characterisation.
3. Not tested in production. Figures are guaranteed by characterisation.
4. Battery voltage V_{BAT} is generally defined. The corresponding V_{BB} voltage is assumed to be 0.7V more positive than V_{BAT} allowing for the diode drop in D_2, Fig. 25.

Analog Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
2-wire port, low freq overload level	V_{OAB}	– 3.1		+ 3.1	V (pk)	See Fig 14, note 5: E_R = 1000Hz, E_L = 0V, R1 = 600Ω, R4 = 0Ω
2-wire port, longitudinal impedance, off hook	Z_{LL1}		25	35	Ω/wire	See Fig 15: f < 100Hz Z_L = 600Ω
2-wire port, longitudinal impedance, on hook	Z_{LL2}		25	35	Ω/wire	See Fig 16: f < 100Hz Z_L = 600Ω
2-wire port, 2-wire return loss	RTL_2	35 25 20	38 28 22		dB dB dB	300-500Hz 500-2500Hz 2.5-3.4kHz See Fig 14, notes 3 & 6: E_L = 0dBu, E_R = 0V, R1 = R4 = 300Ω
Longitudinal current limit, active state	ILL_A	17.5	25		mA/wire (rms)	See Fig 17, note 7: Z_L = 600Ω, E_R = – 10dBm 700-1100Hz
Longitudinal current limit, standby state	ILL_S	3.6	12		mA/wire (rms)	See Fig 17, note 7: Z_L = 600Ω E_R = – 10dBm 700-1100Hz
4-wire transmit port, overload level	V_{OT}	– 3.1		+ 3.1	V (pk)	See Fig 14, note 5: f = 1kHz 4-Wire Load ≥ 25kΩ, E_R = 0V, R1 = 600Ω, R4 = 0Ω
4-wire transmit port, offset voltage	V_{TOFF}		± 10	± 35	mV	See Fig 14: E_R = 0V, E_L = 0V, R1 = 600Ω, R4 = 0Ω
4-wire transmit port,output impedance	Z_{TO}		1	20	Ω	See Fig 14: E_R = 0V, E_L = 0V, R1 = 600Ω, R4 = 0Ω
Transmit (2 to 4-wire) voltage gain	G_T	– 0.15		+ 0.15	dB	See Fig 14: E_R = 0V, E_L = 0dBu 1kHz, R1 = 600Ω, R4 = 0Ω
4-wire receive port, low impedance virtual earth input	Z_{RI}			20	Ω	Note 3
4-wire receive port, low frequency voltage gain	G_{R4}	– 0.15		+ 0.15	dB	See Fig 18: E_R = 2.6dBu 1kHz
4-wire receive port, current gain	G_{RI4}	59.8	60.0	60.2	dB	See Fig 14: R1 = 600Ω, R4 = 0Ω
4 to 4-wire voltage gain	$G_R \times G_T$	– 0.15		+ 0.15	dB	See Fig 14, note 3: E_L = 0V, R1 = 600Ω, R4 = 0Ω
2-wire to 4-wire frequency response	F_{24}	– 0.1		+ 0.1	dB	See Fig 14, notes 3 & 8: E_R = 0V, E_L = 0dBu 200-3400 Hz, R1 = 600Ω, R4 = 0Ω
4-wire to 2-wire frequency response	F_{42}	– 0.1		+ 0.1	dB	See Fig 14, notes 3 & 8: E_L = 0V, E_R = 0dBu 200-3400 Hz, R1 = 600Ω, R4 = 0Ω
4 to 4-wire frequency response	$F_{44} = F_{24} \times F_{42}$	– 0.1		+ 0.1	dB	Note 8
Gain linearity, 2-wire to 4-wire	G_{L24}	– 0.1		+ 0.1	dB	See Fig 14, notes 3 & 9: R1 = 600Ω, E_R = 0V, R4 = 0Ω, E_L = + 7 to –55dBu 1kHz
Gain linearity, 4-wire to 2-wire	G_{L42}	– 0.1		+ 0.1	dB	See Fig 14, notes 3 & 9: R1 = 600Ω, R4 = 0Ω, E_L = 0V, E_R = + 7 to –55dBu 1kHz
Gain linearity, 4-wire to 4-wire	G_{L44}	– 0.1		+ 0.1	dB	See Fig 14, notes 3 & 9: R1 = 600Ω, R4 = 0Ω, E_L = 0V, E_R = + 3 to –45dBu 1kHz

NOTES
5. Overload occurs when distortion is 1% of total signal in the range 300-3400Hz.
6. dBu is defined thus : 0dBu is equivalent to the voltage at 0dBm when loaded with 600Ω (= $0.775V_{RMS}$).
7. E_{LL} = 50Hz. Amplitude is increased until signal-to-distortion ratio at V_T ≤ 20dB.
8. Response is measured with respect to 1kHz.
9. Linearity is measured with respect to gain at – 4dBu.

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Group delay	D_G		5		µs	f = 1kHz, note 3
4-wire idle channel noise (psophometric weighted)	N_{P4}		– 77.0	– 75.0	dBup	See Fig. 14, note 1: $E_L = E_R = 0V$, V_{BB} = –60V, R1 = 600Ω, R4 = 0Ω
2-wire idle channel noise (psophometric weighted)	N_{P2}		– 77.0	– 75.0	dBup	See Fig. 14, note 1: $E_L = E_R = 0V$, V_{BB} = –60V, R1 = 600Ω, R4 = 0Ω
2-wire differential noise (wide band)	N_{D2}		Fig. 20			See Fig. 19, note 3
2-wire longitudinal noise (wide band)	N_{L2}		Fig. 21			See Fig. 19, note 3
Regulator noise, 4-wire transmit, single frequency	N_{R4}			– 55.0	dBu	See Fig. 19, note 3
Regulator noise, 2-wire transverse, single frequency	N_{RT}			– 50.0	dBu	See Fig. 19, note 3
Regulator noise, 2-wire longitudinal, single frequency	N_{RL}			– 50.0	dBu	See Fig. 19, note 3
Longitudinal balance, longitudinal to transverse	B_{L-T}	50	55		dB	See Fig. 15, note 1: Z_L = 600Ω, E_R = 0, E_{LL} = +2dBu 300-3400 Hz
Longitudinal balance, longitudinal to 4-wire	B_{L-4}	50	55		dB	See Fig. 15, note 1: Z_L = 600Ω, E_R = 0, E_{LL} = +2dBu 300-3400 Hz
Longitudinal balance, transverse to longitudinal	B_{T-L}	35	50		dB	See Figs. 15 & 22: Z_L = 600Ω, E_R = 0, E_{LL} = +2dBu 300-3400 Hz
Longitudinal signal rejection, longitudinal to 4-wire	RJ_{L-4}	50	60		dB	See Fig. 15: Z_L = 600Ω, E_R = 0, E_{LL} = +2dBu 300-3400 Hz
Longitudinal signal generation, 4-wire to longitudinal	GN_{4-L}	35	45		dB	See Fig. 23: Z_L = 600Ω, E_R = 2.6dBu f = 300-3400 Hz
Harmonic distortion, 4 to 2-wire	T_{HD1}		– 64 – 55	– 50 – 40	dB dB	E_R = 0dBu See Fig. 14, notes 2 & 10: E_R = 9dBu R1 = 600Ω, R4 = 0Ω
Harmonic distortion, 2 to 4-wire	T_{HD2}		– 64 – 55	– 50 – 40	dB dB	E_L = 0dBu See Fig. 14, notes 2 & 10: E_L = 9dBu R1 = 600Ω, R4 = 0Ω
Intermodulation distortion	ID_{A-B1}			– 40.0	dB	See Fig. 14, notes 3 & 11: $E_R = f_1 + f_2$, $f_1 = f_2$ = – 4 to – 21dBu, R1 = 600Ω, R4 = 0Ω
50Hz intermodulation distortion	ID_{A-B2}			– 49.0	dB	See Fig 14, notes 3 & 12: $V_R = f_1 + f_2$, f_1 = – 9dBu 300-3400 Hz, f_2 = – 23dBu 50 Hz.
Apparent battery voltage	V_{BBAP}	47 47	50 50	53 53	V V	R_{DC} = 25kΩ, Z_L = 300/600Ω R_{DC} = 80kΩ, Z_L = 600/900Ω See Fig. 25, note 13
Loop current, active state	I_{ACT1}	33.2	35.7	38.4	mA	See Fig. 25, note 14: Z_L = 600Ω
Loop current, active state	I_{ACT2}	18			mA	See Fig .25, note 14: Z_L = 1800Ω
2-wire current, disconnected state	I_{DCT}			1.0	mA	LA to LB or ground, or both LA and LB to ground

NOTES
10. Distortion measured in the bandwidth 300-3k4 Hz.
11. f_1 & f_2 in the range 300-3.4kHz, $f_1 \div f_2$ = Non-integer. Measure $(2f_1-f_2)$ relative to f_1 or f_2 level.
12. Measure $(2f_1-f_2)$ relative to f_1 or f_2 level.
13. Applied V_{BAT} = – 63V
14. Feed resistance is (40k + 50)Ω i.e. R_{DC} = 40kΩ. Nominal apparent battery = – 50V. Applied V_{BAT} = – 63V

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Loop current limit conversion factor (see DC line feed section)	K_{LIM}	1.45		1.90	-	Standby mode
Loop detector, current threshold accuracy	I_{TH}	I_{TH} –20%	I_{TH}	I_{TH} + 20%	A	See Fig. 25 : $I_{TH} = 350 \div R_{TH}$
Ring trip detector offset voltage	V_{RTO}	– 50		+ 50	mV	See Fig. 24 : $V_{BB} < V_{CMM} < -2V$
Ring trip detector bias current	I_{RTB}	– 1.0			µA	See Fig. 24 : $I_{RTB} = \frac{1}{2}(I_{RTDA} + I_{RTDB})$
Relay drivers, saturation voltage (active)	V_{SAT}	V_{CC}–2	V_{CC}–1.3		V	I = 25mA drawn from pin
Relay drivers, leakage current (non-active)	I_{LK}		0.05	0.1	mA	V_{OUT} = voltage at pin 8
Relay drivers, clamp voltage	V_{CL-}	V_{BAT}–2.0	V_{BAT}–1.3		V	I = 25mA into pin

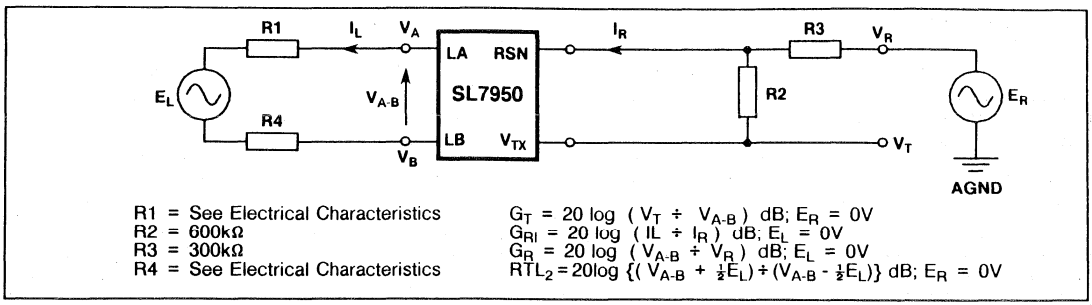
NOTES
15. Constant current in Standby mode approx. $600 \div R_{TH}$.

Digital Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Input low voltage (D0-D3, E0, CHCLK)	V_{IL}			0.8	V	
Input high voltage (D0-D3, E0, CHCLK)	V_{IH}	2.0			V	
Input low current (D0-D3, E0, CHCLK)	I_{IL}			– 0.25	mA	$V_{IL} = 0.4V$
Input high current (D0-D3, E0, CHCLK)	I_{IH}			0.04	mA	$V_{IH} = 2.4V$
$\overline{DET}$ output low voltage	V_{OL}		0.25	0.4	V	$I_{OL} = 0.8mA$
$\overline{DET}$ output high voltage	V_{OH}	2.4	4.0		V	$I_{OH} = 0.1mA$
$\overline{DET}$ output, internal pull-up	R_{OUT}	10		20	kΩ	
Loop detector make response time	t_{LM}			5	ms	$Z_L = 2k\Omega$ ($V_{OL} < 0.45V$)
Loop detector break response time	t_{LB}			10	ms	$Z_L = 2k\Omega$ ($V_{OL} > 2.35V$)
CHCLK input frequency	f_{CLK}		256		kHz	
CHCLK Min Pulse Width	T_{CLK}		500		ns	

Recommended Operating Range

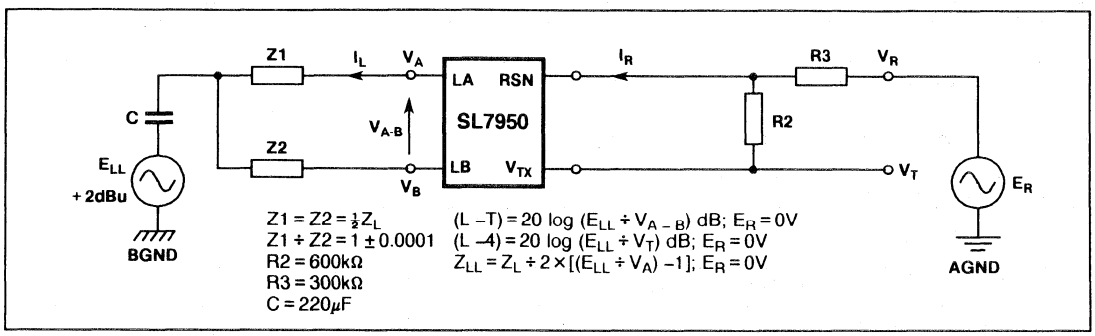
Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply voltage	V_{CC}	4.75	5.0	5.25	V	
Negative supply voltage	V_{EE}	– 4.75	– 5.0	– 5.25	V	
Battery supply voltage	V_{BAT}	– 40.5	– 48	– 64	V	
Battery ground voltage	V_{BGND}	– 0.1		+ 0.1	V	
Ambient temperature	T_{AMB}	0		70	°C	



R1 = See Electrical Characteristics
R2 = 600kΩ
R3 = 300kΩ
R4 = See Electrical Characteristics

$G_T = 20 \log (V_T \div V_{A-B})$ dB; $E_R = 0V$
$G_{RI} = 20 \log (I_L \div I_R)$ dB; $E_L = 0V$
$G_R = 20 \log (V_{A-B} \div V_R)$ dB; $E_L = 0V$
$RTL_2 = 20 \log \{(V_{A-B} + \frac{1}{2}E_L) \div (V_{A-B} - \frac{1}{2}E_L)\}$ dB; $E_R = 0V$

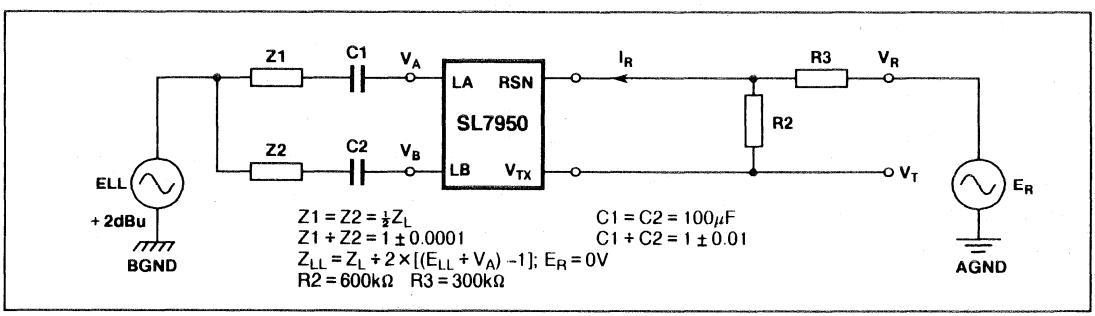
Fig.14 Test configuration (Note the SL7950 block = Fig. 25).



$Z1 = Z2 = \frac{1}{2}Z_L$
$Z1 \div Z2 = 1 \pm 0.0001$
R2 = 600kΩ
R3 = 300kΩ
C = 220μF

$(L - T) = 20 \log (E_{LL} \div V_{A-B})$ dB; $E_R = 0V$
$(L - 4) = 20 \log (E_{LL} \div V_T)$ dB; $E_R = 0V$
$Z_{LL} = Z_L \div 2 \times [(E_{LL} \div V_A) - 1]$; $E_R = 0V$

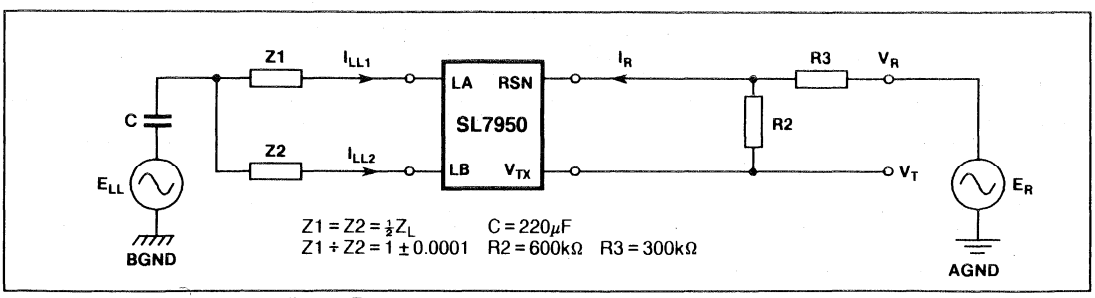
Fig.15 Test configuration (Note the SL7950 block = Fig. 25).



$Z1 = Z2 = \frac{1}{2}Z_L$
$Z1 \div Z2 = 1 \pm 0.0001$
$Z_{LL} = Z_L \div 2 \times [(E_{LL} \div V_A) - 1]$; $E_R = 0V$
R2 = 600kΩ R3 = 300kΩ

C1 = C2 = 100μF
C1 ÷ C2 = 1 ± 0.01

Fig.16 Test configuration (Note the SL7950 block = Fig. 25).



$Z1 = Z2 = \frac{1}{2}Z_L$
$Z1 \div Z2 = 1 \pm 0.0001$
C = 220μF
R2 = 600kΩ R3 = 300kΩ

Fig.17 Test configuration (Note the SL7950 block = Fig. 25).

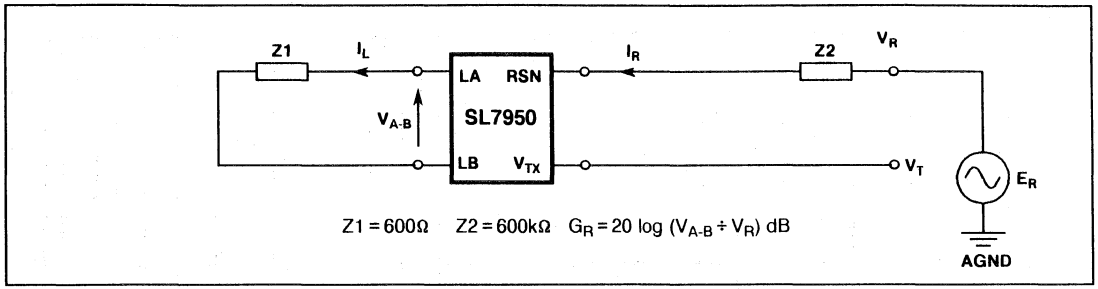


Fig.18 Test configuration (Note the SL7950 block = Fig. 25)

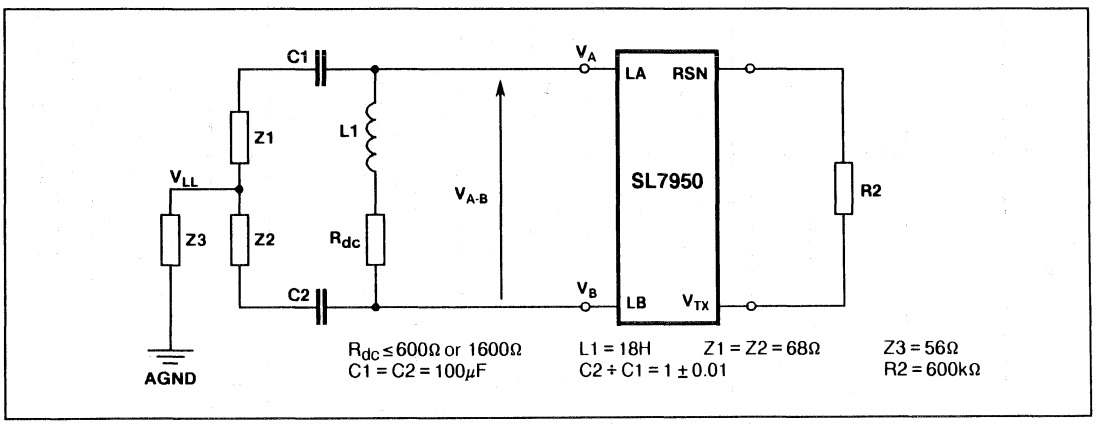
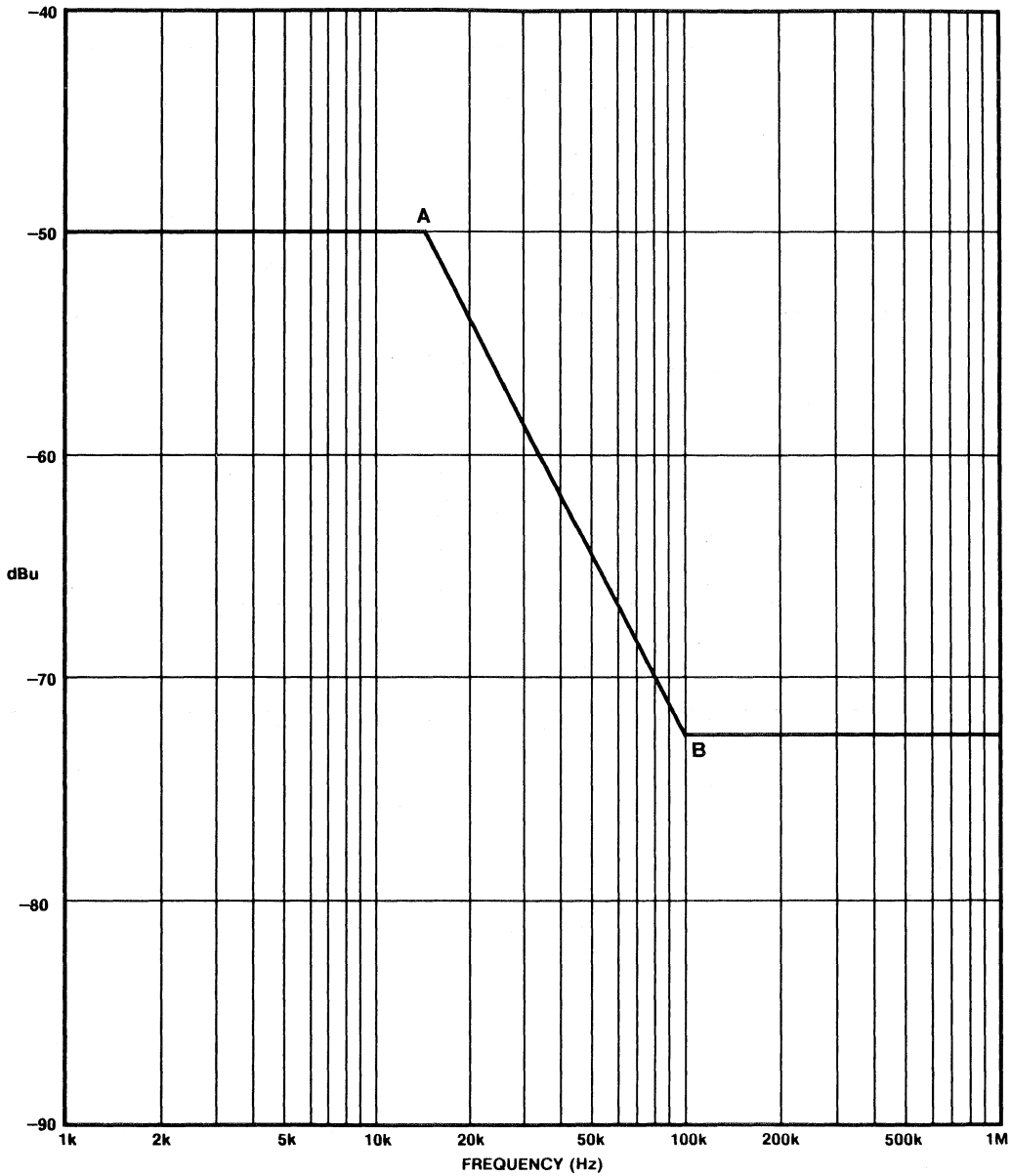


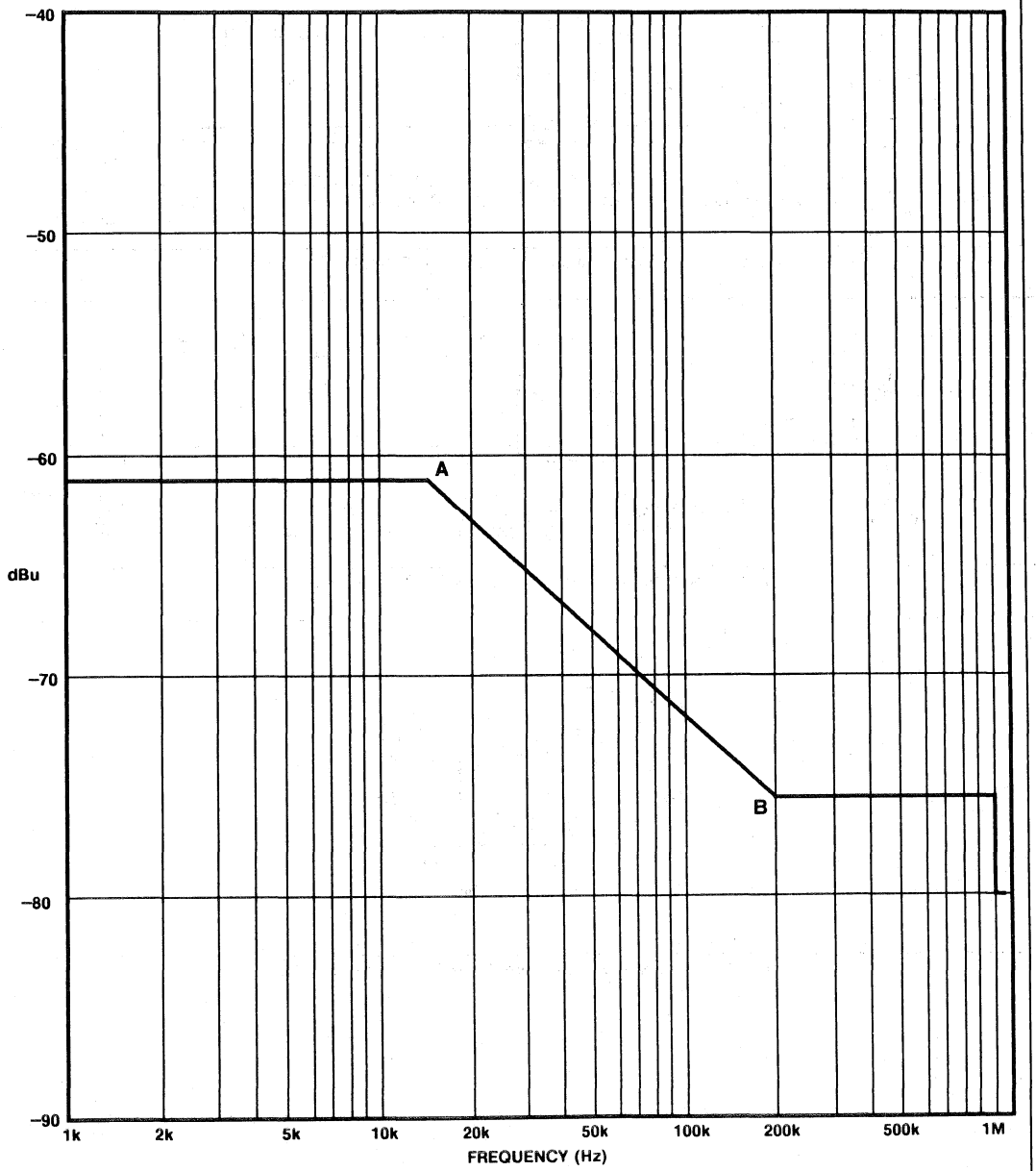
Fig.19 Test configuration (Note the SL7950 block = Fig. 25).



FREQUENCY AT CENTRE OF BAND

A = 15kHz –50dBu
B = 100kHz –73dBu
Bandwidth = 3kHz Minimum Centre Frequency = 1.6kHz
V_{A-B} < –73dBu. f > 1MHz

Fig.20 2-Wire differential noise



FREQUENCY AT CENTRE OF BAND

A = 15kHz	-61dBu
B = 200kHz	-75dBu
Bandwidth = 3kHz	
V_{LL} < -80dBu.	f >1MHz

Fig.21 2-Wire longitudinal noise

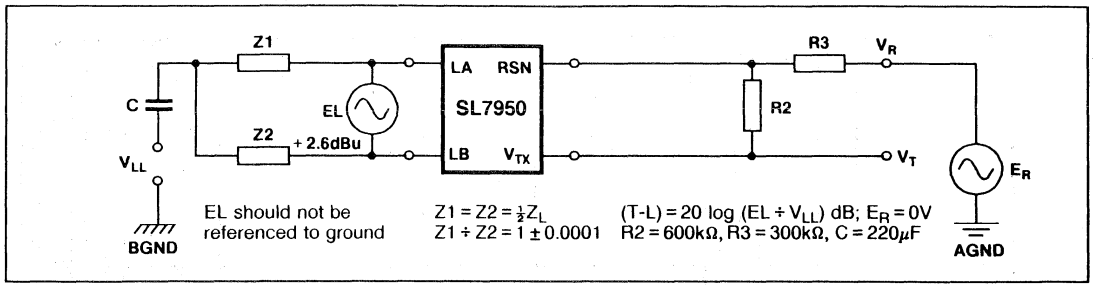


Fig.22 Test configuration (Note the SL7950 block = Fig. 25)

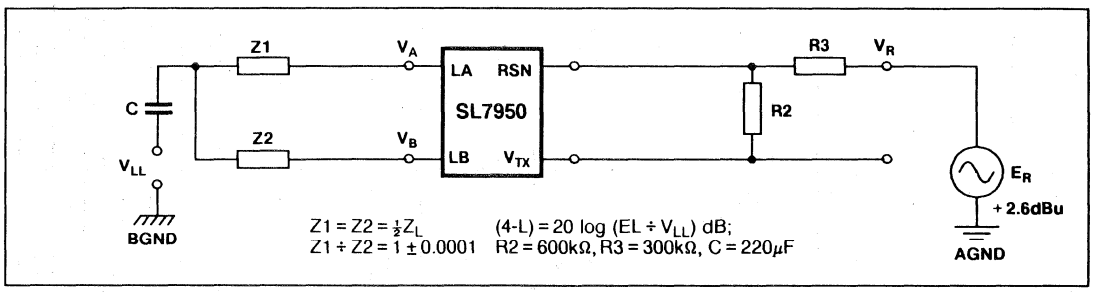


Fig.23 Test configuration (Note the SL7950 block = Fig. 25).

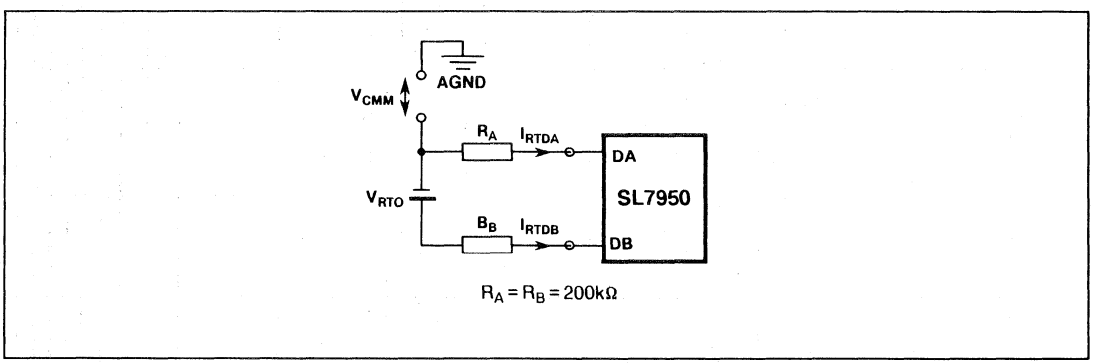
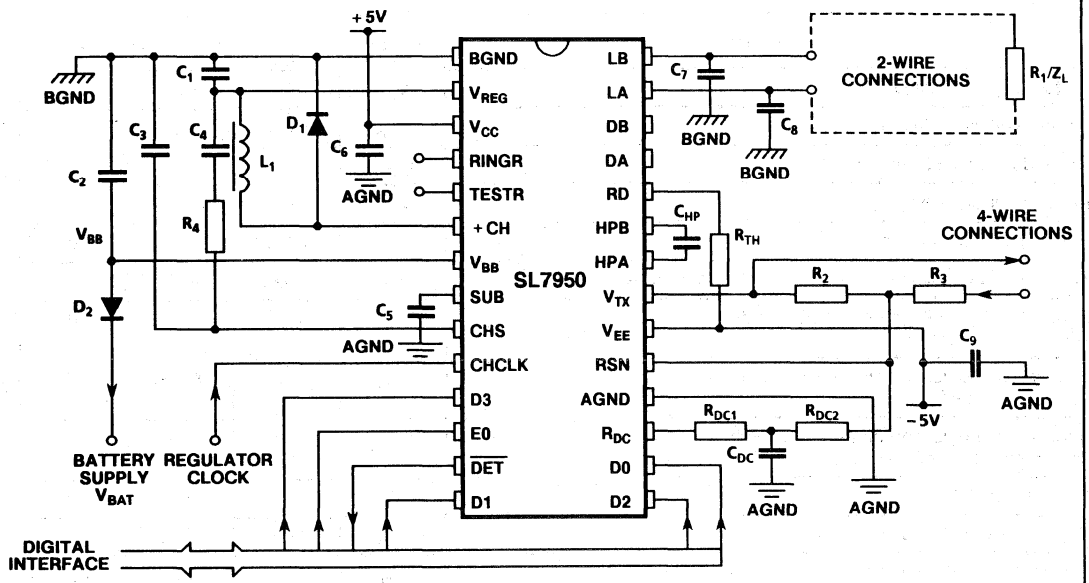


Fig.24 Test configuration (Note the SL7950 block = Fig. 25).



$C_1 = 470n$	$C_6 = 100n$	$C_{DC} = 100n$	$R_{TH} = 56k\Omega$
$C_2 = 470n$	$C_7 = 2.2n$	$D_1 = 100V, 100mA$	$R_{DC1} = R_{DC2} = \frac{1}{2}R_{DC} = 20k\Omega$
$C_3 = 560p$	$C_8 = 2.2n$	$D_2 = 100V, 100mA$	R_1, R_2, R_3 as Test Configuration
$C_4 = 8.2n$	$C_9 = 100n$	$L_1 = 1mH$	Z_L: See Electrical Characteristics
$C_5 = 330n$	$C_{HP} = 330n$	$R_4 = 2.4k\Omega$	

For all tests assume AGND = BGND.

Fig.25 Test circuit for Figs. 14-19 and 22-24

ABSOLUTE MAXIMUM RATINGS* - Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value		Units
		Min.	Max.	
Battery supply voltage	V_{BB}	– 70	+ 0.4	V
Battery voltage, rate of change	V_{BBR}	– 0.4	+ 0.4	V/µs
Continuous battery ground voltage	V_{BGNDC}	– 0.3	+ 0.3	V
Positive supply voltage	V_{CC}	– 0.4	+ 7.0	V
Negative supply voltage	V_{EE}	– 7.0	+ 0.4	V
Subscriber line voltage on LA, LB or both, continuous	V_{LC}	– 70.0	+ 2.0	V
Subscriber line voltage on LA, LB or both, 10ms duration, f = 0.1 Hz rate	V_{LR1}	–70	+ 5.0	V
Subscriber line voltage on LA, LB or both, 1µs duration, f = 0.1 Hz rate	V_{LR2}	–90	+ 10.0	V
Subscriber line voltage on LA, LB or both, 250ns duration, f = 0.1 Hz rate	V_{LR3}	–120	+ 15.0	V
Current from LA or LB	$I_{LLA/B}$		± 150	mA
Switched regulator voltage (off)	V_{CH}	V_{BB}	+ 1.0	V
Switched regulator current (on)	I_{CH}		150	mA
Chopper stabilisation voltage	V_{CHS}	V_{BB}	0	V
RINGR/TESTR relay driver voltage	V_{RLY}	V_{BAT}	V_{CC}	V
Relay source current	I_{RING}		30	mA
Ring-Trip input voltage (DA or DB)	V_{RT}	V_{BB}	0	V
Digital input voltage	V_{ID}	– 0.4	V_{CC}	V
Digital input current (sink)	I_{ID}		– 5.0	mA
Digital output voltage	V_{OD}	– 0.3	V_{CC}	V
Digital output current (source)	I_{OD}		3	mA
Storage temperature	T_{ST}	– 55	+ 150	°C
Operating junction temperature †	T_{JOP}		+ 150	°C
Package power dissipation (DG28 package)	P_{PDG28}		1.5	W
Package power dissipation (LC32 package)	P_{PLC32}		1.2	W

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

† Circuit includes thermal protection such that TPROT (Min) = 150°C.

SL7953

SUBSCRIBER LINE INTERFACE CIRCUIT

The SL7953 is a Subscriber Line Interface Circuit (SLIC) for use at the telephone exchange or PABX end of a telephone line.

It provides power feed, transmits and receives voice signals, controls ringing and detects Ground Key or Off-Hook conditions. These functions can be programmed to provide the flexibility required for different telephone networks.

The SL7953 is fabricated using bipolar technology.

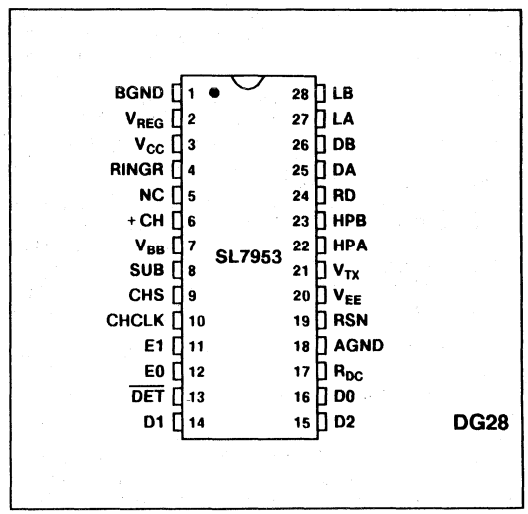


Fig.1 Pin connections - top view

FEATURES

- Low Power Line Feed via Regulator
- Programmable Constant Current Feed Independent of Battery, to Line
- Programmable AC Termination Impedance
- Good Longitudinal Balance
- Ground Key and Ring Trip Detection
- Programmable Off-Hook Detection
- Disconnect and Low Power Standby Modes
- A-Leg Disconnect, B-Leg Standby Mode
- Normal or Reversed Line Polarity Operation
- Ring Relay Driver
- Thermal Shut-Down Protection
- Direct Replacement for Am7953

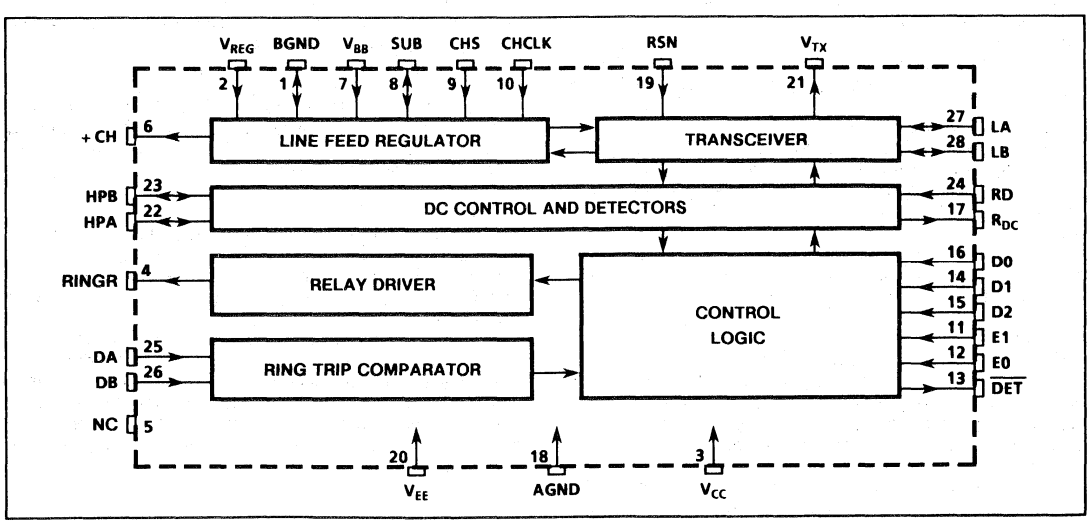


Fig.2 Functional block diagram

FUNCTIONAL OVERVIEW

The SL7953 Subscriber Line Interface Circuit (SLIC), together with some external components, provides most of the line interface functions for ordinary or PABX line connections in a telephone network. It performs the interface between the two wire line and an ALAP (Analogue Line Audio Processor)/COMBO, such as the GEC Plessey Semiconductors MV3010 PSLAC (Plessesy Subscriber Line Audio Circuit) DSP device.

The SLIC circuit contains several functional blocks to achieve the design aims (Fig.2). Firstly, the Transceiver consists of the two wire port, pins LA and LB. These pins are fed from the 4-wire input (RSN) controlling AC conditions, and from the Line Feed Regulator and DC Control blocks, controlling DC conditions. The 2-wire transverse AC signal is fed onto the 4-wire transmit output, V_{TX}.

Power dissipation is minimised, under varying line conditions, by the Line Feed Regulator which adjusts the internal high voltage supply to that required for line feed. It consists of a switching regulator, which can be synchronised to a 256kHz clock.

DC line conditions at the 2-wire interface are determined by the DC Control block. These DC conditions (modes of operation) are set by the Control Logic, which also monitors line status (On/Off-Hook) via the DC Control block detectors (Loop/Ground Key/Ring Trip comparator). The control logic also controls the Ring Relay Driver for Ringing mode of operation.

A brief outline of the device functionality is given below, before a more detailed discussion of the SLIC circuitry in the Functional Description section.

LINE FEED

Line loop (pins LA & LB) feeding is obtained from the battery supply (pin 7) by means of an internal power circuit, which can be set to different modes of operation (refer to table 2). These modes are as follows:

Standby Mode

Standby mode is the SLIC's low power mode in which the battery feed circuit limits the DC loop current to a level just sufficient to enable the SLIC to detect current above the On/Off-Hook threshold. This mode is used when the subscriber is Off-Hook and no call is in progress, or if On-Hook, to save power. Both the Loop and Ground Key detectors work in this mode.

Disconnect A and B Leg

This mode programs the SLIC such that the A and B leg output amplifiers are turned off, preventing current flow to the line.

Disconnect A, Standby B Leg

This is the SLIC Standby mode with the A Leg amplifier turned off, so that current can only flow in the B Leg. In this state it is only possible to detect the application of a ground to the B Leg.

Active Mode

This is the normal operating mode with a call in progress. The SLIC is used as a constant current feed device, with the feed current being set by external resistors.

Polarity reversal

The polarity of the feeding voltage at the SLIC can be reversed on command, in Active and Standby modes. All Active and Standby conditions apply equally to the respective reverse conditions. In these conditions the polarity of any DC parameter is reversed.

Ringing

This mode enables the Ring Relay output and selects the Ring Trip comparator. It does not provide DC line feed or AC ringing voltage which must be supplied externally (via the ring relay).

SUPERVISION

The SLIC provides an Off-Hook (or loop) Detector (OHD), Ring Trip Detector (RTD) and a Ground Key Detector (GKD). These are described below, in addition to the SLIC on-chip thermal protection.

Off-Hook Detector

The Off-Hook Detector recognises the loop status by means of a threshold circuit. The OHD operates in Standby and Active modes (with or without polarity reversal), and in the presence of longitudinal currents. The detector threshold is nominally the same in Standby and Active modes, the actual level being externally programmable.

Ring Trip Detector

This detects when a subscriber goes off-hook during the application of a ringing signal (normally 25Hz) within a maximum delay of 150ms (determined by external components - see Applications section). The detector is active when the Ring Relay Driver is activated.

Ground Key Detector

The GKD circuit detects a current path from the A or B Leg to ground. It can be used in Standby, Active and Disconnect A Standby B modes.

Thermal Protection

In conditions which cause the chip junction temperature to rise above a critical level (around 140°C), the thermal protection will operate. This switches off the line current and therefore reduces the power dissipation.

TRANSMISSION

The signal transmission functions include 2 to 4-wire and 4 to 2- wire conversions.

The 2-wire termination impedance of the SLIC is programmed by external components. Transmit and Receive Gain are fixed and are nominally both unity (0dB), with the 2- wire port terminated in a matched load.

All the transmission parameters apply when the SLIC is operating in the presence of longitudinal currents, as specified in the Electrical Characteristics.

CONTROL

The SLIC is provided with a digital interface for controlling the 2-wire line status and passing line status information to the line card/system hardware. The operating characteristics can be selected by hardware with external components (see Digital Interface).

METERING

Injection of high amplitude high frequency meter pulses is not supported by the SL7953. If this function is required, then the GPS SL376 Metering SLIC can be used instead (refer to separate Data Sheet).

RINGING

The application of the ringing voltage to the subscriber line can be via a relay or suitable high voltage crosspoint, external to the SLIC. This component is driven by the on-chip Ring Relay Driver. The relay is connected between RINGR and V_{BAT}.

When the SLIC is set to RING mode, the Ring Relay Driver output will be activated to energise the ring relay. The relay should be connected so as to cause the line to be disconnected from the SLIC and connected to a suitable ringing supply (continuous) voltage. Ring cadence can then be obtained by de-energising and re-energising the relay as required.

OVERVOLTAGE PROTECTION

Overvoltage protection is required to protect the SLIC from such line phenomena as lightning strikes, and induced AC signals from, or direct contact with, power lines. A suitable form of protection for the SL7953 is described in the SL373/SL376 Application Note AN82.

TEST ACCESS

The testing of the subscriber line is achieved using components external to the SL7953.

INTERFACES

The SL7953 has three main interfaces to external circuitry. These are the 2-wire, 4-wire and Digital interfaces which are described below.

Subscriber Line Interface (2-wire port)

Pins LA and LB form the Subscriber Line Interface providing line feed, signalling supervision and voice transmission between the subscriber's apparatus and exchange. It exhibits very good balance about ground to minimise the crosstalk between adjacent pairs in the local cable and noise from longitudinal interference. The termination impedance is set externally by Z_{TX} (see Fig. 3 and Functional Description).

The 2-wire port is designed to offer a low impedance to any longitudinal signals that appear on the subscriber line and the resulting signal level at the 4-wire output port is minimised. It is able to handle longitudinal currents on the subscriber line in all modes of operation, except Disconnect, Ringing and Disconnect A Standby B modes when the MSLIC 2-wire port is no longer connected to the line.

Analog 4-wire interface

Two pins of the SLIC (V_{TX} and RSN), together with associated grounds, provide the 4-wire interface to an ALAP or COMBO device. Both the transmit (V_{TX}) and receive (RSN) signals are unbalanced and have fixed gain settings. The V_{TX} pin has a low output impedance, whilst the RSN pin is a low impedance virtual earth input. The input current is normally a combination of the receive voice signal from the ALAP, line feed current programmed by the R_{DC} pin (see Applications section) and termination of the V_{TX} pin.

Hybrid Balancing is not provided on the SL7953. This can be done by an ALAP such as the MV3010 PSLAC which uses DSP techniques, including an Adaptive Echo Cancellation feature.

Digital Interface

This is a parallel interface providing control of all the SLIC operating modes and indication of line status information. It consists of the 6 pins as listed in Table 1, the functions of which are described in Table 2.

Pin designation	Pin description
D0	Data input
D1	Data input
D2	Data input
E0	Detector data output enable
E1	Detector select input
$\overline{DET}$	Detector data output

Table 1 Digital interface pin designation

Mode	D2	D1	D0	E0	$\overline{DET}$ output status (Note 2)	
					E1 = 0	E1 = 1
Disconnect A & B Legs	0	0	0	1	(Invalid)	(Invalid)
Ringing	0	0	1	1	Ring Trip (Note 3)	-
Active(non-ringing)	0	1	0	1	Loop Detect	Ground Key
Standby	0	1	1	1	Loop Detect	Ground Key
Disconnect A,standby B	1	0	0	1	(Invalid)	Ground Key
Reserved	1	0	1	1	-	-
Active, polarity reversed	1	1	0	1	Loop Detect	Ground Key
Standby, polarity reversed	1	1	1	1	Loop Detect	Ground Key
As selected by D2-D0,E1 (note 1)	0/1	0/1	0/1	0	1 (off)	1 (off)

NOTES

1. D2, D1, D0 still change SLIC status even though $\overline{DET}$ output is forced to 1 (5V).
2. $\overline{DET}$ = 1 for On-Hook (high line impedance), $\overline{DET}$ = 0 for Off-Hook (low line impedance).
3. $\overline{DET}$ = 1 for Voltage DA > DB , $\overline{DET}$ = 0 for Voltage DA < DB.

Table 2 Digital interface functional description.

FUNCTIONAL DESCRIPTION

VOICE TRANSMISSION AND RECEPTION

It is conventional to assign the signal directions from the point of view of the served telephone set. The receive direction is towards the served telephone and the transmit direction is from it.

The basic voice circuit for the device is shown in Fig.3. The current which flows on the line, into LA and out of LB, is 1000 times the current which flows into RSN and through the device to AGND.

The AC voice current flowing into RSN is composed of the current from V_{RX} through Z_{GR}, which controls the signal received at the remote telephone and a current from V_{TX} through Z_{TX} which controls the termination impedance. There is also a DC current at RSN which is analysed later in the discussion on DC line feed.

The 2-wire termination impedance is $Z_{AB} = (Z_{TX} \div \alpha)$ where α ($\simeq 1000$) is the current gain between RSN and I_L (see Fig.3). This can be checked by setting V_{RX} to zero.

The Receive Gain, for normal voice signals (at V_{RX}), is inversely proportional to Z_{GR}. The actual value, which is negative, can be obtained by setting $(V_L)_{ac}$ equal to zero in Fig.3. This gives:-

AC voltage between LA and LB $(V_{LA}-V_{LB})_{ac}$

$$= (V_{LA} - V_{LB}) - (V_{HPA} - V_{HPB})$$
$$= (I_L)_{ac} \times \{Z_{AB} \| Z_L\}$$
$$= -\left(\frac{Z_L \times \frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right)\frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}$$

i.e. minus the ratio of the line and terminating impedances (Z_L and $Z_{TX} \div \alpha$) in parallel, to the receive impedance divided by the current gain ($Z_{GR} \div \alpha$). This expression simplifies to :-

$$= \frac{-V_{RX}\alpha Z_L Z_{TX}}{(\alpha Z_L + Z_{TX})Z_{GR}}$$

In the transmit direction, the voltage at V_{TX} is the superposition of the voltage from the line, with the voltage produced on the line from V_{RX}, i.e:-

$$V_{TX} = \left[\left(\frac{\frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right)V_L - \left(\frac{Z_L \times \frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right)\frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}\right]$$

This expression simplifies to :-

$$V_{TX} = \frac{[Z_{GR}(V_L)_{ac} - \alpha Z_L V_{RX}]Z_{TX}}{(\alpha Z_L + Z_{TX})Z_{GR}}$$

This equation can be used to determine the transmit gain, from $(V_L)_{ac}$ to V_{TX}, by setting $V_{RX} = 0$ which gives $+ Z_{TX} \div (\alpha Z_L + Z_{TX})$. The 4 wire-4 wire gain, V_{RX} to V_{TX}, is also given by this equation when setting $(V_L)_{ac} = 0$, which gives us the alternative result $-\alpha Z_L Z_{TX} \div [(\alpha Z_L + Z_{TX})Z_{GR}]$. If fuse resistors are included in the 2 wire loop, then Z_L is modified to become $(Z_L + 2R_F)$ in the above equations.

The transmission circuitry also contains a longitudinal feedback circuit, such that the SLIC appears as typically 25Ω resistors from LA and LB to a bias voltage (see DC Line feed section). This bias voltage comes from the DC feed circuitry. The feedback circuit attenuates longitudinal signals from the transmit path, and has no effect on transverse signals.

DC LINE FEED (Active Mode)

DC line feed (loop) current $I_L = \frac{1}{2}(|I_A - I_B|)$ is provided by the device when it is in non-ringing modes. In RING mode, DC line feed and AC ringing voltage are normally applied through the ring relay which is controlled by the device. The line feed current is reduced during standby operation.

In Active mode, Power feed is controlled by the resistance R_{DC} between the R_{DC} pin and the RSN pin (Fig.4). Again, the current in the 2 wire loop will be 1000 times the current into RSN. Operation of the DC feed circuitry is described with reference to Fig.4, which shows a conceptual model.

For the normal line feed region, a voltage V_{DC}, of magnitude 2.5V is produced at the R_{DC} pin. The sign of V_{DC} determines normal or reverse polarity operation. If negative, normal polarity is established and if positive, reverse polarity will occur (polarity is set by control logic - see Table 2). This normal line feed region exists when $|V_{BAT}| - |V_{DCT}| \geq V_{SG}$ ($V_{SG} = 15V$ nominally, $V_{DCT} = |V_{LA} - V_{LB}|$), else the Saturation Guard circuit is active (described later).

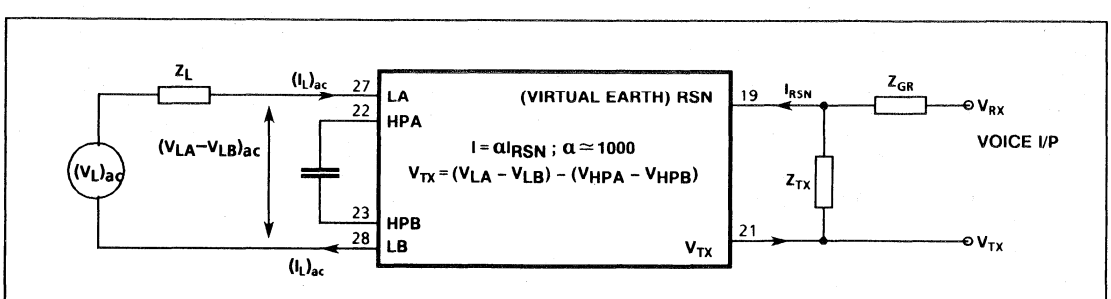


Fig.3 Voice circuit

Note that the internal resistors, R_{HP}, and external capacitor, C_{HP}, form a low pass filter network (the discussion on C_{HP} in SL373/SL376 Application Note AN82 Applications General Considerations Section is also valid for the SL7953). During the action of reversing polarity, the resistors R_{HP} are momentarily short-circuited to reduce the time taken for the DC voltage on C_{HP} to change sign.

The ×1000 virtual earth input current amplifier means that the feed current is determined by R_{DC}, i.e:-

$$I_{FEED} = 2500 \div R_{DC} \text{ (Saturation Guard inactive)}$$

If fuse resistors are included in the 2-wire loop, the feed current will not be affected. However, the fuse resistors will affect the line current in the saturation guard region (desribed later).

As an example, to set $I_{FEED} = 40mA$, then:-

$$R_{DC} = (R_{DC1} + R_{DC2}) = 2500 \div I_{FEED} = 62.5k\Omega$$

The values of R_{DC1} and R_{DC2} should be kept nearly equal, forming a low pass filter network with C_{DC} to reduce chopper noise from the RDC pin (see also discussion in AN82 Applications General Considerations Section). The time constant of this network (C_{DC} and $R_{DC1} \| R_{DC2}$) also affects the time taken for a polarity reversal, and it is normally ≈1.5ms.

The remaining circuitry models the action of the saturation guard circuit. This operates to reduce the voltage at the RDC pin when:- $|V_{BAT}| - |V_{DCT}| < V_{SG}$. V_{SG} is a notional threshold voltage which is the headroom between the value of V_{DCT} and the battery voltage at the point where saturation guard becomes active (this includes the diode drop in series with the V_{BAT} supply, D_2 figure 7). Thus, when the comparator determines this condition, the magnitude of the difference is used to reduce the voltage at RDC.

The total line feed characteristic is shown graphically in Figs. 6a and 6b. The nearly constant voltage region is due to the action of the saturation guard circuit, and is affected by the value of R_{FUSE} as shown in Fig. 6a. Fig. 6b plots the loop current value as a function of line resistance R_L. The example shown is that of a 40mA ($R_{DC} = 62.5K\Omega$) feed current, the graphs being obtained by using the simple models of Figs. 5a and 5b (0Ω fuse resistors). Figs. 6a and 6b also show the action of V_{BB} on the line characteristics.

With the Saturation Guard inactive, normal line feed conditions apply such that the feed current and line/loop resistance determine V_L by the following relationship:-

$$V_L = I_L \times R_L$$

This gives the characteristic shown in Fig. 6a, which is the vertical line section of the graph.

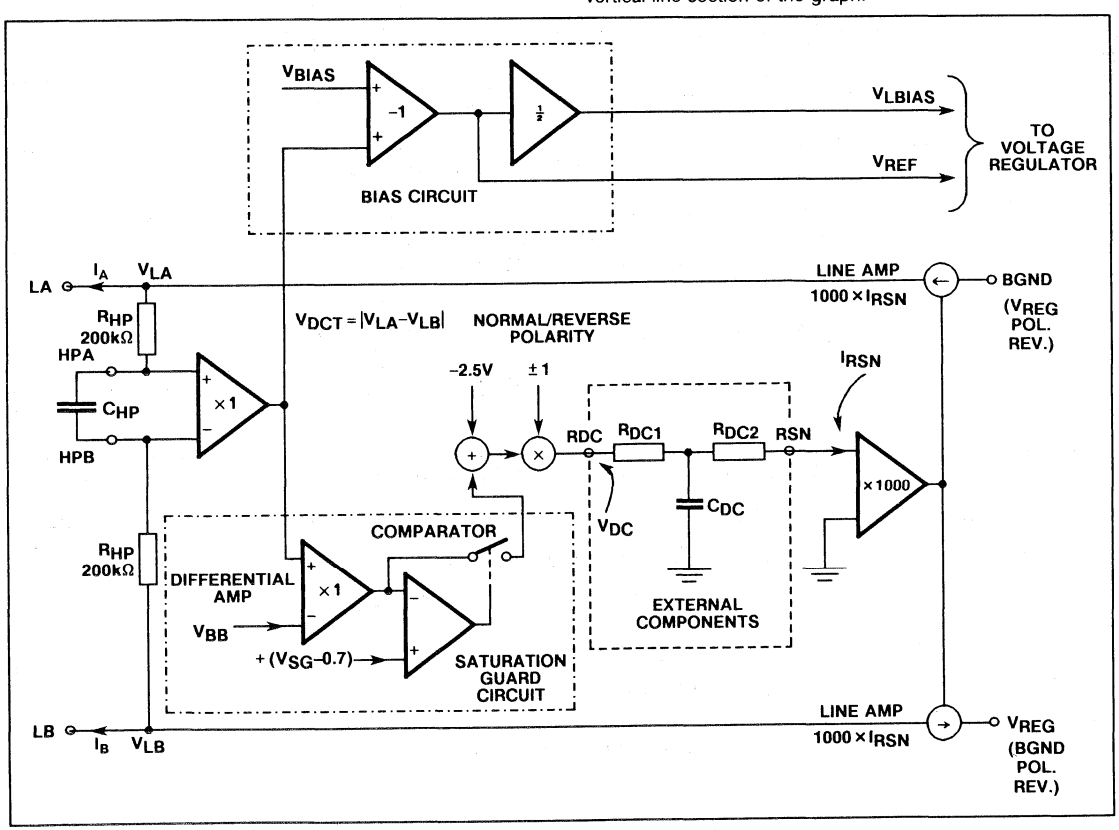


Fig.4 DC power feed circuit model.

When the saturation guard is active, then the line voltage is effectively held constant due to the reduction of the voltage at the R_{DC} pin. Thus, line conditions are set by the following:

$$I_L = [(|V_{BAT}|-V_{SG}) \div (R_L + 2R_{FUSE})]$$

To determine the line resistance (R_{LSG}) and Line voltage (V_{LSG}) at which the saturation guard becomes active, these parameters are obtained by equating the two expressions for normal and saturation guard regions. Thus,

$$R_{LSG} = [(|V_{BAT}|-V_{SG}) \times (R_{DC} \div 2500)]-2R_{FUSE}$$
$$V_{LSG} = |V_{BAT}|-V_{SG}-[2R_{FUSE} \times (2500 \div R_{DC})]$$

The resultant line voltage (V_{LSG}) that occurs depends on the ohmic relationship of I_{LSG} and R_{LSG} (see Fig. 6a) which will equal $|V_{BAT}|-V_{SG}$ when $2R_{FUSE} = 0\Omega$. The open circuit voltage, $V_{LOC} \approx |V_{BAT}|-V_{SG}$ at $R_L = \infty\Omega$, will always be greater than V_{LSG}, even when $2R_{FUSE} = 0\Omega$. This change in voltage between V_{LSG} and V_{LOC} will be greater at lower battery voltages. Fig. 6a shows the nominal effect.

DC LINE FEED (Standby Mode)

For Standby mode, the DC current is limited to a value just sufficient for the Loop Detector to sense Off-Hook. Normally this threshold (I_{DET}) is set externally by a resistor, R_{TH} (see Control and Signalling section). The limited loop current (I_{LIM}) is also determined by R_{TH} via a conversion factor K_{LIM} (nominally 1.7,) such that :-

$$I_L \leq I_{LIM} = K_{LIM} \times I_{DET}$$

The shape of this characteristic is almost a constant current, as shown in Fig. 6a. Since $K_{LIM} > 1$, the current level is still sufficient to detect the Off-Hook threshold (see Control and Signalling section).

LINE POLARITY

Normal line polarity (Active/Standby) consists of the LA pin voltage near to BGND and the LB pin voltage near to V_{BAT}. Under these conditions $I_L = +\frac{1}{2}|I_A-I_B|$ and the voltage at the R_{DC} pin will be negative. Reverse polarity will give LA voltage near V_{BAT}, LB voltage near BGND, $I_L = -\frac{1}{2}|I_A-I_B|$ and the R_{DC} pin is positive.

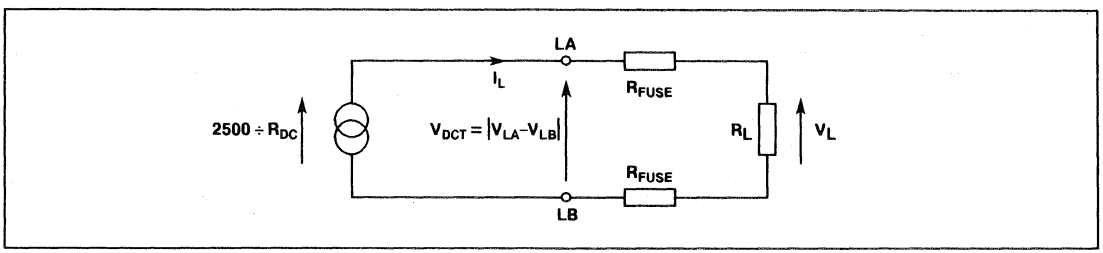


Fig. 5a Simple power feed model (normal line feed)

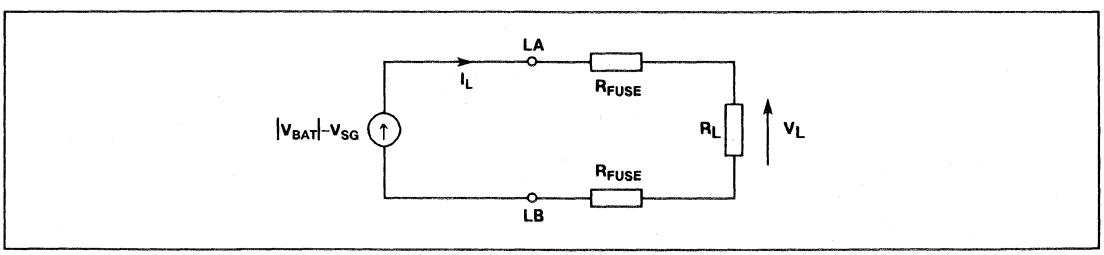


Fig. 5b Simple power feed model (saturation guard active)

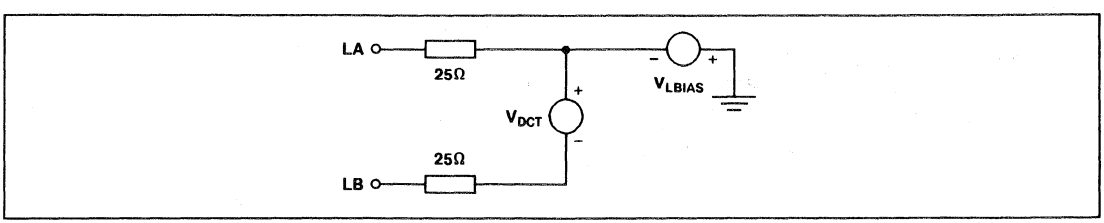
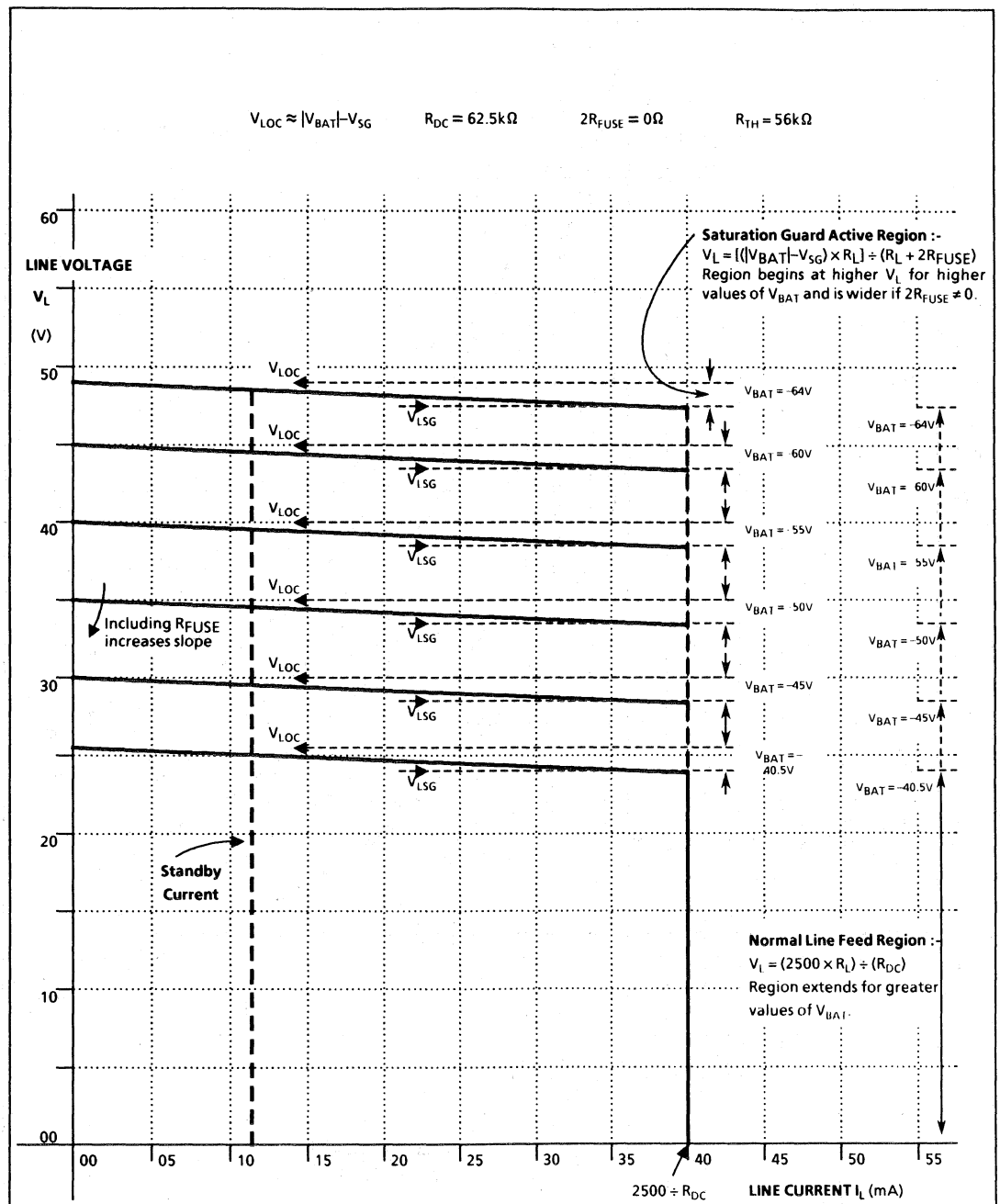


Fig. 5c Longitudinal bias circuit.



$V_{LSG} = (|V_{BAT}|)-[V_{SG} + (2R_{FUSE} \times 2500) \div (R_{DC})]$

$R_{LSG} = [(|V_{BAT}|-V_{SG}) \times (R_{DC}) \div 2500)]-2R_{FUSE}$

Note for Saturation Guard, constant voltage (V_{LA}-V_{LB}) region depends on V_{BAT}; even with $2R_{FUSE} = 0$ (as shown) some voltage drop between the values of V_{LOC} and V_{LSG} will occur.

Fig. 6a Line feed characteristic, V_L vs I_L.

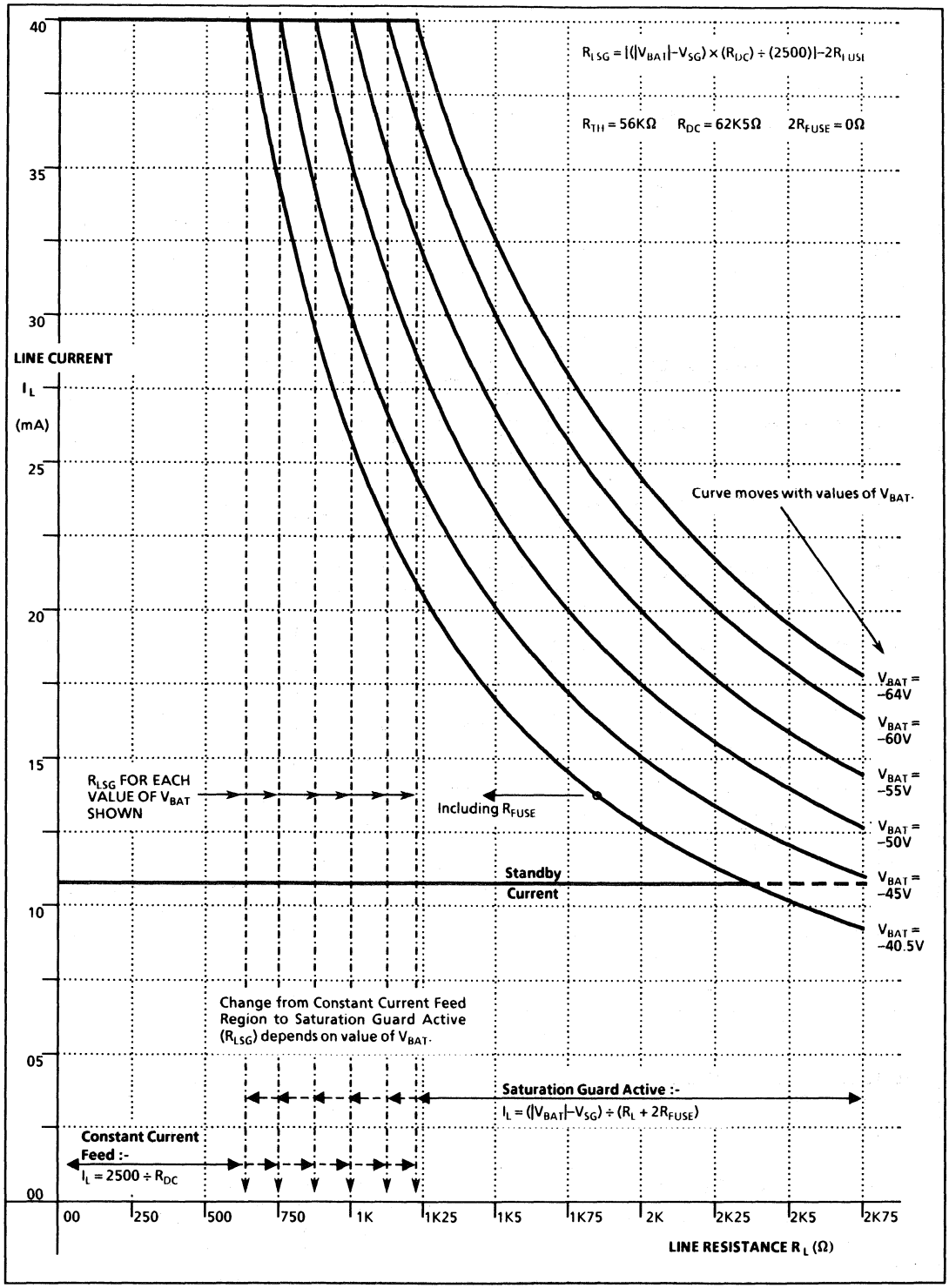


Fig. 6b : Line Feed Characteristic, I_L vs R_L.

BIAS CIRCUIT

The Bias circuit (Fig. 4) produces two reference voltages, both referred to ground. These are V_{REF}, being related to the 2-wire transverse DC voltage and V_{LBIAS} approximately half V_{REF}.

V_{REF} controls the line feed regulator and V_{LBIAS} sets the 2-wire feed balance voltage (centre point voltage of the lines). The longitudinal control loop achieves an input impedance of approximately 25Ω per line for longitudinal signals, as shown in Fig. 5c.

LINE FEED REGULATOR

The DC voltage between LA and LB will vary with the DC loop resistance. Unless the voltage supplied to the chip can be varied to match that on the line there will be a voltage drop across the chip along the path taken by the feed current. This could cause significant power dissipation. The purpose of the line feed regulator is to minimise this power dissipation by regulating the voltage supplied to the line amplifiers.

Regulated voltage is supplied to the line amplifiers on V_{REG} and unregulated voltage is supplied on V_{BB}. The chip switches V_{BB} onto +CH when more power is required at the V_{REG} pin. V_{REG} is the voltage used by the device to power the 2-wire interface, and it is adjusted to follow a reference voltage V_{REF} (from Power Feed). This reference voltage is determined as follows:

$$V_{REF} = -\{ | V_{DCT} | + V_{BIAS} \}$$

and is such to set V_{REG} to the minimum required to power the line interface, thus minimising power dissipation. The voltage V_{BIAS} is needed to keep the amplifier response linear when audio signals are transmitted.

Fig. 7 shows the external components associated with the power supply aspect of the voltage regulator. +CH is the positive terminal of the regulator switch that connects to V_{BB}. When the switch is turned on, current in L1 and C1 increases, thus increasing stored energy. When the switch turns off, this stored energy sustains L1 current which flows in D1. The voltage at +CH is thus a square wave of up to 50V p-p making this node sensitive to PCB layout. Note that the inductor should be capable of taking twice the line current without saturating. The regulator will work with a wide range of inductor resistance, although if this is too large, long line drive capability and regulator efficiency will be reduced. Since there are large current fluctuations from V_{BB} through the switch, C2 provides filtering of the V_{BB} pin, whilst D2 isolates the V_{BAT} supply should the LA/LB pins be taken negative of the V_{BAT} supply.

The chip senses the voltage at V_{REG}, compares it to its requirements and switches power from V_{BB} to +CH, using the variable mark/space method, to give appropriate matching. The rate of switching can be governed by CHCLK (pin 10) or allowed to free run, its stability ensured by the network on CHS (pin 9), i.e. C3, R1, C5. Since noise is produced by the switching, a decoupling node is provided at SUB (pin 8).

CONTROL AND SIGNALLING

The mode of operation of the SL7953 is determined by the digital interface pins, as described in Tables 1 and 2. These pins enable ringing or non-ringing modes of operation, controlling line status, line polarity, relay driver and selection of line detector.

The line status is selected by use of the D2..D0 pins, Table 2, to determine the modes as listed. The function of these modes has already been described in the 'Overview' and 'DC Line Feed' sections; more detail of the device detectors is given on the following page (refer to Fig. 8).

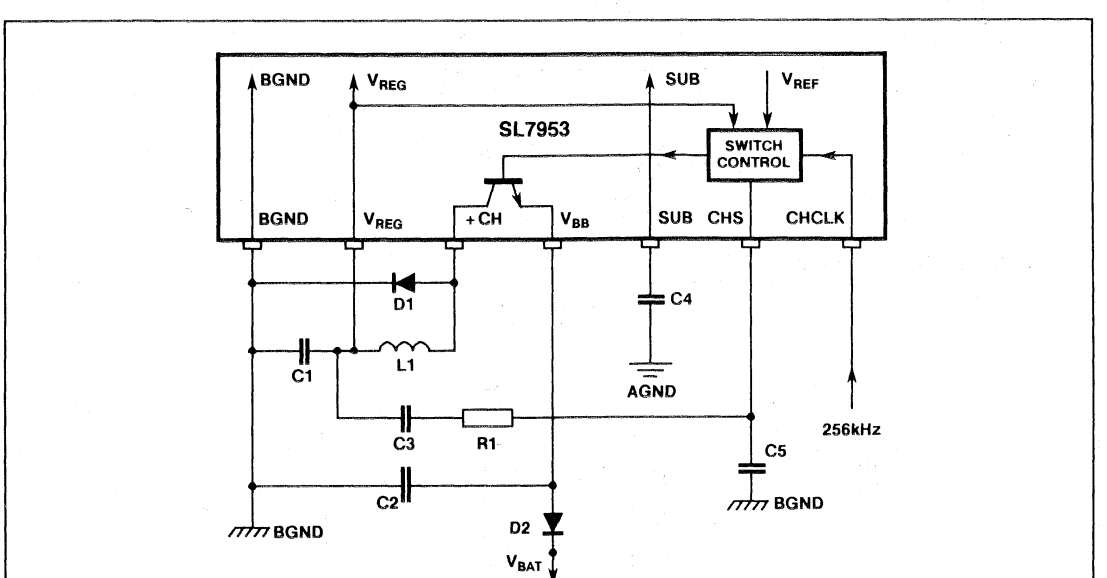


Fig.7 Voltage regulator power supply circuit.

Loop Detect

This detector is used in Active and Standby modes (with/without polarity reversal). The loop current at which the detector indicates the Off-Hook condition, is set by the comparator at pins 24 (RD) and 20 (V_{EE}). Normally a resistor, R_{TH}, is connected between these pins, such that Off-Hook line current threshold (I_{DET}) is set by:

$$I_{DET} = 350 \div R_{TH}$$

This is due to the fact that the current out of the RD pin is equal to the loop current $I_L = (\frac{1}{2}|I_A - I_B|)$ divided by ~280. This will create a voltage across R_{TH} at the RD pin. Off-Hook is given by a logic low at the $\overline{DET}$ output pin (when detector is selected) when this voltage rises above the internal 1.25V reference.

Ground Key Detector

This detector is selected by the E1 pin of the Digital Interface. It can be used in Active and Standby modes (with/without polarity reversal), as well as Disconnect A Standby B mode.

Operation of the detector is via an internal threshold and the longitudinal current $I_{LL} = I_A + I_B$ of the 2-wire loop. Ground Key detection is indicated when either the midpoint of the A and B legs is connected to ground, or the B leg (A leg, polarity reversed) is connected to ground. The resistance values for which Ground Key detection is valid are given in the Electrical Characteristics section.

Ring Trip Detector

This consists of a comparator connected to the DA and DB pins, and indicates Ring Trip when the voltage at DA < DB. Selection of Ringing mode operates the Ring Relay and enables the Ring Trip Detector. The external ringing supply must consist of DC line feed in addition to the AC ringing voltage. In order that the Ring Trip Detector senses Ring Trip in ringing mode, a resistance bridge network is used in association with pins DA, DB, line and ring source. This network is described in the Applications section of this data sheet. It is also discussed further in AN82 (the SL7953 contains the same detector circuit for Ring Trip as the SL373/SL376 SLICs).

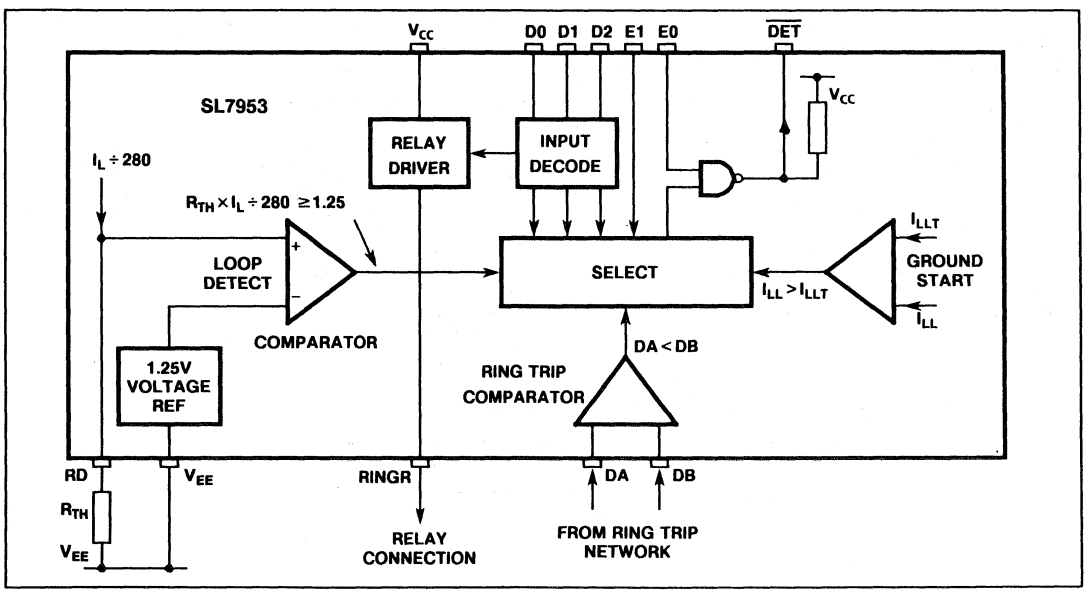


Fig.8 Detector circuits.

FUNCTIONAL PARAMETER SUMMARY

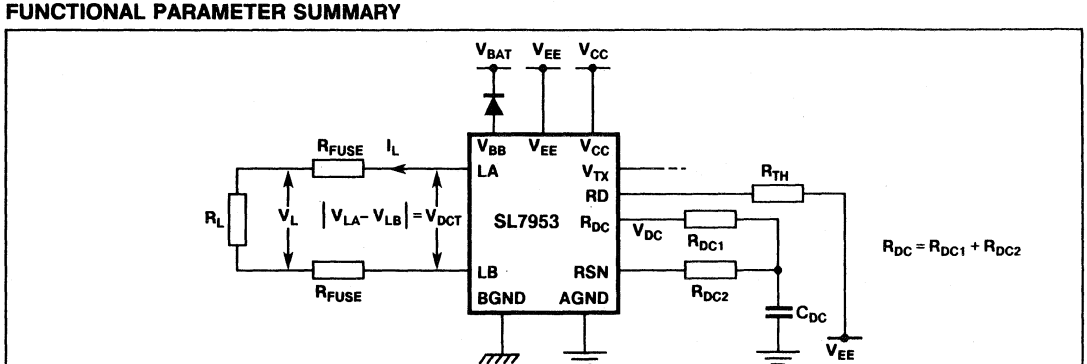


Fig.9 DC parameters and components for the SL7953

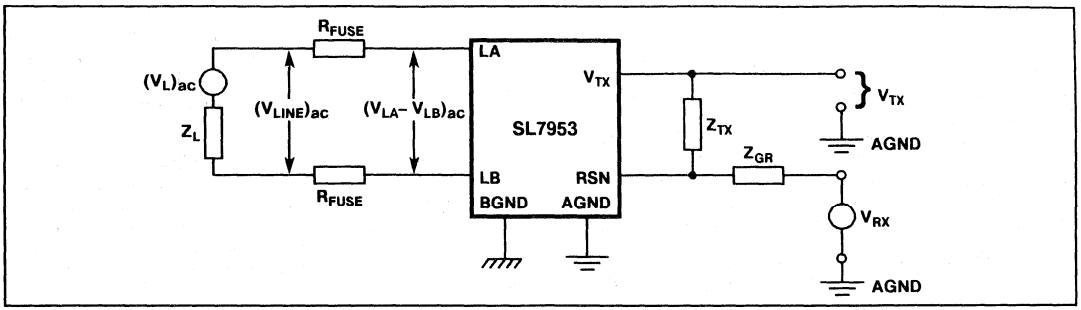


Fig.10 AC parameters and components for the SL7953

LIST OF DEFINITIONS

1. Loop Current is defined as :- $I_L = \pm\frac{1}{2}|I_A - I_B|$

   I_A = current out of LA pin, I_B = current out of LB pin, + ⇒ normal line polarity and –⇒ reverse line polarity.

2. Longitudinal Current is defined as :- $ILL = (I_A + I_B)$

   I_A = current out of LA pin, I_B = current out of LB pin.

3. Normal Line Feed Region when $|V_{BAT}|-|V_{DCT}| > V_{SG}$ with $I_L = I_{FEED} = (2500 \div R_{DC})$

4. Saturation Guard Threshold when $|V_{BAT}|-|V_{DCT}| = V_{SG} = 15.0V$ such that :-

   $V_L = V_{LSG} = |V_{BAT}|-V_{SG}-[2R_{FUSE} \times (2500 \div R_{DC})]$ which will equal $|V_{BAT}|-V_{SG}$ with $2R_{FUSE} = 0$ and
   $R_{LSG} = [(|V_{BAT}|-V_{SG}) \times (R_{DC} \div 2500)]-[2R_{FUSE}]$

5. Saturation Guard feed Region when $|V_{BAT}|-|V_{DCT}| < V_{SG}$ with $I_L = [|V_{BAT}|-V_{SG}] \div [R_L + 2R_{FUSE}]$

6. Note that V_{LSG} is referred to as the value of the line voltage, V_L, at the point where Saturation Guard becomes active. This will differ from the value of $|V_{LA}-V_{LB}|$ (i.e. V_{DCT}) if $2R_{FUSE} \neq 0$. V_{SG} is used as a notional threshold voltage which is the internal headroom between the $|V_{LA}-V_{LB}|$ voltage and the battery supply, at this same point.

7. Open Circuit Line Voltage V_{LOC} at $R_L = \infty\Omega$ such that :- $V_L = V_{LOC} \approx [|V_{BAT}|-V_{SG}]$

   V_{LOC} will be $\geq V_{LSG}$ even with $2R_{FUSE} = 0$. The voltage drop from V_{LOC} to the defined V_{LSG} point will be greater at lower values of V_{BAT}.

8. Standby Mode DC Feed Current $I_L \leq I_{LIM} = K_{LIM} \times I_{DET} \approx 600 \div R_{TH}$

9. 2 Wire Termination Impedance $Z_{AB} = (Z_{TX} \div \alpha) = (Z_{TX} \div 1000)$

   Note that Z_{TX} is normally set to $[\alpha(Z_L + 2R_{FUSE})]$ where Z_L is the desired termination impedance.

10. Recieve Gain from V_{RX} to $(V_{LA}-V_{LB})_{ac}$ or $(V_{LINE})_{ac}$ is set by Z_{GR} after setting Z_{TX}. Thus, with $(V_L)_{ac} = 0$:-

    $$\frac{(V_{LA}-V_{LB})_{ac}}{V_{RX}} = \frac{-\alpha Z_L Z_{TX}}{[\alpha(Z_L) + Z_{TX}]Z_{GR}}$$ with $2R_{FUSE} = 0$; $$\frac{(V_{LINE})_{ac}}{V_{RX}} = \frac{-\alpha Z_L Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]Z_{GR}}$$ with $2R_{FUSE} \neq 0$

11. Resultant Transmit Gain is then :- $$\frac{V_{TX}}{(V_L)_{ac}} = \frac{Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]}$$ with $V_{RX} = 0$

12. Resultant 4 Wire-4 Wire Gain is then :- $$\frac{V_{TX}}{V_{RX}} = \frac{-\alpha(Z_L + 2R_{FUSE})Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]Z_{GR}}$$ with $(V_L)_{ac} = 0$

13. Off-Hook Threshold is set by R_{TH} at :- $I_L = I_{DET} = 350 \div R_{TH}$

14. Ring Trip Threshold is set by the bridge associated with pins 25 .. 28 and the 2 Wire Line, thus :-

    $R_L = R_{LTH} = R_{B4}(2R_F) \div (R_{B4}-R_{B1})$ assuming $R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$ and $R_{FEED1} = R_{FEED2}$ for the bridge components (balanced ringing). $R_{B1}..R_{B4} \approx$ a few 100KΩ and $R_{FEED1} \approx$ a few 100Ω.

15. AC ringing voltage at DA (DB by the same amount) is reduced by a factor of :- $[1 + (2\pi f_r t_r)^2]^{-\frac{1}{2}}$

    f_r is the ringing frequency and t_r is determined by the bridge components including C_B, thus :- $t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$ for balanced ringing

APPLICATIONS

The requirements for the subscriber line interface vary considerably from one telephone administration to another. The SL7953 is designed to have the flexibility to meet these varying requirements. For simplicity, only a single example is given to illustrate how the device is connected. Fig. 11 shows the circuit which can be used to evaluate the device. Further Applications information, as given in AN82 SL373/SL376 Applications Note, is valid for the SL7953 as indicated at relevant points in this section of the data sheet.

The DA and DB pins are connected to a resistance bridge network (R_{B1} to R_{B4}). This allows the change in line resistance to be sensed when the remote telephone goes off-hook during ringing (ring trip). The details of this network (and C_B) are given later (see Ring Trip section). The resistors R_{FEED1} and R_{FEED2} provide feeding of the ringing source onto the line during ringing mode. The Ring Relay coil is connected through a current limiting resistor.

Connections to the LA and LB pins are shown, and include the resistors R_{FUSE} in addition to the ring relay. These resistors have a value around 20 to 30 ohms, depending on the application, and provide current line protection.

Overvoltage and protection circuitry may consist of slew-limiting inductors between the pins and the line itself and a thyristor or Zener protection network at the line. In many applications, especially in PBXs, the amount of protection circuitry can be reduced. The capacitors between LA, LB and ground, allow noise from the regulator to be decoupled.

The capacitor C_{HP} between HPA and HPB is used to filter out the AC component of the signal on the line. The voltage difference between the two pins should be effectively DC. Application Note AN82 contains a further discussion on this component.

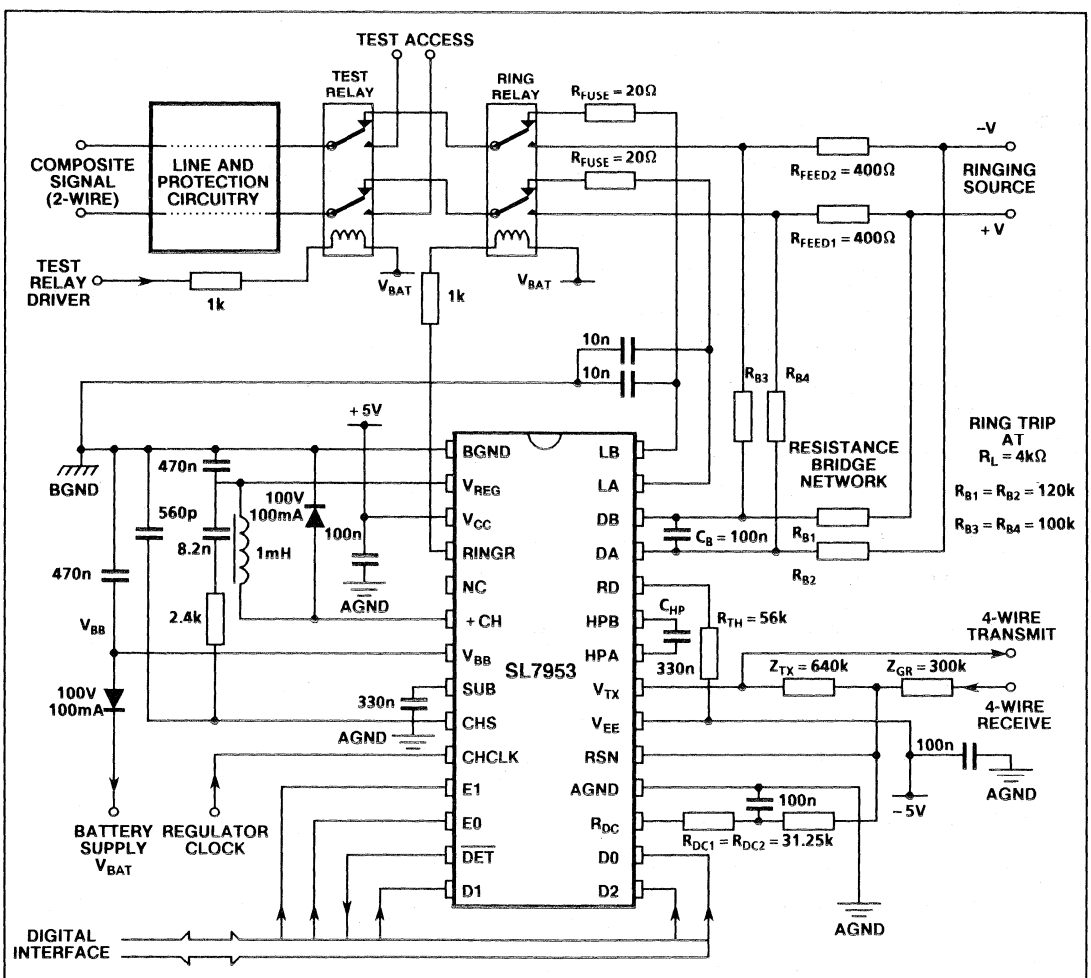


Fig. 11 Application circuit

The resistor, R_{TH}, between RD (pin 24) and V_{EE} (pin 20) programs the threshold current for the loop detector. A capacitor in parallel can be added to reduce the effect of the AC component of the line current, but this can cause instability on standby operation with highly inductive lines if it is too large. The value of R_{TH} sets the current I_{DET} according to the relationship:-

$$I_{DET} = 350 \div R_{TH}$$

CHS is connected to BGND through a capacitor and to V_{REG} by a capacitor and resistor in series. This stabilises the regulator control loop (pins 2, 6 and 7).

It is recommended that the substrate (SUB, pin 8) is decoupled to AGND. However, BGND may be used if this is sufficiently quiet, else some degradation in noise performance may be experienced. The on-chip decoupling resistor between pins V_{BB} and SUB is approximately 140Ω.

DC current flows between RDC (pin 17) and RSN (pin 19). This is used to set the line feed current. Any minor AC fluctuations are reduced by splitting the resistance (R_{DC}) between RDC and RSN, and connecting a capacitor to AGND from the midpoint of the resistance ($R_{DC1} = R_{DC2} = \frac{1}{2}R_{DC}$).

The network (Z_{TX}) between V_{TX} and RSN controls the AC terminating impedance. The value of Z_{TX} can be calculated from the relationship :-

$$Z_{TX} = (\text{Required } Z_T) \times (\text{Receive current gain})$$

The receive gain is set by the network (Z_{GR}) which controls the receive current flowing into RSN. This can be a complex impedance network to allow for complex impedance terminations. More details of these gain settings are given in AN82.

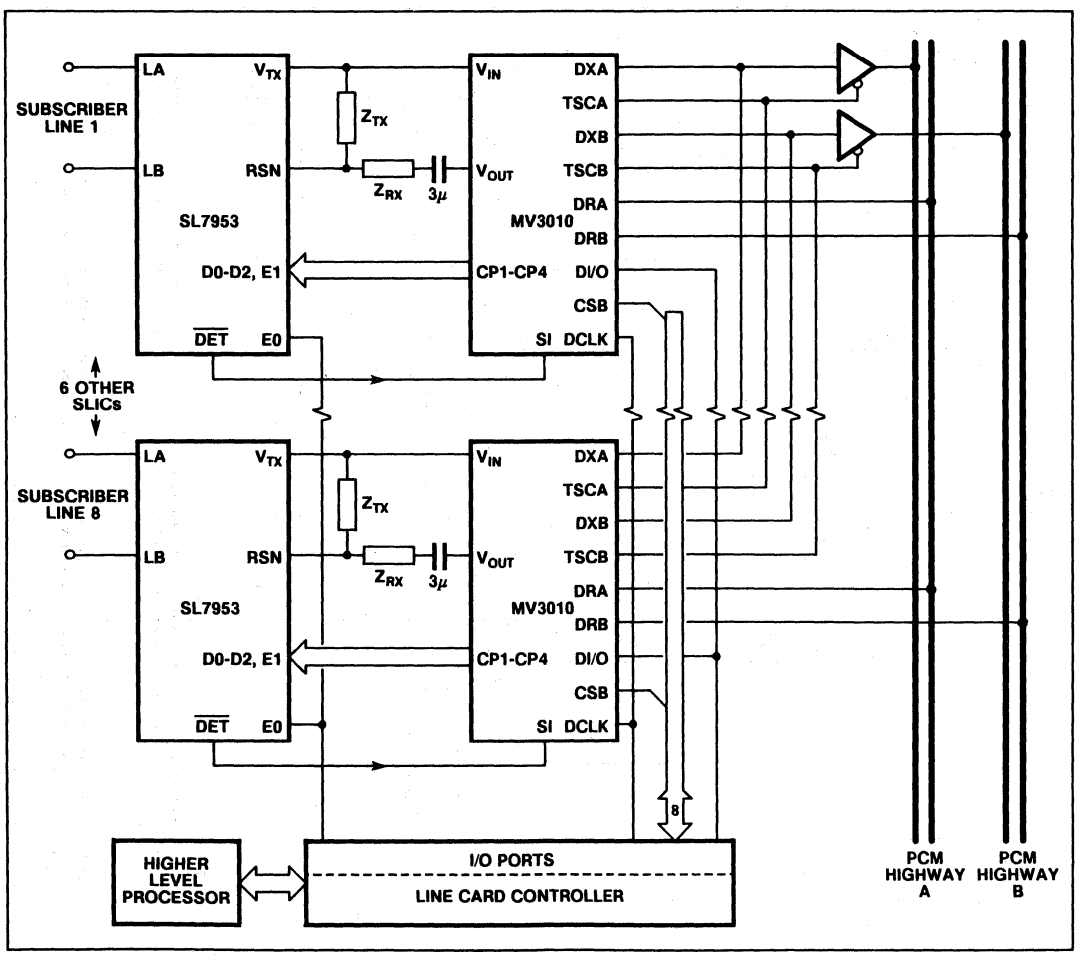


Fig.12a SLIC/PSLAC line interface card

Both the control and status pins are TTL compatible. They are designed to give a simple interface to digital circuits and are directly compatible with the GEC Plessey Semiconductors' MV3010 PSLAC (Plessey Subscriber Line Audio Circuit - see separate data).

The circuits of Fig. 12a and 12b show different ways of connecting the SLIC to the MV3010 to form an 8-channel subscriber line card architecture. For Fig. 12a, each PSLAC is controlled via a serial interface consisting of the common DI/O line, DCLK line and one of 8 $\overline{CS}$ lines. The PSLAC accepts/inputs data when the line card controller pulls the associated $\overline{CS}$ pin low and toggles DCLK (may be continuous). One of the control instructions of the PSLAC sets its CP1-CP5 I/O latches to outputs, whilst a further code writes data to each output. Four of these lines (CP1-CP4) are used to control the SLIC status (CP5 is not used). In addition to the output of data via CP1-CP4, a PSLAC control code monitors the status of the dedicated SI input. Consequently the line card controller gains access to the SLIC $\overline{DET}$ status via the PSLAC. Action to control the SLIC is then taken accordingly by the higher level processor that is controlling the line card.

Fig. 12b shows an optional interconnect to the SLIC, making use of the E0 control input. When this input is high, all 8 $\overline{DET}$ outputs can be read simultaneously, and the higher level software can then write to the necessary PSLAC associated with each low of the 8-bit port. This writing of data can be done simultaneously to those PSLACs required, by toggling DCLK and DI/O together with the selected $\overline{CS}$ inputs. Note that E0 must be set low to disable the $\overline{DET}$ outputs during this action, thus avoiding contention on this '$\overline{DET}$ bus'.

More data on the PSLAC device, interface circuitry and controller, can be found by reference to the MV3010 data and to Application Notes AN42, AN84, AN101, AN103, AN104 and AN111.

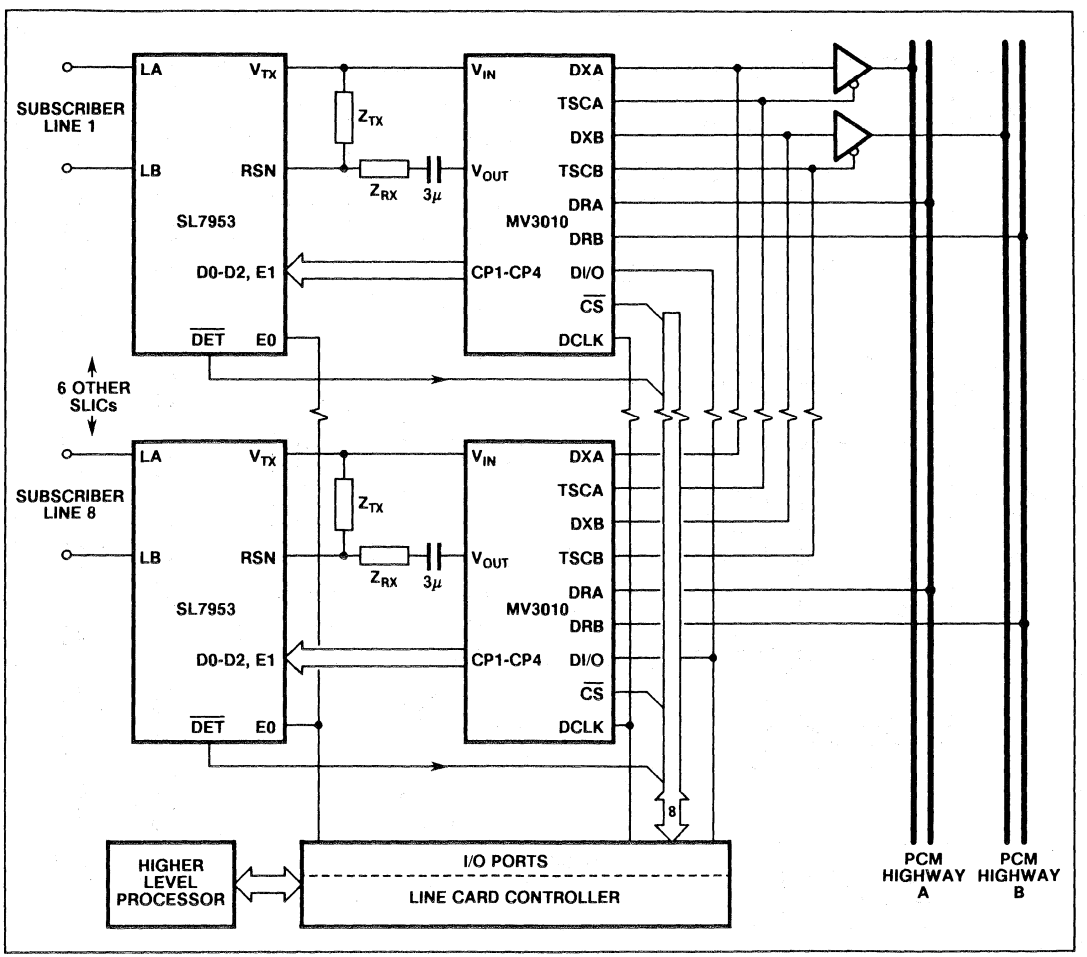


Fig.12b AlternativeSLIC/PSLAC line interface card

RING TRIP

Ring Trip detection operates by comparing the voltages on DA and DB and providing the output on $\overline{DET}$ when this function is enabled using the status input pins of the Digital Interface. A resistance bridge (R_{B1} to R_{B4}) must be connected to the line and to the ringing voltage sources to cause the differential voltage between DA and DB to change sign when the line resistance falls below the level associated with Ring Trip. Note that it is simplified by use of $R_{B1} = R_{B2}$ and $R_{B3} = R_{B4}$ (see discussion in AN82).

Ringing voltage is normally applied to the line through the ring relay which is activated via RINGR in Ringing Mode. The ringing voltage sources, including line feed, are connected via ringing feed resistors, R_{FEED1} and R_{FEED2}. The resistance bridge operates by allowing the DC voltage dropped across the ringing feed resistors in the Off-Hook condition to reverse the polarity of the voltage on DA and DB (DA < DB). Since the AC ringing voltage is greater than the DC feed, the capacitor C_B (Fig. 13) will filter this out at the comparator inputs. The connection shown is suitable for balanced ringing only. For unbalanced ringing, separate capacitors from DA (C_{B1}) and DB (C_{B2}) to ground will be required to achieve the same result.

Fig. 13 shows how the resistance bridge is connected when used with balanced ringing. The circuit can operate correctly provided there is a DC feed in addition to the AC ringing voltage.

If R_{LTH} is the line resistance corresponding to the Ring Trip threshold (DA = DB), this can be determined from the values of R_F ($R_{FEED1} = R_{FEED2} = R_F$), R_{B1} and R_{B4} ($R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$) as:-

$$R_{LTH} = \frac{R_{B4}(2\ R_F)}{(R_{B1} - R_{B4})}$$

R_{B1} and R_{B4} should be a few hundred kΩ.

The amplitude of the AC ringing voltage at DA (DB is by the same amount) is reduced by a factor of $(1 + 4\pi^2 f_r^2 t_r^2)^{-\frac{1}{2}}$ where f_r is the ringing AC frequency and t_r is set by:-

$$t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$$

for balanced ringing. For $f_r \approx 20$Hz, t_r should be ≈ 50ms. For unbalanced ringing C_B will become $C_{B1}C_{B2} \div (C_{B1} + C_{B2})$ in the above equation.

The circuit for balanced ringing is analysed in more detail in the SL373/SL376 Applications Note AN82, along with that for unbalanced operation. This information is also valid for the SL7953, since the Ring Trip Detection circuitry is the same for all devices.

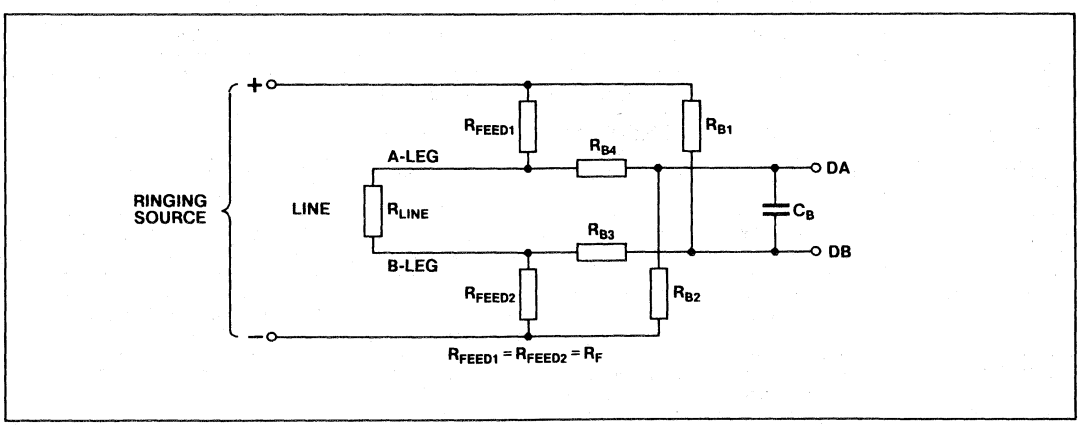


Fig. 13 Ring trip circuit

PIN DESCRIPTIONS Pin names for the Am7953 are shown thus: [XXX]; note that the functionality is identical.

Symbol	Pin no.	Pin name and description
BGND [BGND]	1	**Battery Ground (Power Input).** 0 Volts.
V_{REG} [V_{REG}]	2	**Regulated Voltage (Negative Power Input).** The voltage at this pin is compared to that required for line feed, and the result is used to control the voltage regulator.
V_{CC} [V_{CC}]	3	**Positive Supply (Power Input).** +5 Volts.
RINGR [RINGOUT]	4	**Ring Relay Driver Output, Transistor Emitter.** This output is designed to drive a relay, when used together with the V_{BAT} supply. The driver collector connects to the V_{CC} pin.
NC	5	**(No Connection)**
+CH [L]	6	**Switching Regulator (Chopper) Output (Negative Power Output).** Chopper switch transistor collector. An internal regulator controls the mark/space ratio of the switching waveform to maintain V_{REG} (pin 2) at the required voltage.
V_{BB} [V_{BAT}]	7	**Battery Voltage (Negative Power Input).** This is the negative voltage battery supply pin which connects to the V_{BAT} supply via an external diode. It is connected to the chopper switch emitter, and via an on-chip resistor to SUB.
SUB [Q_{BAT}]	8	**Quiet Battery, Substrate (Decoupling Node).** An external decoupling capacitor (0.33µF) should be connected between this pin and AGND. An internal resistor connects to V_{BB}.
CHS [CHS]	9	**Line Feed Regulator (Chopper) Stabilising Network.** This is the input to the voltage comparator which is used to control the switching regulator.
CHCLK [CHCLK]	10	**Line Feed Regulator (Chopper) Clock (Digital Input).** This is the external clock input for the voltage regulator. The frequency is 256kHz (nominal), triggered on the rising edge. The regulator will free run in the absence of an input signal.
E1 [E_1]	11	**Control Input (Digital Input).** Selects the line status detector (Loop or Ground Key).
E0 [E_0]	12	**Detector Data output Enable (Digital Input).** Enables the Detector data output pin ($\overline{DET}$).
$\overline{DET}$ [$\overline{DET}$]	13	**Detector Data output (Digital Output).** This pin outputs the status of the detector which has been selected by D0 - D2. It is enabled by the E0 pin.
D1 [C_2] D2 [C_3] D0 [C_1]	14 15 16	**Control Input (Digital Input).** **Control Input (Digital Input).** **Control Input (Digital Input).** These inputs determine the SLIC operating mode, and control the ring relay status, selection of ringing and non-ringing Modes, line polarity, line status and line detector.
R_{DC} [R_{DC}]	17	**DC Reference Voltage (Voltage Output).** A reference voltage of ±2.5Volts (±depending on line polarity), is output at this pin, excepting Saturation Guard operation.
AGND [AGND]	18	**Analog Ground (Analog Reference Node).** This is the ground reference pin for the analog signals. It also provides a ground reference for the Digital Interface. Signal reference and decoupling connections should be separately run to this pin.
RSN [RSN]	19	**Receive Summing Node (Current Input).** The current which is input on this pin is used to control the transverse current at LA and LB.
V_{EE} [V_{EE}]	20	**Negative Supply (Power Input).** –5 Volts.
V_{TX} [V_{TX}]	21	**Transmit Voltage (Voltage Output).** The voltage output at this pin is equal to the difference between the voltage (V_{LA}–V_{LB}) and the differential DC voltage (V_{HPA}–V_{HPB}), multiplied by the 2 to 4-wire voltage gain.
HPA [HPA] HPB [HPB]	22 23	**High Pass A, High Pass B - AC/DC separation (Voltage Inputs).** These inputs sense the DC feed voltages on the LA and LB pins respectively. Under normal operation they are connected to LA and LB respectively by internal resistors and should be connected as shown in Fig. 11.
RD [R_D]	24	**Loop Detection Control (Current Output / Voltage Input).** This pin outputs a current which equals the transverse loop current through LA and LB divided by 280. Off-Hook is indicated via the $\overline{DET}$ pin when the voltage at this pin is ≥(V_{EE} + 1.25) Volts.
DA [DA] DB [DB]	25 26	**Ring Trip Detector A, Ring Trip Detector B (Voltage Inputs).** These are the A and B inputs to the internal ring trip comparator. The output of the comparator controls the ring trip output on $\overline{DET}$.
LA [AX(TIPX)] LB [BX(RINGX)]	27 28	**A Line Transceiver, B Line Transceiver (Current Outputs / Voltage Inputs).** These two pins form the 2-wire port connecting to the subscriber loop.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Range - see page 3-127)

Test conditions (unless otherwise stated)

V_{CC} = +5.0V, V_{EE} = -5.0V, V_{BAT} = -50V (see note 1), $V_{AGND} = V_{BGND}$, T_{AMB} = +25°C, $V_{AGND} = V_{BGND}$, V_{IL} = 0.7V, V_{IH} = 2.0V and $Z_L = \infty\Omega$. Test circuit Fig. 26. Voltages are measured with respect to analog ground (V_{AGND}). Typical figures are for design aid only; they are not guaranteed and are not subject to production testing.

Supply Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply (V_{CC}) current, disconnect mode	I_{CC1}			4	mA	
Positive supply (V_{CC}) current, standby mode	I_{CC2}			10	mA	On / Off-Hook, $I_L = 0$
Positive supply (V_{CC}) current, active mode	I_{CC3}			10	mA	On / Off-Hook, $I_L = 0$
Negative supply (V_{EE}) current, disconnect mode	I_{EE1}			2	mA	
Negative supply (V_{EE}) current standby mode	I_{EE2}			3	mA	On / Off-Hook, $I_L = 0$
Negative supply (V_{EE}) current active mode	I_{EE3}			3	mA	On / Off-Hook, $I_L = 0$
Battery supply (V_{BB}) current disconnect mode	I_{BB1}			1	mA	
Battery supply (V_{BB}) current standby mode	I_{BB2}			5	mA	On-Hook, $I_L = 0$
Battery supply (V_{BB}) current active mode	I_{BB3}			6	mA	On-Hook, $I_L = 0$
Positive supply (V_{CC}) rejection ratio, supply to 2-wire transverse	P_{SRT}	20			dB	50mV on V_{CC} supply, 50-3400Hz, $Z_L \leq 600\Omega$,
Positive supply (V_{CC}) rejection ratio, supply to 2-wire longitudinal	P_{SRL}	17			dB	50mV on V_{CC} supply, 5kHz-3400Hz, $Z_L \leq 600\Omega$,
Negative supply (V_{EE}) rejection ratio, supply to 2-wire transverse	N_{SRT}	20			dB	50mV on V_{EE} supply, 50-3400Hz, $Z_L \leq 600\Omega$,
Negative supply (V_{EE}) rejection ratio, supply to 2-wire longitudinal	N_{SRH}	17			dB	50mV on V_{EE} supply, 5kHz-3400Hz, $Z_L \leq 600\Omega$,
Battery supply (V_{BB}) rejection ratio, supply to 2-wire transverse	B_{SRT}	20			dB	50mV on V_{BAT} supply, 50-3400Hz, $Z_L \leq 600\Omega$,
Battery supply (V_{BB}) rejection ratio, supply to 2-wire longitudinal	B_{SRL}	25			dB	50mV on V_{BAT} supply, 5kHz-3400Hz, $Z_L \leq 600\Omega$,
Power dissipation, active state	P_{WA1}		0.7	1.0	W	$Z_L = 0 - \infty\Omega$
Power dissipation, active state	P_{WA2}		0.3	0.425	W	$Z_L = \infty\Omega$
Power dissipation, standby state	P_{WD1}		0.18	0.3	W	On-Hook
Power dissipation, disconnect A standby B	P_{WD2}		0.05	0.14	W	

NOTE

1. The battery voltage V_{BAT} is generally defined. The corresponding V_{BB} voltage is assumed to be 0.7V more positive than V_{BAT} allowing for the diode drop in D_2, Fig. 25.

Analog Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
2-wire port, low freq overload level	V_{OAB}	- 3.1		+ 3.1	V (pk)	See Fig 14, note 2: E_R = 1000Hz, E_L = 0V, R1 = 600Ω, R4 = 0Ω
2-wire port, longitudinal impedance, off hook	Z_{LL1}		25	35	Ω/wire	See Fig 15: f < 100Hz Z_L = 600Ω
2-wire port, longitudinal impedance, on hook	Z_{LL2}		25	35	Ω/wire	See Fig 16: f < 100Hz Z_L = 600Ω
2-wire port, 2-wire return loss	RTL_2	35 25 20	38 28 22		dB dB dB	300-500Hz ,See Fig 14, note 4: 500-2500Hz, E_L = 0dBu (note 3), E_R = 0V, 2.5-3.4kHz, R1 = R4 = 300Ω
Longitudinal current limit, active state	ILL_A	17.5	25		mA/wire (rms)	See Fig 17, note 5: Z_L = 600Ω, E_R = - 10dBm 700-1100Hz
Longitudinal current limit, standby state	ILL_S	8.0	12		mA/wire (rms)	See Fig 17, note 5: Z_L = 600Ω E_R = - 10dBm 700-1100Hz
4-wire transmit port, overload level	V_{OT}	- 3.1		+ 3.1	V (pk)	See Fig 14, note 2: f = 1kHz 4-Wire Load ≥ 25kΩ, E_R = 0V, R1 = 600Ω, R4 = 0Ω
4-wire transmit port, offset voltage	V_{TOFF}	- 15		+ 15	mV	See Fig 14: E_R = 0V, E_L = 0V, R1 = 600Ω, R4 = 0Ω
4-wire transmit port,output impedance	Z_{TO}		3	10	Ω	See Fig 14: E_R = 0V, E_L = 0V, R1 = 600Ω, R4 = 0Ω
Transmit (2 to 4-wire) voltage gain	G_T	- 0.15		+ 0.15	dB	See Fig 14: E_R = 0V, E_L = 0dBu 1kHz, R1 = 600Ω, R4 = 0Ω
4-wire receive port, low impedance virtual earth input	Z_{RI}		1	20	Ω	Note 4
4-wire receive port, low frequency voltage gain	G_{R4}	- 0.15		+ 0.15	dB	See Fig 18: E_R = 2.6dBu 1kHz
4-wire receive port, current gain	G_{RI4}	59.8	60.0	60.2	dB	See Fig 14: R1 = 600Ω, R4 = 0Ω
4 to 4-wire voltage gain	$G_R \times G_T$	- 0.15		+ 0.15	dB	See Fig 14, note 4: E_L = 0V, R1 = 600Ω, R4 = 0Ω
2-wire to 4-wire frequency response	F_{24}	- 0.1		+ 0.1	dB	See Fig 14, notes 4 & 6: E_R = 0V, E_L = 0dBu 200-3400 Hz, R1 = 600Ω, R4 = 0Ω
4-wire to 2-wire frequency response	F_{42}	- 0.1		+ 0.1	dB	See Fig 14, notes 4 & 6: E_L = 0V, E_R = 0dBu 200-3400 Hz, R1 = 600Ω, R4 = 0Ω
4 to 4-wire frequency response	$F_{44} = F_{24} \times F_{42}$	- 0.1		+ 0.1	dB	Note 6
Gain linearity, 2-wire to 4-wire	G_{L24}	- 0.1		+ 0.1	dB	See Fig 14, notes 4 & 7: R1 = 600Ω, E_R = 0V, R4 = 0Ω, E_L = +7 to -55dBu 1kHz
Gain linearity, 4-wire to 2-wire	G_{L42}	- 0.1		+ 0.1	dB	See Fig 14, notes 4 & 7: R1 = 600Ω, R4 = 0Ω, E_L = 0V, E_R = +7 to -55dBu 1kHz
Gain linearity, 4-wire to 4-wire	G_{L44}	- 0.1		+ 0.1	dB	See Fig 14, notes 4 & 7: R1 = 600Ω, R4 = 0Ω, E_L = 0V, E_R = +3 to -45dBu 1kHz

NOTES
2. Overload occurs when distortion is 1% of total signal in the range 300-3400Hz.
3. dBu is defined thus : 0dBu is equivalent to the voltage at 0dBm when loaded with 600Ω (= 0.775V_{RMS}).
4. Not tested in production. Figures are guaranteed by characterisation.
5. E_{LL} = 50Hz. Amplitude is increased until signal-to-distortion ratio at V_T ≤ 20dB.
6. Response is measured with respect to 1kHz.
7. Linearity is measured with respect to gain at - 4dBu.

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
4-wire idle channel noise (psophometric weighted)	N_{P4}		– 77.0	– 75.0	dBup	See Fig. 14, note 8: $E_L = E_R = 0V$, R1 = 600Ω, R4 = 0Ω
2-wire idle channel noise (psophometric weighted)	N_{P2}		– 77.0	– 75.0	dBup	See Fig. 14, note 8: $E_L = E_R = 0V$, R1 = 600Ω, R4 = 0Ω
2-wire differential noise (wide band)	N_{D2}		Fig. 20			See Fig. 19, note 4
2-wire longitudinal noise (wide band)	N_{L2}		Fig. 21			See Fig. 19, note 4
Regulator noise, 4-wire transmit, single frequency	N_{R4}			– 55.0	dBu	See Fig. 19, note 4
Regulator noise, 2-wire transverse, single frequency	N_{RT}			– 50.0	dBu	See Fig. 19, note 4
Regulator noise, 2-wire longitudinal, single frequency	N_{RL}			– 50.0	dBu	See Fig. 19, note 4
Longitudinal balance, longitudinal to transverse	B_{L-T}	50	55		dB	See Fig. 15, note 8: $Z_L = 600Ω$, $E_R = 0$, E_{LL} = + 2dBu 300-3400 Hz
Longitudinal balance, longitudinal to 4-wire	B_{L-4}	50	55		dB	See Fig. 15, note 8: $Z_L = 600Ω$, $E_R = 0$, E_{LL} = + 2dBu 300-3400 Hz
Longitudinal balance, transverse to longitudinal	B_{T-L}	40	50		dB	See Fig. 22: $Z_L = 600Ω$, $E_R = 0$, E_{LL} = + 2dBu 300-3400 Hz
Longitudinal signal rejection, longitudinal to 4-wire	RJ_{L-4}	50	60		dB	See Fig. 15: $Z_L = 600Ω$, $E_R = 0$, E_{LL} = + 2dBu 300-3400 Hz
Longitudinal signal generation, 4-wire to longitudinal	GN_{4-L}	40	45		dB	See Fig. 23: $Z_L = 600Ω$, E_R = 2.6dBu f = 300-3400 Hz
Harmonic distortion, 4 to 2-wire	T_{HD1}		– 64	– 50	dB	E_R = 0dBu See Fig. 14, notes 9 & 10: R1 = 600Ω, R4 = 0Ω
Harmonic distortion, 2 to 4-wire	T_{HD2}		– 64	– 50	dB	E_L = 0dBu See Fig. 14, notes 9 & 10: R1 = 600Ω, R4 = 0Ω
Intermodulation distortion	ID_{A-B1}			– 40.0	dB	See Fig. 14, note 11: $E_R = f_1 + f_2$, $f_1 = f_2$ = – 1 to – 21dBu, R1 = 600Ω, R4 = 0Ω
50Hz intermodulation distortion	ID_{A-B2}			– 49.0	dB	See Fig 14, notes 4 & 12: $E_R = f_1 + f_2$, f_1 = – 9dBu 300-3400 Hz, f_2 = – 23dBu 50 Hz.
Loop current, active state, constant current region	I_{ACT1}	38	40	42	mA	See note 13: $Z_L = 600Ω$, $R_{DC} = 62.5kΩ$
Loop current, active state	I_{ACT2}	16.5			mA	See note 13: $Z_L = 1800Ω$, $R_{DC} = 62.5kΩ$
Loop current, standby state, normal or reversed polarity	I_{LIM}	10	11.4	12.8	mA	See note 14; $Z_L = 600Ω$
2-wire current, disconnected state	I_{DCT}			1.0	mA	LA to LB or ground, or both LA and LB to ground

NOTES
8. This parameter will degrade when the saturation guard is active i.e. $|V_{BAT}|-|V_{DCT}| < 15.0V$ (V_{SG}).
9. Distortion measured in the bandwidth 300-3400 Hz.
10. Measured at 1kHz in production; other frequencies guaranteed by characterisation.
11. f_1 & f_2 in the range 300-3400Hz, $f_1 \div f_2$ = Non-integer. Measure $(2f_1-f_2)$ relative to f_1 or f_2 level.
12. Measure $(2f_1-f_2)$ relative to f_1 or f_2 level.
13. Applied $V_{BAT} = -63V$.
14. Constant current in standby mode is approximately 600 + R_{TH}.

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
2-wire current, disconnect A standby B mode	I_{DASB}			1.0	mA	$Z_L = 600\Omega$
Loop detector, current threshold	I_{TH}	$I_{TH} - 20\%$	I_{TH}	$I_{TH} + 20\%$	A	$I_{TH} = 350 \div R_{TH}$
Ring trip detector offset voltage	V_{RTO}	– 50		+ 50	mV	See Fig. 24 : $R = 200k\Omega$ $V_{BB} < V_{CMM} < -2V$
Ring trip detector bias current	I_{RTB}	–1.0			µA	See Fig. 24 : $I_{RTB} = \frac{1}{2}(I_{RTDA} + I_{RTDB})$
Ground key active mode $\overline{DET} = 0$	R_{G10}	900			Ω	See Fig. 25, notes 15 and 16: SW1 closed, RW = 300Ω
Ground key active mode $\overline{DET} = 1$	R_{G11}			10	kΩ	See Fig. 25, notes 15 and 16: SW1 closed, RW = 300Ω
Earthcall active mode $\overline{DET} = 0$	R_{G20}	1.7			kΩ	See Fig. 25, notes 15 and 16: SW1 open, RW = 300Ω
Earthcall active mode $\overline{DET} = 1$	R_{G21}			10	kΩ	See Fig. 25, notes 15 and 16: SW1 open, RW = 0Ω
Earthcall disconnect A standby B mode, $\overline{DET} = 0$	R_{G30}	1.7			kΩ	See Fig. 25, notes 15 and 16: SW1 open, RW = 300Ω
Earthcall disconnect A standby B mode, $\overline{DET} = 1$	R_{G31}			10	kΩ	See Fig. 25, notes 15 and 16: SW1 open, RW = 0Ω
Relay driver, saturation voltage (active)	V_{SAT}	$V_{CC} - 2.0$	$V_{CC} - 1.6$		V	I = 25mA drawn from pin
Relay driver, leakage current (non-active)	I_{LK}			0.1	mA	V_{OUT} = Voltage at pin 8
Relay driver, clamp voltage	V_{CLMP}	$V_{BAT} - 3.0$			V	I = 25mA into pin

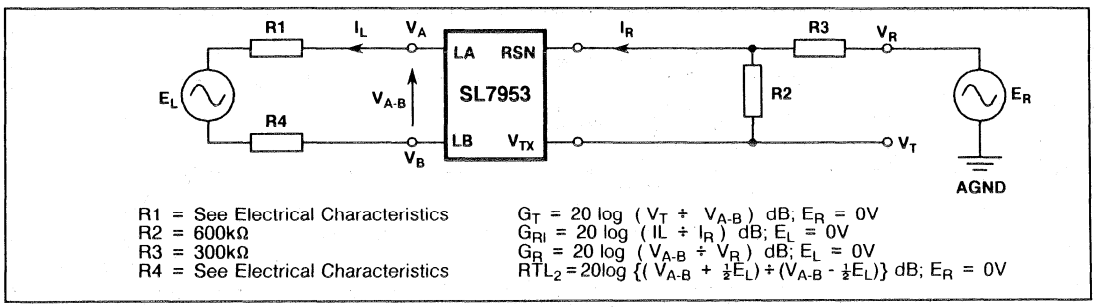
NOTES
15. For polarity reversed state, connections to LA and LB are reversed.
16. 'Must detect' and 'Must not detect' are indicated in the min. and max. columns respectively.

Digital Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Input low voltage (D0-D2,E0,E1,CHCLK)	V_{IL}			0.8	V	
Input high voltage (D0-D2,E0,E1,CHCLK)	V_{IH}	2.0			V	
Input low current (D0-D2,E0,E1,CHCLK)	I_{IL}			– 0.25	mA	$V_{IL} = 0.4V$
Input high current (D0-D2,E0,E1,CHCLK)	I_{IH}			0.04	mA	$V_{IH} = 2.4V$
$\overline{DET}$ output low voltage	V_{OL}			0.4	V	$I_{OL} = 0.8mA$
$\overline{DET}$ output high voltage	V_{OH}	2.4			V	$I_{OH} = 0.1mA$
$\overline{DET}$ output, internal pull-up	R_{OUT}	10		20	kΩ	
Propagation delay, E1 to $\overline{DET}$	t_{PD}			4	µs	$\overline{DET}$ 6.2kΩ to V_{CC}, 15pF to BGND
Loop detector make response time	t_{LM}			3	ms	$Z_L = 2k\Omega$
Loop Detector break response time	t_{LB}			3	ms	$Z_L = 2k\Omega$
CHCLK input frequency	F_{CLK}		256		kHz	
CHCLK min. pulse width	T_{CLK}		500		ns	

Recommended Operating Range

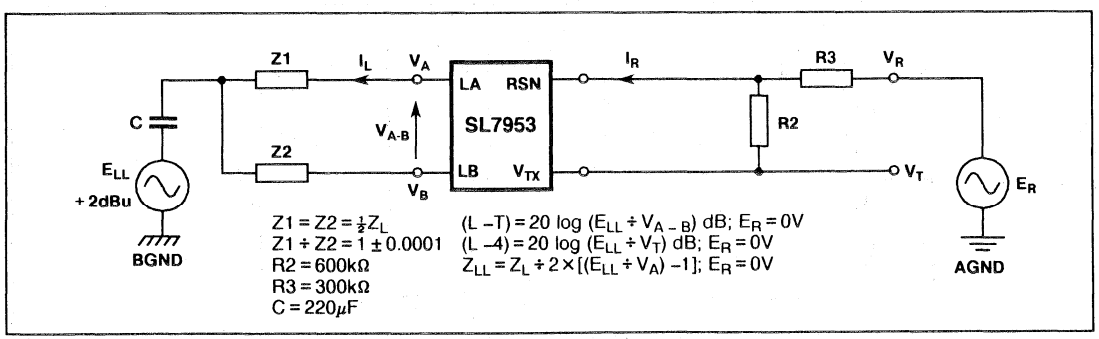
Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply voltage	V_{CC}	4.75	5.0	5.25	V	
Negative supply voltage	V_{EE}	– 4.75	– 5.0	– 5.25	V	
Battery supply voltage	V_{BAT}	– 40.5	– 48	– 64	V	
Battery ground voltage	V_{BGND}	– 0.1		+ 0.1	V	
Ambient temperature	T_{AMB}	0		70	°C	



R1 = See Electrical Characteristics
R2 = 600kΩ
R3 = 300kΩ
R4 = See Electrical Characteristics

$G_T = 20 \log (V_T \div V_{A-B})$ dB; $E_R = 0V$
$G_{RI} = 20 \log (I_L \div I_R)$ dB; $E_L = 0V$
$G_R = 20 \log (V_{A-B} \div V_R)$ dB; $E_L = 0V$
$RTL_2 = 20\log \{(V_{A-B} + \frac{1}{2}E_L) \div (V_{A-B} - \frac{1}{2}E_L)\}$ dB; $E_R = 0V$

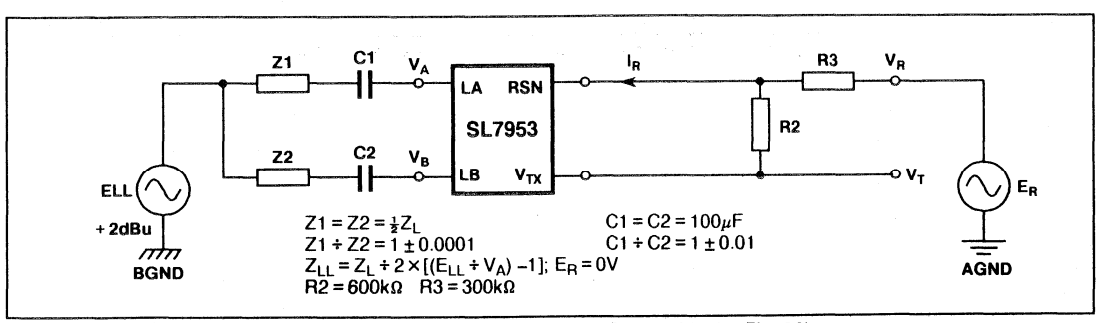
Fig.14 Test configuration (Note the SL7953 block = Fig. 26).



$Z1 = Z2 = \frac{1}{2}Z_L$
$Z1 \div Z2 = 1 \pm 0.0001$
R2 = 600kΩ
R3 = 300kΩ
C = 220μF

$(L-T) = 20 \log (E_{LL} \div V_{A-B})$ dB; $E_R = 0V$
$(L-4) = 20 \log (E_{LL} \div V_T)$ dB; $E_R = 0V$
$Z_{LL} = Z_L \div 2 \times [(E_{LL} \div V_A) - 1]$; $E_R = 0V$

Fig.15 Test configuration (Note the SL7953 block = Fig. 26).



$Z1 = Z2 = \frac{1}{2}Z_L$
$Z1 \div Z2 = 1 \pm 0.0001$
$Z_{LL} = Z_L \div 2 \times [(E_{LL} \div V_A) - 1]$; $E_R = 0V$
R2 = 600kΩ R3 = 300kΩ

C1 = C2 = 100μF
$C1 \div C2 = 1 \pm 0.01$

Fig.16 Test configuration (Note the SL7953 block = Fig. 26).

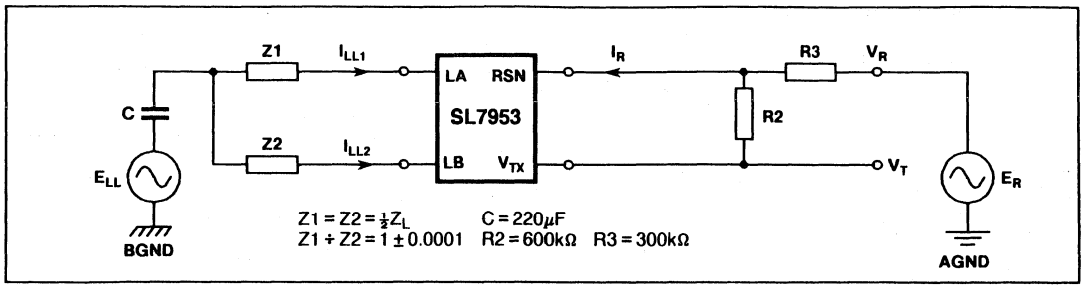


Fig.17 Test configuration (Note the SL7953 block = Fig. 26).

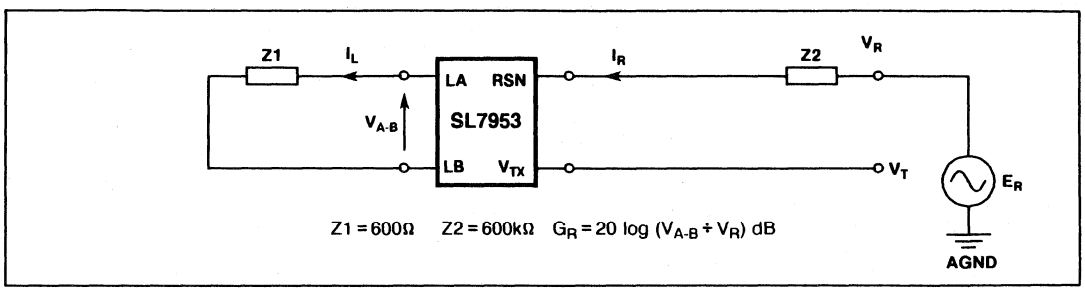


Fig.18 Test configuration (Note the SL7953 block = Fig. 26)

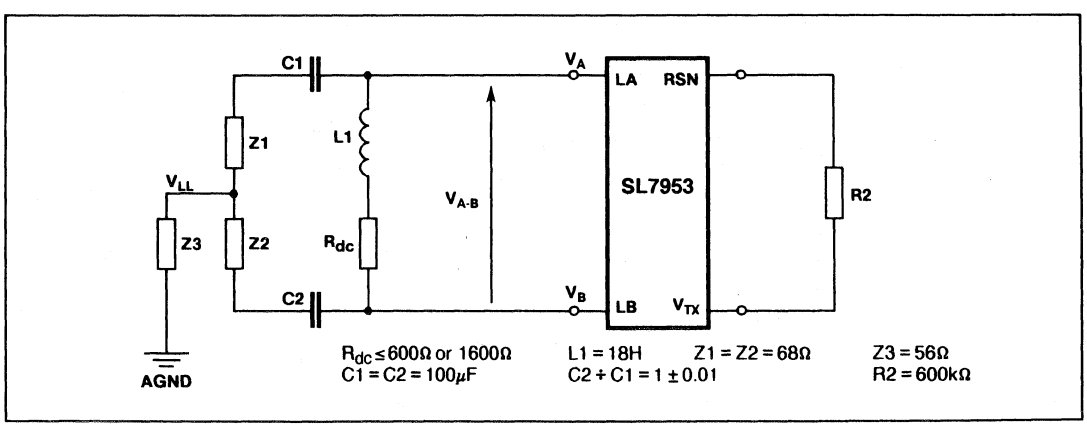
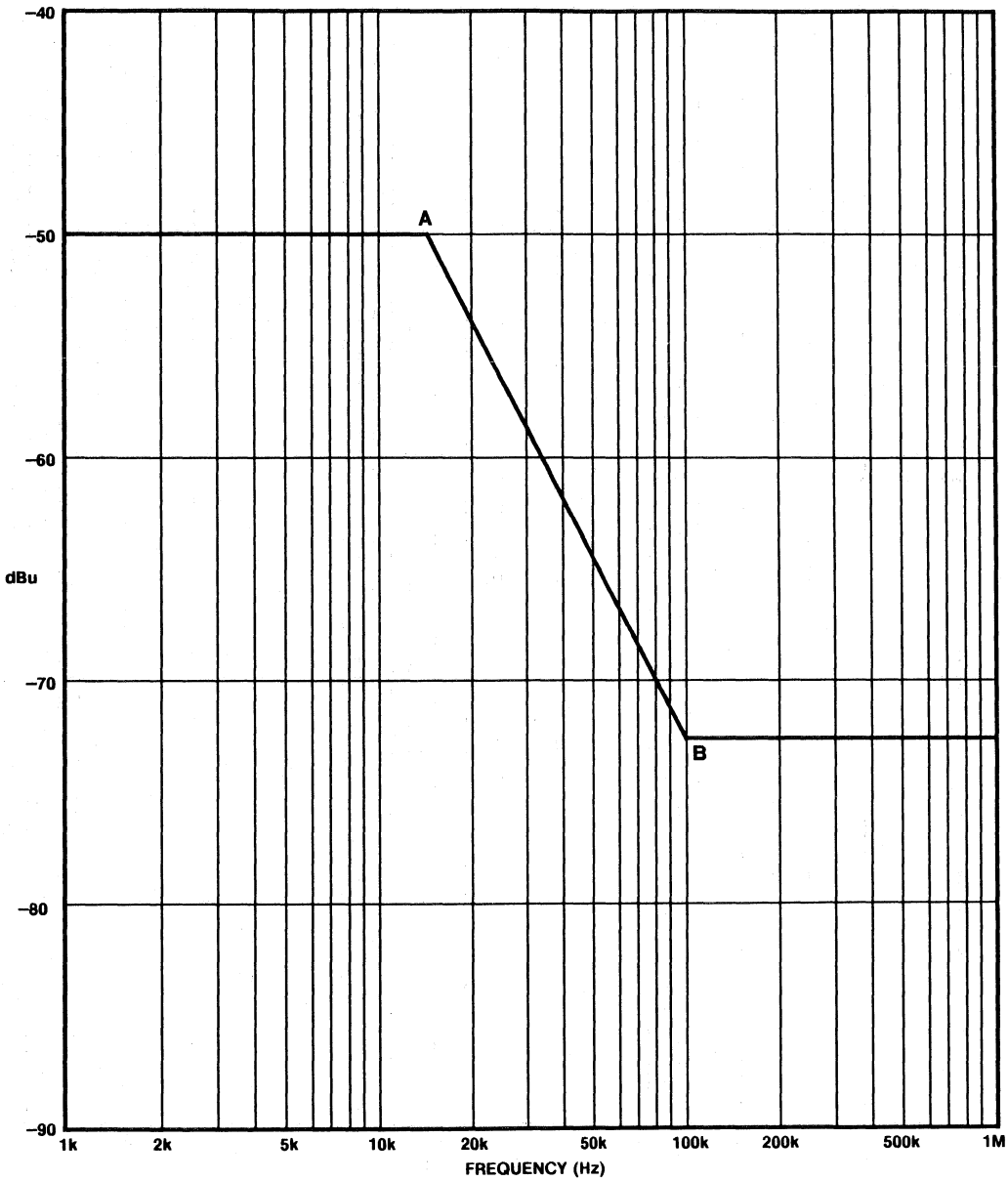


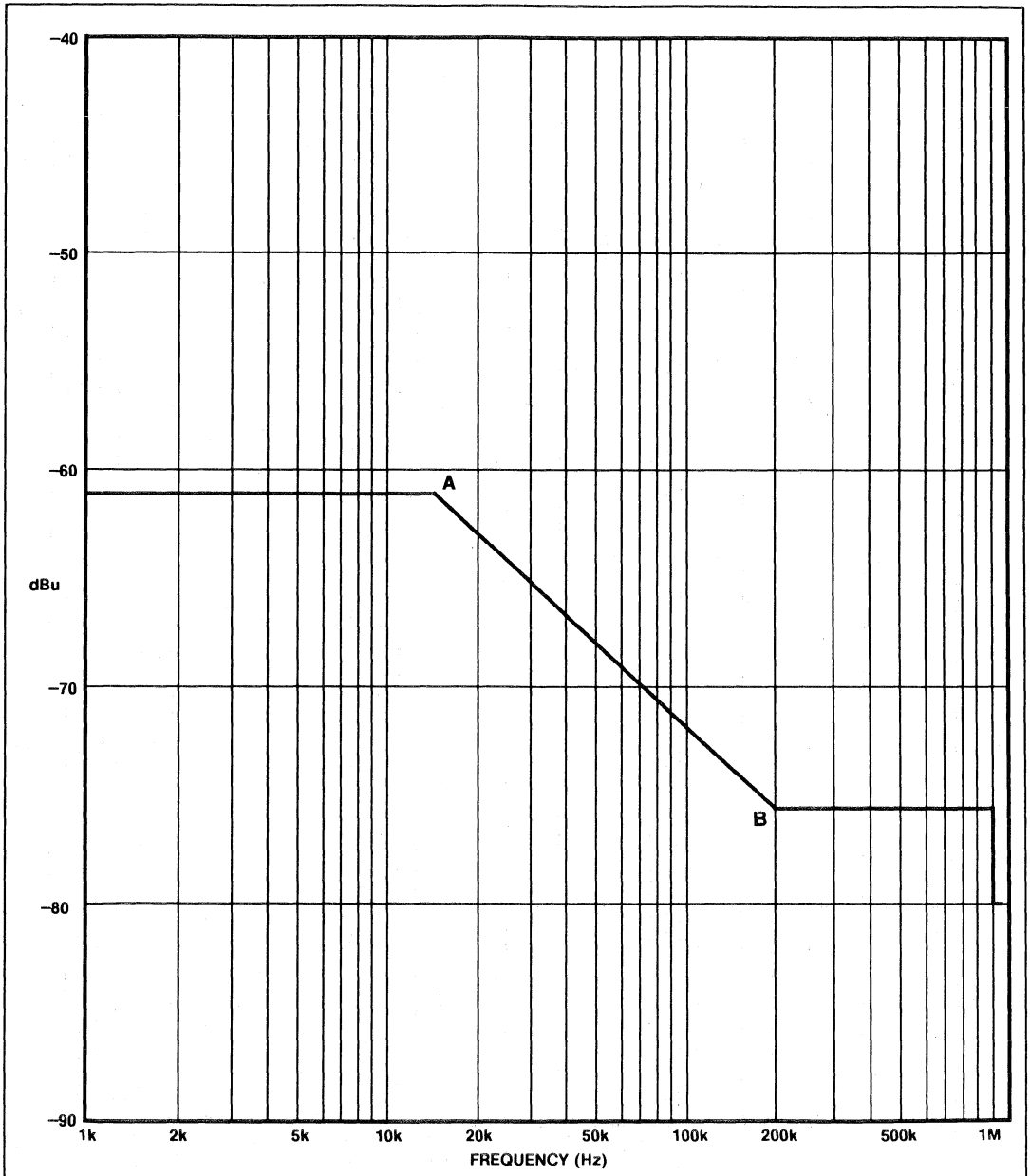
Fig.19 Test configuration (Note the SL7953 block = Fig. 26).



FREQUENCY AT CENTRE OF BAND

A = 15kHz –50dBu
B = 100kHz –73dBu
Bandwidth = 3kHz Minimum Centre Frequency = 1.6kHz
V_{A-B} < –73dBu. f > 1MHz

Fig.20 2-Wire differential noise



FREQUENCY AT CENTRE OF BAND

A = 15kHz –61dBu
B = 200kHz –75dBu
Bandwidth = 3kHz
V_{LL} < –80dBu. f >1MHz

Fig.21 2-Wire longitudinal noise

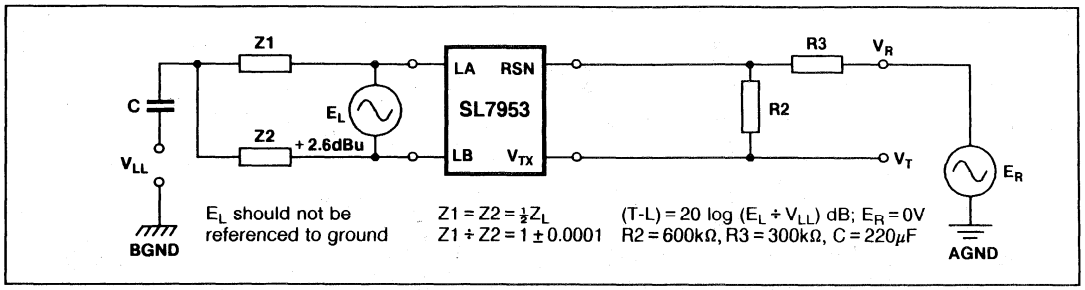


Fig.22 Test configuration (Note the SL7953 block = Fig. 26)

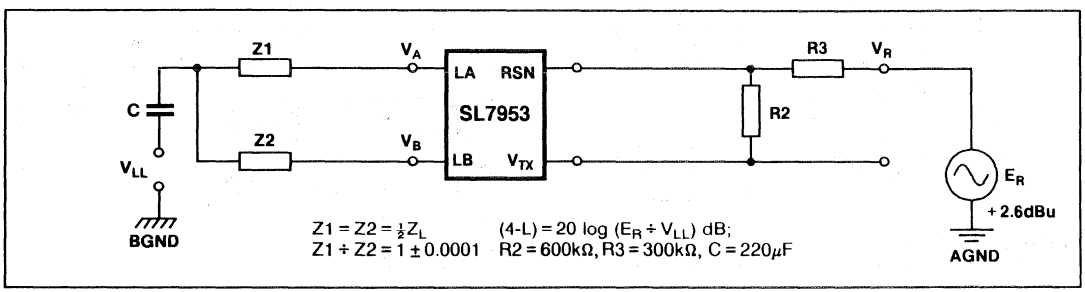


Fig.23 Test configuration (Note the SL7953 block = Fig. 26).

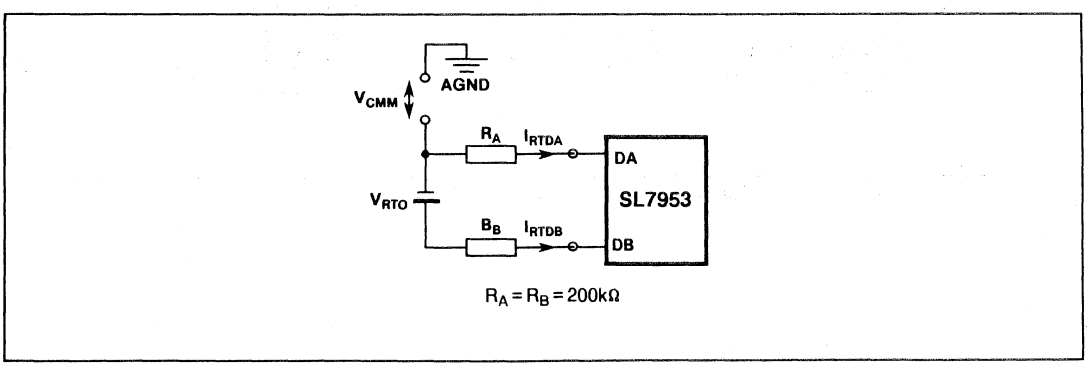


Fig.24 Test configuration (Note the SL7953 block = Fig. 26).

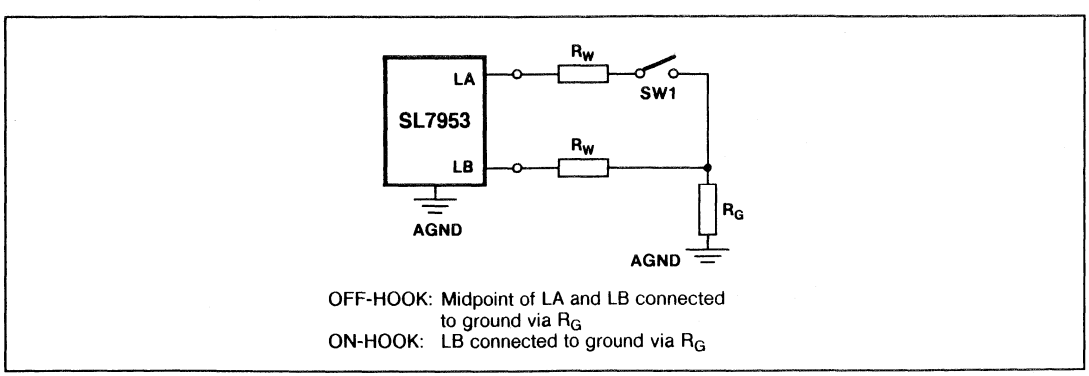
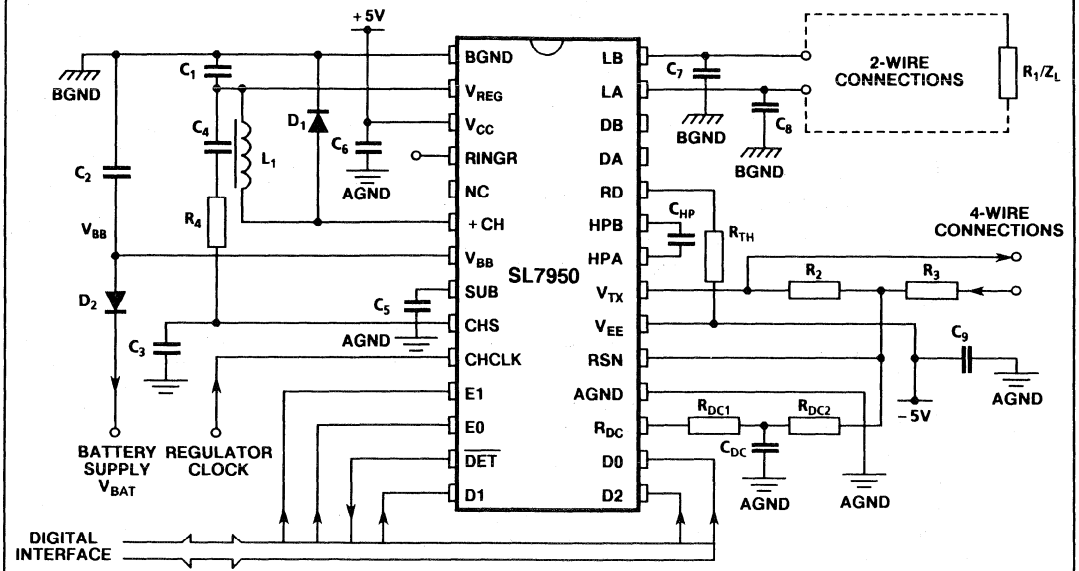


Fig.25 Test configuration (Note the SL7953 block = Fig. 26).



C_1 = 470n	C_6 = 100n	C_{DC} = 100n	R_{TH} = 56kΩ
C_2 = 470n	C_7 = 2.2n	D_1 = 100V,100mA	$R_{DC1} = R_{DC2} = \frac{1}{2}R_{DC}$ = 31.25kΩ
C_3 = 560p	C_8 = 2.2n	D_2 = 100V,100mA	R_1, R_2, R_3 as Test Configuration
C_4 = 8.2n	C_9 = 100n	L_1 = 1mH	Z_L: See Electrical Characteristics
C_5 = 330n	C_{HP} = 330n	R_4 = 2.4kΩ	

For all tests assume AGND = BGND.

Fig.26 Test circuit for Figs. 14-19 and 22-25

ABSOLUTE MAXIMUM RATINGS* - Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value		Units
		Min.	Max.	
Battery supply voltage	V_{BB}	– 70	+0.4	V
Battery voltage, rate of change (C5 Fig. 26 = 330n)	V_{BBR}	– 0.4	+0.4	V/µs
Continuous battery ground voltage	V_{BGNDC}	– 2.0	+2.0	V
Positive supply voltage	V_{CC}	– 0.4	+7.0	V
Negative supply voltage	V_{EE}	– 7.0	+0.4	V
Subscriber line voltage on LA, LB or both, continuous	V_{LC}	– 70.0	+1.0	V
Subscriber line voltage on LA, LB or both, 10ms duration, f = 0.1 Hz rate	V_{LR1}	–70	+5.0	V
Subscriber line voltage on LA, LB or both, 1µs duration, f = 0.1 Hz rate	V_{LR2}	–90	+10.0	V
Subscriber line voltage on LA, LB or both, 250ns duration, f = 0.1 Hz rate	V_{LR3}	–120	+15.0	V
Switched regulator voltage (off)	V_{CH}	V_{BB}	+1.0	V
Switched regulator current (on)	I_{CH}		150	mA
RINGR relay driver voltage	V_{RLY}	V_{BAT}	V_{CC}	V
Relay source current	I_{RING}		60	mA
Ring-Trip input voltage (DA or DB)	V_{RT}	V_{BB}	0	V
Ring-Trip input current (DA or DB)	I_{RT}		±2	mA
Digital input voltage	V_{ID}	– 0.4	V_{CC}	V
Digital input current (sink)	I_{ID}		– 5.0	mA
Digital output voltage	V_{OD}	– 0.3	V_{CC}	V
Digital output current (source)	I_{OD}		3	mA
Storage temperature	T_{ST}	– 55	+ 150	°C
Operating junction temperature †	T_{JOP}		+ 150	°C
Package power dissipation (DG28)	P_{PDG28}		1.5	W

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

† Circuit includes thermal protection such that T_{PROT} (Min) = 140°C.

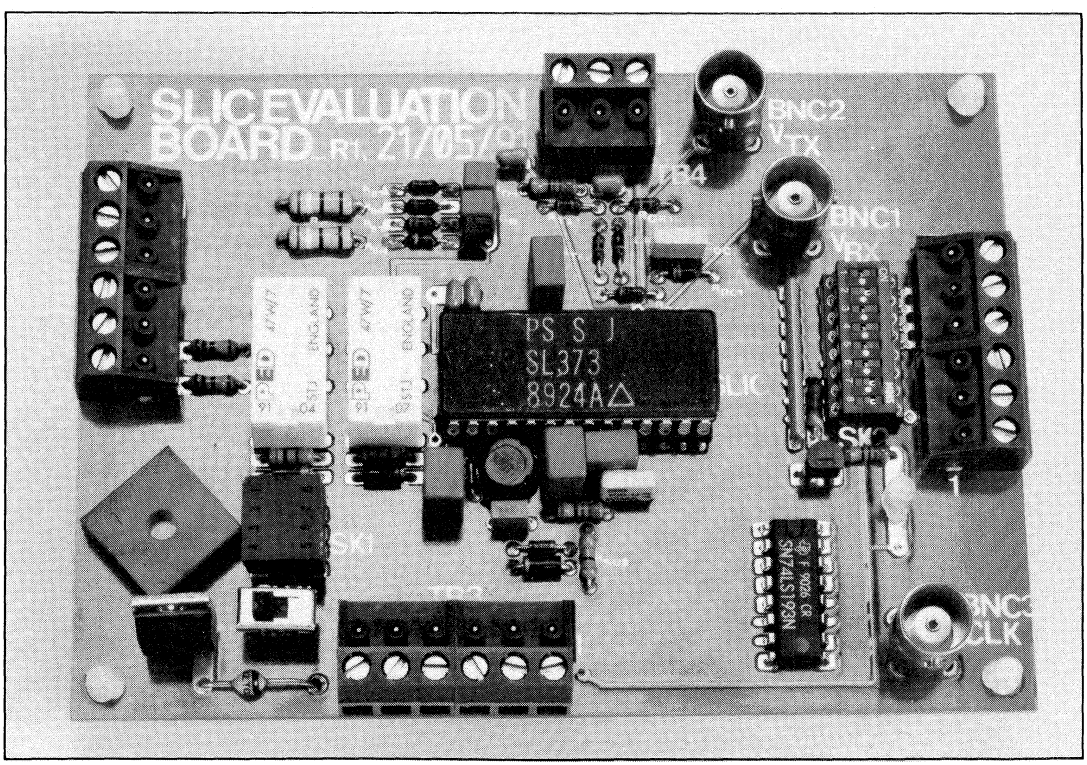
PCBAN114

A UNIVERSAL SLIC EVALUATION BOARD

Now available from GPS is the PCBAN114 printed circuit board which can be used to evaluate any one of the range of Subscriber Line Interface Circuits (SLICs). The design of the board allows customisation for the chosen SLIC by selecting appropriate component values. For more details of the board and how to incorporate the required SLIC, reference should be made to Applications Note AN114. This also shows how it can be interfaced to the PSLAC (Plessey Subscriber Line Audio Circuit) Evaluation Package PCBAN111 to facilitate development of a complete Line Card circuit design.

FEATURES

- May Be Used For Any One of the Range of SLICs, i.e. the SL373, SL374, SL376, SL7950 or SL7953.
- Selectable On-Board or Off-Board Digital Control of SLIC Status.
- Hardware Programmable 2-Wire Impedance and Receive Gain via On Board Component Values.
- Hardware Programmable Off-Hook and Ring Trip Detector Thresholds via On-Board Component Values.
- Caters For all Types of On-Chip SLIC Relay Driver via a PCB Header.
- Selectable Input Clock Frequency for the SLIC Regulator Circuit.
- Optional Overvoltage Protection Components Footprint on the PCB.
- Interfaces Directly to the PCBAN111 PSLAC Evaluation Package.
- Applications Note AN114 fully Describes the Operation and Uses of the Evaluation Board.



The universal SLIC evaluation board.

MV3010

SUBSCRIBER LINE AUDIO CIRCUIT

The MV3010 is a Subscriber Line Audio Circuit (SLAC) for use in subscriber line cards in telephone exchanges or similar equipment.

It performs A/D and D/A conversion, adjusts the gain and frequency response for both the transmit and receive paths and performs echo suppression by automatically cancelling any content of the receive signal from the transmit path. The device also allows line card control and monitoring facilities via digital I/O pins. High performance is ensured through the use of DSP techniques implemented in CMOS technology.

The MV3010 meets or betters all CCITT G.714 specifications over a range of programmable gains to 13dB.

The adaptive echo cancellation algorithm used ensures completely robust performance to a complete range of likely near and far end signal sources.

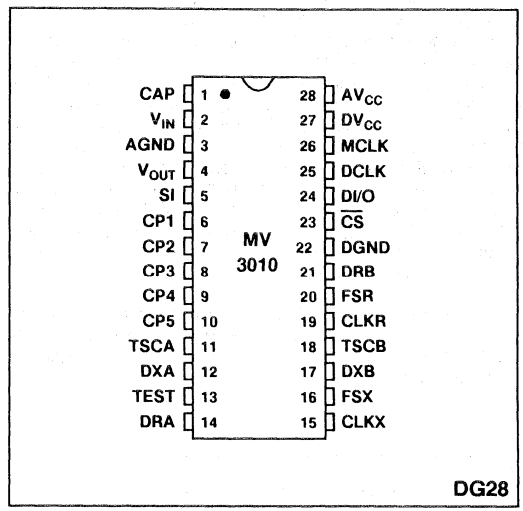


Fig.1 MV3010 Pin connections - top view.

FEATURES

- Adaptive Echo Cancellation (Hybrid Balance).
- Programmable Filters and Gain Control.
- Selectable for μ-Law, A-Law or Linear Codes.
- Programmable Line Control Interface.
- Programmable Time Slot and Clock Offset Assignments.
- Power Down Mode - Low Standby Power.
- On-chip Reference Voltage.
- Meets/betters CCITT and AT&T Specifications
- 2048kHz and 1544kHz PCM operation.

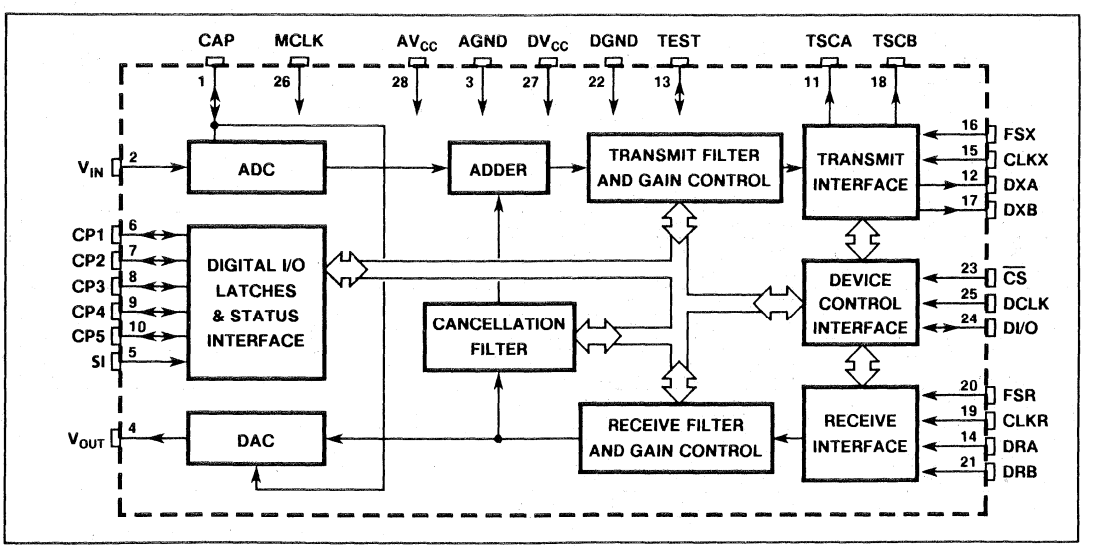


Fig. 2 Functional block diagram

FUNCTIONAL DESCRIPTION

OVERVIEW

The MV3010 Plessey Subscriber Line Audio Circuit (PSLAC) performs the coding, decoding, filtering, echo cancellation and line supervision functions which are required for the subscriber line interface in a digital PABX or Central Office. It can be easily interfaced with any of the SL37X or SL79XX Subscriber Line Interface Circuits (SLIC) to provide a complete subscriber line interface/line card, supporting all of the BORSCHT functions.

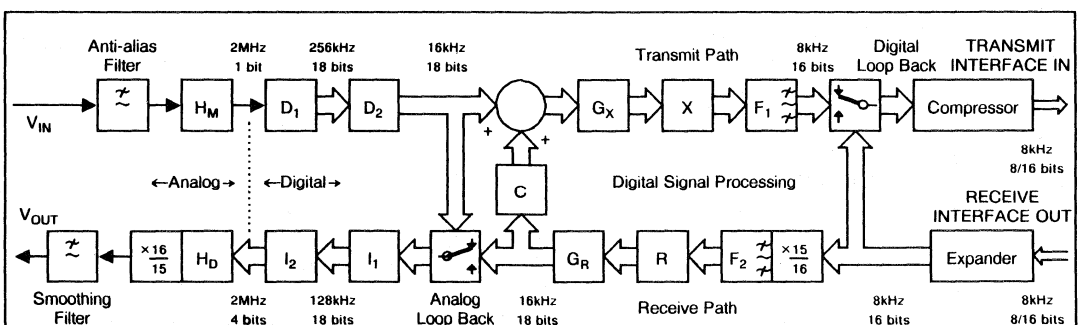
The PSLAC (Fig 2) samples the signal at VIN, pin 2, and provides companded or linear coded PCM samples, depending on programming (see Control and Monitoring section), at the DXA or DXB output pins. This is refered to as the Transmit direction. The Receive direction performs the opposite conversion, taking companded or linear PCM samples from the DRA or DRB pin and providing an analog signal at V_{OUT}, pin 4. For both of the Transmit and Receive directions, the overall gain, frequency response, clock rate and PCM time slot assignment can be dynamically adjusted by virtue of the DSP structure of the PSLAC. Also included is an automatically adaptive/static Trans-Hybrid filter (C Filter) for cancellation of any V_{OUT} signal present at the V_{IN} pin.

The serial Device Control Interface provides complete control and monitoring for all the PSLAC operating modes and functions, which are now described in more detail in the following sections.

RECEIVE PATH

PCM encoded signals are received on either the DRA pin or the DRB pin, depending on programming (see Control and Monitoring section). Bit and frame synchronisation are established by the CLKR clock and FSR pulse as described in the PCM Interface section, but will always consist of PCM samples at a basic 8kHz rate. Thus the PCM interface passes 16 bit, 8kHz samples into the receive path of the PSLAC DSP, as shown in figure 3. PCM samples are first expanded from A-Law or μ-Law, if necessary, before being passed through CCITT/AT&T filters, F_2. At this point samples may be switched into the transmit path to provide digital loop back (see Control and Monitoring section). Data is now interpolated from 16 to 18 bit samples running at 16kHz for the internal DSP, which now introduces an optional programmable Receive Filter, R. A 15/16 gain factor compensates for the D/A gain to restore a nominal receive gain of 0dB.

The Receive Filter is a 4 tap FIR type structure (16kHz taps) and can be used to modify the frequency response of the receive path. This might be used to adjust the overall frequency response, that may be affected by components of the external analog circuitry (e.g. 2 to 4 wire conversion) associated with V_{OUT}. Dynamic programming and enable/disable of the filter can be achieved via the Control Interface. Note that disabling of the filter does not alter the programmed coefficients, which may be entered when the filter is in either state. This filter is described more fully in the Transmit and Receive Filters section.



FUNCTION	NAME	DESCRIPTION
A/D Conversion	H_M	A/D Conversion to 2MHz 1 bit
Decimation Filters	D_1	Triangularly Weighted FIR 2MHz→256kHz
Decimation Filters	D_2	'Imperial college' 256kHz→16kHz
Transmit Gain adjust	G_X	One Tap FIR, -∞ to +15.6dB, user programmable
Transmit Filter	X	Four Tap FIR, user programmable
CCITT/AT&T Filters	F_1	'Imperial college' - Decimation 16kHz→8kHz, 4kHz low pass, 50/60Hz Notch and DC reject Filters
CCITT/AT&T Filters	F_2	'Imperial college' - Interpolation 8kHz→16kHz, 4kHz low pass Filter and DC reject Filter
Receive Filter	R	Four Tap FIR, user programmable
Receive Gain adjust	G_R	One Tap FIR, -∞ to +6dB, user programmable
Cancellation Filter	C	9 Tap FIR + 10th TAP IIR - Adaptive, user programmable
Interpolation Filters	I_1	'Imperial college' 16kHz→128kHz
Interpolation Filters	I_2	Sample/Hold 128kHz→2MHz
D/A Conversion	H_D	D/A Conversion and multiply by 16/15

Fig. 3 PSLAC Signal Processing Flow.

Following the Receive Filter is a gain stage (G_R) which can be used to adjust the overall Receive Gain of the receive path. Note that it does not have any other effect on the receive signal (frequency response or phase) other than an absolute adjustment of gain. G_R is set to 0dB (×1.0) at first application of power to the device, and can be dynamically programmed via the Control Interface. Coefficient values to adjust the Receive Gain in steps of 0.5dB are given in Table 1, and described further for other increments in Table 9.

At this point, the samples are fed in two separate directions. Firstly, they are passed to the C Filter for echo cancellation (Trans-Hybrid balance) in the Transmit Path, and secondly to the Interpolation Filters I_1 and I_2.

The C Filter is a 9 Tap FIR type filter (16kHz) plus a 10th Tap recursive IIR stage, and is described more fully in the C Filter section. It can be enabled and disabled in the same way as for the Transmit/Receive Filters, via the Control Interface. Additionally it has an adaptive mode to self adjust the cancellation according to changing conditions of the 4 wire interface (see C Filter section).

The internal sample format of 18 bits, 16kHz, is interpolated to 4 bit, 2MHz, in two stages by I_1 and I_2. Alternatively, samples may be switched in from the transmit path, to I_1, providing an Analog Loop Back mode (see Control and Monitoring section). D/A conversion, H_D introduces a gain of 16/15. The smoothing filter reduces noise and signal harmonics resulting in an output at VOUT (pin 4) of up to 3V p-p (+1.5/–1.5) biased at a DC level of V_{OO} (≈2.5V). The DC level is a consequence of the single (split analog and digital rails) +5.0V supply. The output stage, shown in figure 4a, can be coupled to a SLIC or other line interface circuitry. This is discussed further in the Applications section.

TRANSMIT PATH

The Transmit path, figure 3, begins at the VIN pin (pin 2). Analog input can be up to 6Vp-p about ground (+3.0V/–3.0V) despite the single +5.0V supply. The input stage is shown in figure 4b. Note that when left open circuit, the VIN pin biases to ≈1.66V. To maintain dynamic range of the input, the driving output should therefore have a low output impedance, to restore a ground centre point (removal of any DC bias at VIN is also necessary to prevent disabling of C Filter adaption - see separate section). The signal is now digitised using an over-sampling technique running at 1 bit, 2MHz, before being passed to the decimation stages D_1 and D_2. An anti-alias filter prevents harmonics above the sample rate from being aliased back down into the pass band.

Decimation stages D_1 and D_2 produce an 18 bit, 16kHz, sample rate for internal use by the PSLAC DSP, as for the Receive Path. Output from D_2 can be switched into the receive path to provide an Analog Loop Back function (see Control and Monitoring section). After this stage, samples from the Receive Path are added, via the C Filter, into the Transmit path. This is because in the intended application of a high quality Line Card/COMBO device, the analog input may contain some of the analog output of the PSLAC, due to the echo return of the 2 to 4/4 to 2 wire conversion (performed externally to the PSLAC). Any such content of the received signal is now attenuated by this added signal. Such use of the C Filter is described in more detail in later sections.

Following this, the Transmit signal now passes through three stages that act in a similar manner to that of the Receive side. Firstly a gain stage, G_X, provides overall adjustment of the Transmit Gain. This can be carried out in 0.5dB steps, as given in Table 1, or given other values as shown in Table 9.

Secondly, the samples now pass through a 4 Tap FIR Filter section (X) which is identical in form to the R Filter of the Receive side. The X Filter can be used to correct for phase/frequency errors in the Transmit Path, is dynamically programmable and can be disabled/enabled as for the R Filter.

Lastly, the 18 bit, 16kHz, samples are now decimated further to 8kHz by the F1 stage which provides CCITT/AT&T filters, in addition to 50/60Hz and DC reject filtering, which may be disabled via the Control Interface.

Before being passed to the PCM interface for output, the signal may be compressed to 8 bit A Law or μ Law PCM coding (Tables 2 and 3) or remain 16 bit linear (Table 4), as programmed via the Control Interface. The compressor can be switched to take samples from the receive path to provide a Digital Loop Back mode (see Control and Monitoring section). The PCM Interface outputs the samples at a basic 8kHz rate as defined by FSX (pin 16). The clock rate may be from 64kHz to 4096kHz in integral steps of 64kHz, as described further in the PCM Interface section.

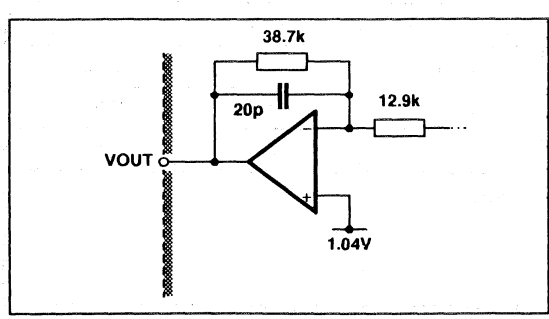


Fig. 4a : PSLAC VOUT circuitry.

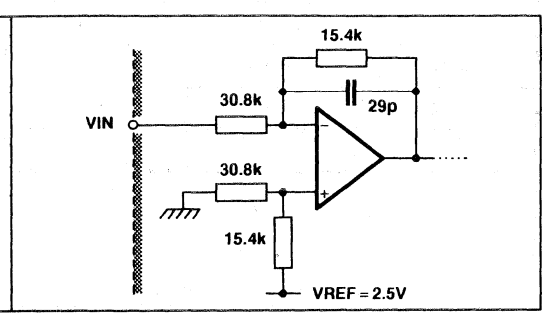


Fig. 4b : PSLAC VIN circuitry.

G_X (dB)	Hex Code	G_X (dB)	Hex Code	G_X (dB)	Hex Code	G_X (dB)	Hex Code
+12.0	9F-D8	+6.0	FF-F8	0.0	F0-80	–6.0	E8-84
+11.5	9C-90	+5.5	FE-90	–0.5	EF-8C	–6.5	E7-C8
+11.0	98-E4	+5.0	FC-B8	–1.0	EE-A0	–7.0	E7-94
+10.5	95-CC	+4.5	FA-F0	–1.5	ED-BC	–7.5	E6-E0
+10.0	92-CC	+4.0	F9-AC	–2.0	EC-DC	–8.0	E6-B0
+9.5	8F-E4	+3.5	F7-F8	–2.5	EC-80	–8.5	E6-80
+9.0	8D-8C	+3.0	F6-CC	–3.0	EB-A8	–9.0	E5-D8
+8.5	8A-C8	+2.5	F5-AC	–3.5	EA-D8	–9.5	E5-B0
+8.0	88-98	+2.0	F4-94	–4.0	EA-8C	–10.0	E5-88
+7.5	85-F8	+1.5	F3-84	–4.5	E9-C4	–10.5	E4-E4
+7.0	83-E8	+1.0	F1-F8	–5.0	E9-80	–11.0	E4-C0
+6.5	81-E8	+0.5	F0-F8	–5.5	E8-C0	–11.5	E4-A0
						–12.0	E4-84

Transmit gain coefficients. *

G_R (dB)	Hex Code	G_R (dB)	Hex Code	G_R (dB)	Hex Code
+6.0	BF-EC	0.0	A0-80	–6.0	90-84
+5.5	BC-A4	–0.5	9E-9C	–6.5	8F-94
+5.0	B8-F4	–1.0	9C-C4	–7.0	8E-A4
+4.5	B5-DC	–1.5	9A-F8	–7.5	8D-C0
+4.0	B2-DC	–2.0	99-B4	–8.0	8C-E0
+3.5	AF-F0	–2.5	98-80	–8.5	8C-84
+3.0	AD-98	–3.0	96-D4	–9.0	8B-AC
+2.5	AA-D8	–3.5	95-B0	–9.5	8A-DC
+2.0	A8-A4	–4.0	94-98	–10.0	8A-90
+1.5	A6-84	–4.5	93-88	–10.5	89-C8
+1.0	A3-F4	–5.0	92-80	–11.0	89-84
+0.5	A1-F4	–5.5	91-80	–11.5	88-C0
				–12.0	88-84

Receive gain coefficients . *

* Note: Smaller steps are possible - see Table 9.

Table 1 Transmit and receive gain coefficients for 0.5dB step adjustments .

PCM INTERFACE

The PCM Interface of the PSLAC consists of the pins DXA, DXB, CLKX, FSX, TSCA and TSCB for the Transmit output and pins DRA, DRB, CLKR and FSR for the Receive input. Figures 5 and 6 give the basic timing diagrams for Transmit and Receive directions. Note that in both cases the sample rate is set by the respective frame sync pulse (FSX/FSR) at 125µs (8kHz) intervals. This defines the length of the PCM frame which remains unchanged at all times.

For the PCM Transmit output, the FSX pulse is identified about a negative edge of CLKX, which also defines the start of the first bit (bit 1, msb) of the first 8 bit (for companded codes) or 16 bit (for linear code) sample of the frame. The PSLAC can be programmed to place the 8/16 bit sample in any 8 bit Time Slot of the frame. For 16 bit samples, the sample is moved by multiples of 8 bits, so that a minimum of two Time Slots are needed between any adjacent (multiplexed with other PSLACs) samples of the PCM frame (an offset of 8 bits is still valid). In addition, the position of all Time Slots relative to the FSX pulse can be offset by from 0 to 7 clock periods of CLKX (Clock Offset). The Time Slot and Clock Offset are dynamically programmable via the device Control Interface.

The number of Time Slots that can be in any one frame, and hence also the data rate, depends on the frequency of the data clock, CLKX. There must be at least one 8 bit Time Slot in the frame (two 8 bit Time Slots will be required for 16 bit samples), the maximum number being thirty two 8 bit Time Slots (64 for expanded mode - described later). The frequency of CLKX can therefore vary between 64kHz and 4096kHz depending on the number of Time Slots required. The number of Time Slots, N_{TS}, that are in the frame is determined by the relationship:-

$$N_{TS} = CLKX \div 64k$$

where CLKX is between 64k and 2048kHz (4096kHz expanded) in 64k steps (from 128kHz, for 16 bit linear coding).

Gating of the outputs onto a backplane or bus, can be obtained by use of the output TSCA for DXA as the programmed output pin (TSCB for DXB output). The output TSCA, or TSCB, will go low for the duration of the programmed data output time slot. Thus DXA or DXB can be gated onto a common backplane to provide security of output data. Alternatively, note that the DXA/DXB outputs are high impedance when no data is being output, so that several PSLAC outputs can be wire-ored.

Precise timing information for DXA, DXB, CLKX, FSX, TSCA and TSCB is given in the Electrical Characteristics section.

For the PCM input, the FSR pulse is also identified about a negative edge of the data clock i.e. CLKR. Data is also at the same basic sample rate of 125µs and has the same options of data/clock rate as for the output PCM. This means that there can be from 1 to 32 (64 expanded) 8 bit Time Slots, offset by 0 to 7 clock periods in the PCM frame. For 16 bit samples, the options of a multiple of 8 bit Time Slots as an offset, are still valid, as is the minimum of two Time Slots required between any adjacent (multiplexed) samples of the PCM frame. The above relationship for N_{TS} is also valid for the receive PCM timing.

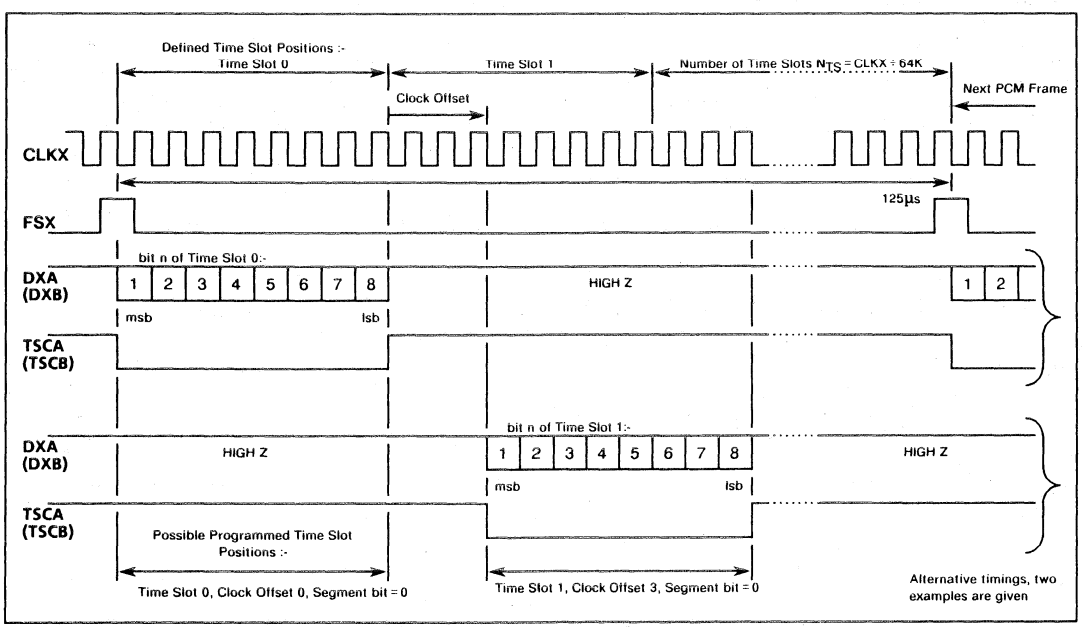


Fig. 5 : PSLAC Transmit PCM Timing Diagram.

Data is clocked into the device on the negative edge of CLKR. The first negative edge after FSR has occured defines the strobe time for the first bit of the first 8/16 bit sample of the frame. Positions of the 8 bit Time Slots are refered to this point. The Time Slot and Clock Offset of the frame that the PSLAC reads is again dynamically programmable via the Control Interface, all other bits of the frame data being ignored. Examples of the Receive PCM timing are shown in figure 6, with more precise timing information for DRA, DRB, CLKR and FSR given in the Electrical Characteristics section.

Programming of the PSLAC Transmit and Receive PCM timing can be such that a different format can exist between the two. However, coding of the data (companded 8 bit/linear 16 bit) is set simultaneously for both directions. Whilst FSX and FSR are both at a set 8kHz, they need not be coincident in time, provided they do not wander in phase. In the same way, CLKX, DXA/DXB can be offset from CLKR, DRA/DRB.

PCM Timing - Expanded Mode

The normal maximum number of Time Slots is 32 (for both Transmit and Receive directions) with CLKX/CLKR at 2048KHz and 256 data bits in the frame. This can be increased to 64 Time Slots by using expanded mode of operation. This creates a second set or segment of 256 bits that can be included in the frame. Thus, PCM data will be clocked out or read from either the first set of 256 bits (segment 0) or the second set of 256 bits (segment 1). Expanded mode is set via the Control Interface using the R_{SA} and X_{SA} bits (see Control and Monitoring section). The maximum number of Time Slots in expanded mode is 64 (32 for 16 bit samples), which can be set separately for Transmit and Receive directions.

2048kHz and 1544kHz PCM Formats

For 32 channel PCM, CLKX and CLKR are 2048kHz with Time Slot and Clock Offsets addressed as in Table 7 of the Control and Monitoring section. All 32 Time Slots of normal operation appear such that codes 20-6F are all valid. For 24 channel PCM, CLKX and CLKR are set to 1544KHz, with FSR and FSX still at 8KHz so that only 24 channels, plus bit 1 of Time Slot 25, appear in the frame. All other possible bits of the frame do not appear such that only codes 20-37, 40-57 and 60-6F of Table 7 are valid.

ENCODING AND DECODING

The analog input signal should be in the range ±3V with respect to analog ground. An input signal in this range is encoded according to the A-law, μ-Law or Linear algorithms. The corresponding PCM code is decoded to give an analog output signal in the range ±1.5V with respect to V_{OO} (nominally 2.5 Volts). This means that the analog output is one half of the amplitude of the analog input and has a net DC offset from ground. There are different reference milliwatt signals (0dBm0 levels) for input and output due to the difference in amplitude.

It is normal in a system to have a single coding scheme for a system, so for this reason Transmit and Receive coding are programmed simultaneously to work with the same scheme. The following sections describe each type of coding of the PSLAC.

A-Law and μ-Law Codes (8 Bit)

These are non-linear codes in which the signal is described in terms of a sign bit plus segment and chord bits which denote the magnitude. There are 7 segments for A-Law and 8 for μ-Law. The size of the segments increase in approximately exponential steps.

Each segment is divided up linearly into chords (except the zero level in μ-Law). This means that the resolution is finer at smaller input voltages than at larger, and so gives a better match to the human ear. Table 2 shows how the A-Law code operates and Table 3 shows the μ-Law code.

In both codes positive values are represented by a sign bit of 1. The A-Law data is alternate digit inverted (ADI) and the μ-Law magnitude data is in effect inverted. These techniques are used to ensure that there are sufficient data transitions for good clock recovery (not

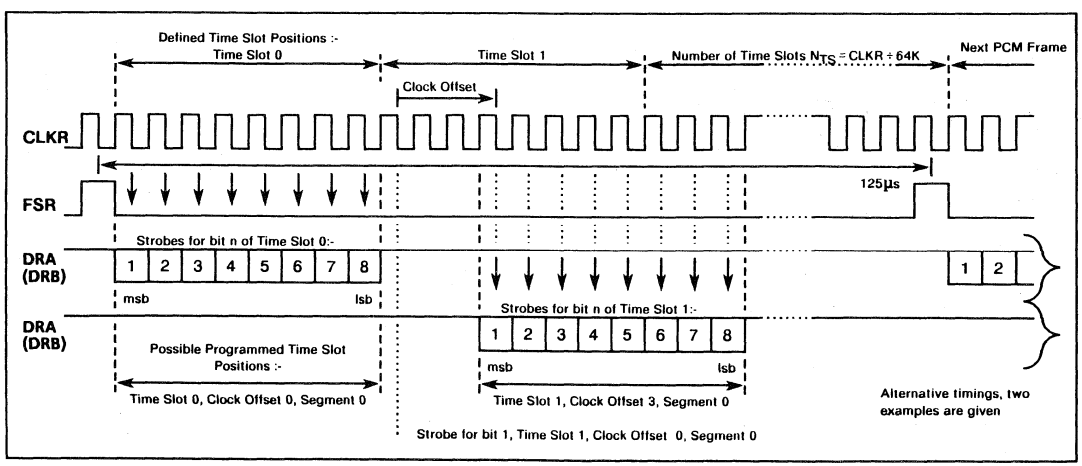


Fig 6 PSLAC receive PCM diagram.

Segment Number	Number × Size of Interval	Normalised Input Voltage = V_{IN} × (4096 ÷ 3)	PCM DATA CHARACTER		Normalised Output Voltage (Note 2) = (V_{OUT}–V_{OO}) × (4096 ÷ 1.5)
			Without ADI msb lsb	With ADI (Note 4) msb lsb	
1	32×2	+(–) 0 to 2	1(0) 000 0000	1(0) 101 0101	+(–) 1
		+(–) 2 to 4	1(0) 000 0001	1(0) 101 0100	+(–) 3
		+(–) 4 to 6	1(0) 000 0010	1(0) 101 0111	+(–) 5
		+(–) 6 to 8	1(0) 000 0011	1(0) 101 0110	+(–) 7
		:	:	:	:
		+(–) 60 to 62	1(0) 001 1110	1(0) 100 1011	+(–) 61
		+(–) 62 to 64	1(0) 001 1111	1(0) 100 1010	+(–) 63
2	16×4	+(–) 64 to 68	1(0) 010 0000	1(0) 111 0101	+(–) 66
		+(–) 68 to 72	1(0) 010 0001	1(0) 111 0100	+(–) 70
		+(–) 72 to 76	1(0) 010 0010	1(0) 111 0111	+(–) 74
		+(–) 76 to 80	1(0) 010 0011	1(0) 111 0110	+(–) 78
		:	:	:	:
		+(–) 120 to 124	1(0) 010 1110	1(0) 111 1011	+(–) 122
		+(–) 124 to 128	1(0) 010 1111	1(0) 111 1010	+(–) 126
3	16×8	+(–) 128 to 136	1(0) 011 0000	1(0) 110 0101	+(–) 132
		+(–) 136 to 144	1(0) 011 0001	1(0) 110 0100	+(–) 140
		+(–) 144 to 152	1(0) 011 0010	1(0) 110 0111	+(–) 148
		+(–) 152 to 160	1(0) 011 0011	1(0) 110 0110	+(–) 156
		:	:	:	:
		+(–) 240 to 248	1(0) 011 1110	1(0) 110 1011	+(–) 144
		+(–) 248 to 256	1(0) 011 1111	1(0) 110 1010	+(–) 252
4	16×16	+(–) 256 to 272	1(0) 100 0000	1(0) 001 0101	+(–) 264
		+(–) 272 to 288	1(0) 100 0001	1(0) 001 0100	+(–) 280
		+(–) 288 to 304	1(0) 100 0010	1(0) 001 0111	+(–) 296
		+(–) 304 to 320	1(0) 100 0011	1(0) 001 0110	+(–) 312
		:	:	:	:
		+(–) 480 to 496	1(0) 100 1110	1(0) 001 1011	+(–) 488
		+(–) 496 to 512	1(0) 100 1111	1(0) 001 1010	+(–) 504
5	16×32	+(–) 512 to 544	1(0) 101 0000	1(0) 000 0101	+(–) 528
		+(–) 544 to 576	1(0) 101 0001	1(0) 000 0100	+(–) 560
		+(–) 576 to 608	1(0) 101 0010	1(0) 000 0111	+(–) 592
		+(–) 608 to 640	1(0) 101 0011	1(0) 000 0110	+(–) 624
		:	:	:	:
		+(–) 960 to 992	1(0) 101 1110	1(0) 000 1011	+(–) 976
		+(–) 992 to 1024	1(0) 101 1111	1(0) 000 1010	+(–) 1008
6	16×64	+(–) 1024 to 1088	1(0) 110 0000	1(0) 011 0101	+(–) 1056
		+(–) 1088 to 1152	1(0) 110 0001	1(0) 011 0100	+(–) 1120
		+(–) 1152 to 1216	1(0) 110 0010	1(0) 011 0111	+(–) 1184
		+(–) 1216 to 1280	1(0) 110 0011	1(0) 011 0110	+(–) 1248
		:	:	:	:
		+(–) 1920 to 1984	1(0) 110 1110	1(0) 011 1011	+(–) 1952
		+(–) 1984 to 2048	1(0) 110 1111	1(0) 011 1010	+(–) 2016
7	16×128	+(–) 2048 to 2176	1(0) 111 0000	1(0) 010 0101	+(–) 2112
		+(–) 2176 to 2304	1(0) 111 0001	1(0) 010 0100	+(–) 2240
		+(–) 2304 to 2432	1(0) 111 0010	1(0) 010 0111	+(–) 2368
		+(–) 2432 to 2560	1(0) 111 0011	1(0) 010 0110	+(–) 2496
		:	:	:	:
		+(–) 3840 to 3968	1(0) 111 1110	1(0) 010 1011	+(–) 3904
		+(–) 3968 to 4096	1(0) 111 1111	1(0) 010 1010	+(–) 4032

Notes :-
1. 4096 Normalised value units correspond to 3.14dBm0.
2. Output Voltage (V_{OUT}) is DC offset by V_{OO}, see Electrical Characteristics.
3. Characters in parenthesis are alternatives for negative values.
4. Alternate Digit Inversion (ADI) is obtained by inversion of the even bits.

Table 2 : A-Law code.

Segment Number	Number × Size of Interval	Normalised Input Voltage = VIN × (8192 ÷ 3)	PCM DATA CHARACTER msb lsb	Normalised Output Voltage (Note 2) = (V_{OUT}–V_{OO}) × (8192 ÷ 1.5)
1	1 × 1	+ (–) 0 to 1	1(0) 111 1111	+ (–) 0
		+ (–) 1 to 3	1(0) 111 1110	+ (–) 2
		+ (–) 3 to 5	1(0) 111 1101	+ (–) 4
	15 × 2	+ (–) 5 to 7	1(0) 111 1100	+ (–) 6
		:	:	:
		+ (–) 27 to 29	1(0) 111 0001	+ (–) 28
		+ (–) 29 to 31	1(0) 111 0000	+ (–) 30
2	16 × 4	+ (–) 31 to 35	1(0) 110 1111	+ (–) 33
		+ (–) 35 to 39	1(0) 110 1110	+ (–) 37
		+ (–) 39 to 43	1(0) 110 1101	+ (–) 41
		:	:	:
		+ (–) 87 to 91	1(0) 110 0001	+ (–) 89
		+ (–) 91 to 95	1(0) 110 0000	+ (–) 93
3	16 × 8	+ (–) 95 to 103	1(0) 101 1111	+ (–) 99
		+ (–) 103 to 111	1(0) 101 1110	+ (–) 107
		+ (–) 111 to 119	1(0) 101 1101	+ (–) 115
		:	:	:
		+ (–) 207 to 215	1(0) 101 0001	+ (–) 211
		+ (–) 215 to 223	1(0) 101 0000	+ (–) 219
4	16 × 16	+ (–) 223 to 239	1(0) 100 1111	+ (–) 231
		+ (–) 239 to 255	1(0) 100 1110	+ (–) 247
		+ (–) 255 to 271	1(0) 100 1101	+ (–) 263
		:	:	:
		+ (–) 447 to 463	1(0) 100 0001	+ (–) 455
		+ (–) 463 to 479	1(0) 100 0000	+ (–) 471
5	16 × 32	+ (–) 479 to 511	1(0) 011 1111	+ (–) 495
		+ (–) 511 to 543	1(0) 011 1110	+ (–) 527
		+ (–) 543 to 575	1(0) 011 1101	+ (–) 559
		:	:	:
		+ (–) 927 to 959	1(0) 011 0001	+ (–) 943
		+ (–) 959 to 991	1(0) 011 0000	+ (–) 975
6	16 × 64	+ (–) 991 to 1055	1(0) 010 1111	+ (–) 1023
		+ (–) 1055 to 1119	1(0) 010 1110	+ (–) 1087
		+ (–) 1119 to 1183	1(0) 010 1101	+ (–) 1151
		:	:	:
		+ (–) 1887 to 1951	1(0) 010 0001	+ (–) 1919
		+ (–) 1951 to 2015	1(0) 010 0000	+ (–) 1983
7	16 × 128	+ (–) 2015 to 2143	1(0) 001 1111	+ (–) 2079
		+ (–) 2143 to 2271	1(0) 001 1110	+ (–) 2207
		+ (–) 2271 to 2399	1(0) 001 1101	+ (–) 2335
		:	:	:
		+ (–) 3807 to 3935	1(0) 001 0001	+ (–) 3871
		+ (–) 3935 to 4063	1(0) 001 0000	+ (–) 3999
8	16 × 256	+ (–) 4063 to 4319	1(0) 000 1111	+ (–) 4191
		+ (–) 4319 to 4575	1(0) 000 1110	+ (–) 4447
		+ (–) 4575 to 4831	1(0) 000 1101	+ (–) 4703
		:	:	:
		+ (–) 7647 to 7903	1(0) 000 0001	+ (–) 7775
		+ (–) 7903 to 8159	1(0) 000 0000	+ (–) 8031

Notes :-
1. 8159 Normalised value units correspond to 3.17dBm0.
2. VOUT Output Voltage (V_{OUT}) is DC offset by V_{OO}, see Electrical Characteristics.
3. Characters in parenthesis are alternatives for negative values

Table 3 : μ-Law Code.

performed by the PSLAC) on the Receive side of digital trunk lines when the channel is quiet.

Linear Code (16 Bit)

The device may be programmed for linear operation to simplify the design of telephone conference circuits or if additional signal processing is desired. A 2s' complement scheme is used with positive values represented by the sign bit equal to 0 (the opposite of the non-linear codes). The resolution is slightly less than the theoretical limit for 16 bits (see Table 4).

Signal Levels and the Digital Milliwatt

Signal levels for A-law and μ-Law codes are defined with respect to a milliwatt reference level in units of dBm0. This means that a signal of 0dBm0 is a reference milliwatt signal i.e. it is at the local reference level. It does not mean that the signal will dissipate 1mW into a 600Ω resistor (i.e. is 2.191V p-p) unless the local reference level, 0dBm0, also corresponds to 0 in units of dBm (600Ω).

The specifications for A-Law and μ-Law codes (CCITT Specification G.711) define that the uppermost coding decision levels for A-Law (4096) and μ-Law (8159) correspond to 3.14dBm0 and 3.17dBm0 respectively.

This means that the 0dBm0 level is about 5.6dBm (600Ω) at the analog input and about -0.4dBm (600Ω) at the analog output.

The digital milliwatt signal provides an example of this in practice. The digital milliwatt is a defined sequence of 8 codes which, if there was no loss on the receive path, would produce a 0dBm0 signal on the analog output. The codes for the digital milliwatt for the three cases are given in Table 5. The actual voltages involved can be determined from Tables 2, 3 and 4.

TRANSMIT AND RECEIVE FILTERS

Both the Transmit and Receive paths contain a 4 Tap FIR filter, as shown in Figure 7. The Z^{-1} sections are a delay by the internal sample rate i.e. 62.5μs (16kHz), with the output a weighted summation (A_0-A_3) of the input and delayed signals. The multipliers, or coefficients A_0-A_3 for each filter, are stored in RAM locations on chip and used by the DSP processing of the PSLAC to calculate the output samples. These coefficients are loaded via the Control Interface, as described in the Control and Monitoring section. Thus the output of the filters can be represented by the transfer function:-

$$H(Z) = \sum_{n=0}^{3} A_n(Z^{-n}) = A_0 + A_1Z^{-1} + A_2Z^{-2} + A_3Z^{-3}$$

Normalised Input Voltage $V_{IN} \times (32{,}768 \div 3)$	PCM DATA CHARACTER msb lsb	Normalised Output Voltage $-V_{OO} \times (32{,}768 \div 1.5)$
–32,768 to –32,255.5	1 000 0000 1111 1111	–32,256
–32,255.5 to –32,254.5	1 000 0010 0000 0001	–32,255
–32,254.5 to –32,253.5	1 000 0010 0000 0010	–32,254
:	:	:
–1.5 to –0.5	1 111 1111 1111 1111	–1
–0.5 to +0.5	0 000 0000 0000 0000	0
+0.5 to +1.5	0 000 0000 0000 0001	+1
:	:	:
+32,253.5 to +32,254.5	0 111 1101 1111 1110	+32,254
+32,254.5 to +32,255.5	0 111 1101 1111 1111	+32,255
+32,255.5 to + 32,768	0 111 1111 0000 0000	+32,256

Table 4 Linear code.

Phase	A-Law msb lsb	μ-Law msb lsb	LINEAR msb lsb
–7/8 × 180°	0 011 0100	0 001 1110	1 101 1101 1000 0100
–5/8 × 180°	0 010 0001	0 000 1011	1 010 1110 1000 0100
–3/8 × 180°	0 010 0001	0 000 1011	1 010 1110 1000 0100
–1/8 × 180°	0 011 0100	0 001 1110	1 101 1101 1000 0100
+1/8 × 180°	1 011 0100	1 001 1110	0 010 0010 0111 1100
+3/8 × 180°	1 010 0001	1 000 1011	0 101 0001 0111 1100
+5/8 × 180°	1 010 0001	1 000 1011	0 101 0001 0111 1100
+7/8 × 180°	1 011 0100	1 001 1110	0 010 0010 0111 1100

Table 5 Successive PCM input codes for Digital Milliwatt on V_{OUT}.

The unit delay operator of the digital filter, Z^{-1}, can be represented as:-

$$Z^{-1} = \exp(-j2\pi f \div f_0)$$

where f_0 is the sample frequency (16kHz), f the signal frequency. We can obtain the real part of the filter response from the following:-

$$\mathrm{Re}\{H(z)\} = \sum_{n=0}^{3} A_n \cos(2\pi n f t) \qquad \text{with } t = 1/f_0$$

i.e. $= A_0 + A_1\cos(\omega t) + A_2\cos(2\omega t) + A_3\cos(3\omega t)$ ...(1)

and similarily the imaginary part of the filter response will be :-

$$\mathrm{Im}\{H(z)\} = \sum_{n=0}^{3} A_n \sin(2\pi n f t)$$

i.e. $= A_1\sin(\omega t) + A_2\sin(2\omega t) + A_3\sin(3\omega t)$ ...(2)

We can write $\cos(2\omega t)$, $\cos(3\omega t)$, $\sin(2\omega t)$ and $\sin(3\omega t)$ in terms of $\cos(\omega t)$ and $\sin(\omega t)$, so that equations 1 and 2 become :-

$$\mathrm{Re} = A_0 - A_2 + (A_1 - 3A_3)\cos(\theta) + 2A_2\cos^2(\theta) + 4A_3\cos^3(\theta) \quad ..(3)$$
$$\mathrm{Im} = \sin(\theta)[A_1 - A_3 + 2A_2\cos(\theta) + 4A_3\cos^2(\theta)] \quad ...(4)$$

where $\theta = 2\pi f t$. For the amplitude, A, and phase, ϕ, characteristics we can use the following:-

$$A = (\mathrm{Re}^2 + \mathrm{Im}^2)^{\frac{1}{2}}$$
$$\tan(\phi) = (\mathrm{Im}) \div (\mathrm{Re})$$

Using equations 3 and 4 for real and imaginary parts of the filter response, then we obtain:-

$$A = \{8Q\cos^3(\theta) + 4P\cos^2(\theta) + 2N\cos(\theta) + M\}^{\frac{1}{2}} \quad ...(5)$$

with $Q = A_0A_3$
$P = A_0A_2 + A_1A_3$
$N = A_0A_1 + A_1A_2 + A_2A_3 - 3A_0A_3$
$M = (A_0 - A_2)^2 + (A_1 - A_3)^2$

and $\tan(\phi) = \tan(\theta)\{1 + [2A_2\cos(\theta) + (A_2 - A_0)] \div \mathrm{Re}\}$ ...(6)

with Re as in 3, as general equations for A and ϕ of the filter response, relative to the filter input signal.

Both Transmit and Receive filters can be switched in and out of the signal path by Control Words input via the Control Interface. This can be done with the device in its power-up or power-down modes of operation. In addition, further Control Words allow both reading and writing of the filter coefficients A_0-A_3, also in both modes.

C FILTER

The structure of the C Filter is shown in outline form in figure 8. In fact the C Filter consists of two separate filters, with identical form, known as the Foreground and Background Filters. The Foreground Filter provides modified samples of the receive path for cancellation of the receive signal (via the echo path) from the transmit signal. The Background Filter is used in adaptive mode to automatically search for any new coefficients that may improve cancellation by the Foreground Filter.

Adaptive Mode, as described, uses the error from both filters to determine whether or not the background coefficients provide better cancellation than the foreground coefficients. Whenever this is the case, then the new coefficients are transferred to the Foreground Filter, and the Background Filter continues searching for even better coefficients. Note that the Error Filter output is used in the

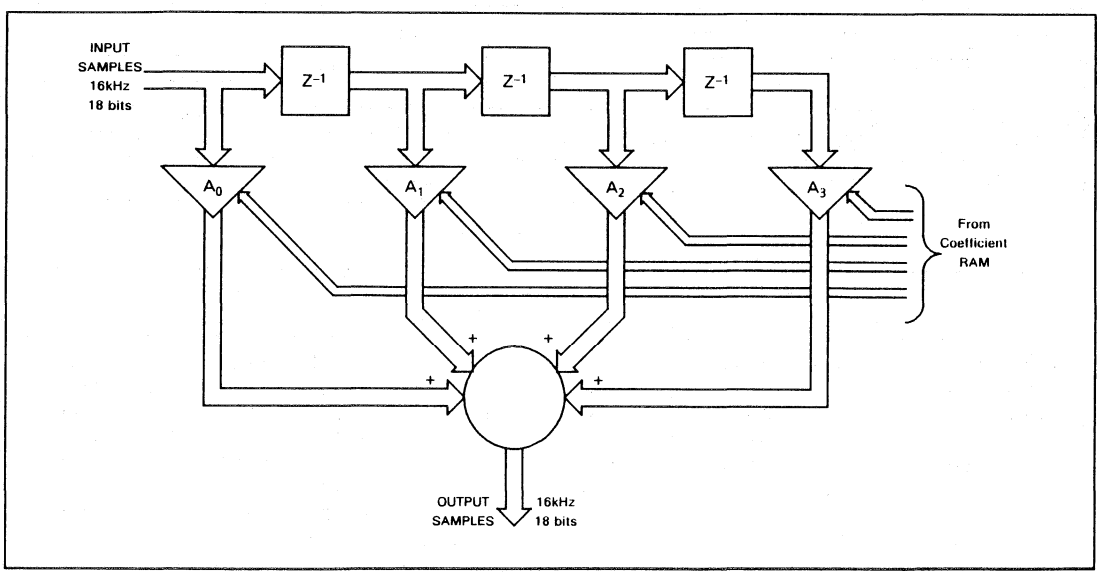


Figure 7 Transmit and receive filter structure (4 Tap FIR).

decision process for the transfer of new coefficients, with the DC Tap eliminating DC.

In the non-adaptive mode updating of coefficients is inhibited, and the C Filter uses the last set of coefficients entered into the Foreground Filter. These will either be from the Background Filter (adaption has been frozen) or those entered via the Control Interface. Writing or reading of coefficients can be carried out at any time in either the power-up or power-down modes of operation of the PSLAC.

The nature/value of the coefficients depends on the nature of the echo path. This echo path depends on the interface of the PSLAC to the subscriber line (2 to 4 wire conversion). Such an interface might consist of a transformer type Hybrid or a solid state Subscriber Line Interface Circuit (SLIC), such as the GEC Plessey Semiconductors SL373 or SL376 (see separate data sheets). It is normal to expect that the 2 to 4-wire conversion will consist of a mismatch of the receive input to the 2-wire line and not completely (if at all) remove the receive signal from the transmit signal. This Echo Return varies as the conditions of the line (length/impedance etc) vary, so causing differing characteristics of the echo path. It is the job of the C filter to remove this echo from the transmit signal. Thus the C Filter allows several software solutions, with one hardware design, to provide different line interfaces within the telephone network. The C Filter adaptive mode then makes it possible for the PSLAC to automatically follow any changing conditions of each subscriber line, so maintaining good Echo Return Loss at the PSLAC PCM output.

Note that the echo path will include any D/A and A/D delays within the PSLAC, which are discussed later on in this section. We need now to discuss the C Filter in more detail.

Fig. 9 shows a more detailed model of the C Filter. It can be seen that the filter is 9 taps FIR followed by a tenth tap IIR, which has a 15/16 multiplier in the feedback loop forming the last tap. This last tap allows matching of any long tail of the impulse resonse of the echo path, whilst maintaining a more concise structure. As for the Transmit and Receive Filters, the C Filter also operates at a basic 16kHz (62.5µs taps) rate.

Since both Foreground and Background Filters are of the same structure, we can represent them as being made up from one set of unit delay sections (Z^{-1}). The two filter outputs are then just different summations of the filter sections. Note that only the odd numbered taps of the Background Filter (coefficients A_1, A_3, A_5, A_7, A_9) are involved in the adaptive process. This prevents adaption of the filter to frequencies in the range 4kHz-8kHz.

The adaptive process uses the difference between the Adaptive Error and the Fixed Error to decide whether or not to update the foreground coefficients. Adaptive Error is determined from the difference between the Background Filter output and the Transmit input, as is the Fixed Error from that of the Foreground Filter output and Transmit input. If the long term average of the Adaptive Error is less than 7/8 of the Fixed Error, then a signal will be generated to initiate transfer of the adaptive coefficients (odd taps only) to the Foreground Filter.

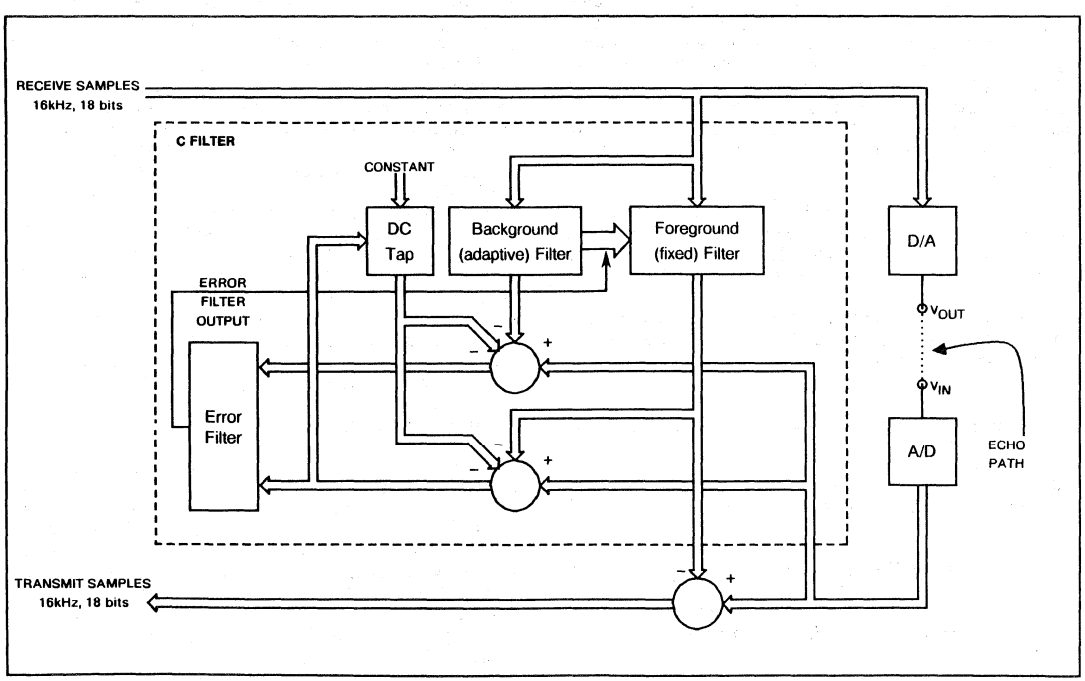


Fig 8 : PSLAC basic C Filter Structure (9 Tap FIR + 1 Tap IIR).

The minimum time for adaption is 64ms under appropriate conditions. Typically adaption may take several hundred ms. New coefficients for the Background Filter are generated using the classic Widrow/Hoff algorithm. The PSLAC thus uses the nature of the signal to analyse the echo path. In order to obtain good broadband cancellation using adaption it is necessary to use a broadband signal at the receive input. If a single tone were to be used, for example, then whilst cancellation is achieved at this frequency, there is no guarantee of performance at other frequencies (if the C Filter is now set to non-adaptive mode) since the PSLAC was unable to use these frequencies in the echo analysis.

For the C Filter to be operative, it must first be enabled via the control interface. The filter can then be used in either Adaptive mode (able to follow changes in the echo path) or Non-Adaptive mode (fixed modelling of the echo path). Adaption takes place (Adapt Enable, Fig. 9) with the C Filter enabled, under two separate conditions. Firstly, it may be controlled by use of enable/disable codes via the Control Interface, as described in the Control and Monitoring section. Alternatively, it is set by the logic level at the Status Input (SI) pin using other control codes. Note that adaption may not occur if there is a large DC bias at the VIN pin. The SI pin also controls adaption as described in the Stand-Alone section. When disabled, Transmit samples remain totally unaffected by the C Filter. As with the Transmit and Receive Filters, all of the coefficients can be programmed and/or read out via the Control Interface, whether or not the PSLAC is in Power-Up or Power-Down mode (see Control and Monitoring section).

A signal correlator is incorporated which will detect periodic signals in the receive path. When detected the background filter coefficients, even if deemed to give better cancellation, are not transferred to the foreground. The correlator may be disabled for testing and preprogramming purposes (see control and monitoring section). A double talk detector is also included to prevent adaption while large near end signals are present. A programmable coefficient DTC allows the relative levels of near and far end signals that trigger this detector to be set (see Table 13). Setting this coefficient to zero will disable this feature.

An oscillation quench circuit will reset the adaptive coefficients to their preprogrammed values should an unstable situation occur. This action can be monitored via the control interface (see Table 14).

We can obtain a mathematical representation of the C Filter in the same way as for the Transmit and Receive Filters. Thus we can write:-

$$H(Z) = \sum_{n=0}^{8} A_n Z^{-n} + \{[A_9 Z^{-9}] \div [16-15Z^{-1}]\} \quad ...(7)$$

with $Z^{-1} = \exp(-j\omega t)$ as before. For real and imaginary parts of the filter response (equation 7) we get:-

$$\mathrm{Re}\{H(Z)\} = \sum_{n=0}^{8} A_n \cos(n\theta) + \{A_9 X\} \quad ...(8)$$

$$\mathrm{Im}\{H(Z)\} = \sum_{n=0}^{8} A_n \sin(n\theta) + \{A_9 Y\} \quad ...(9)$$

where $X = \{[16\cos(9\theta)-15\cos(8\theta)] + [481-480\cos(\theta)]\}$
and $Y = \{[16\sin(9\theta)-15\sin(8\theta)] \div [481-480\cos(\theta)]\}$

which can be used to obtain the amplitude, A, and phase, ϕ, of the filter from :-

$$A = (Re^2 + Im^2)^{\frac{1}{2}} \quad ...(10)$$
$$\mathrm{Tan}(\phi) = (\mathrm{Im} \div \mathrm{Re}) \quad ...(11)$$

Equations 8 to 11 form the basis of a computer program that calculates the necessary coefficient values required to obtain a given response. More information on this is given in Application Note AN84, Preprogramming the PSLAC C Filter using the measurement method.

When determining coefficients for a given C Filter response, note that the echo path will include the PSLAC D/A and A/D delays. In addition, the amplitude of the echo signal is also affected by the difference between the VOUT and V_{IN} dynamic ranges and also includes the 16/15 of the D/A conversion. The combined effect is to add a 5.46dB (×8/15) loss to the echo path, at a delay of 125µs, or 2 Taps (i.e. at A_2).

CONTROL and MONITORING

The MV3010 is controlled and monitored through the device control interface. This allows control of the I/O Latches and status interface, PCM coding and modes of operation, the programming of the Transmit and Receive Time Slot and Clock Offsets, the Gain and Filter coefficients, the C Filter modes and the activation and deactivation of the diagnostic functions.

Initialisation, Power-Up/Power-Down

When power is first applied, the MV3010 is initialised and goes into its power-down mode of operation. This has several consequences: the Transmit PCM Outputs (DXA and DXB) go into their high-impedance state; the Analog Output (V_{OUT}) goes to Analog Ground (AGND); Transmit and Receive Time Slot and Clock Offsets are set to zero; PCM ports A, non-expanded mode are selected; the Digital I/O pins (CP1 to CP5) are configured as inputs; A-Law is selected; Transmit, Receive and Cancellation Filters are disabled; Transmit and Receive Gains are set to 0dB, correlator is enabled, double talk coefficient is set to zero and the adaptive mode of the C Filter is set only if the SI pin is high. None of the PSLAC functions are active or meaningful until the device is put into its power-up mode. power-down mode is thus a standby, low power consumption state of the device. When a Power-Up command is sent via the Control Interface, then the PSLAC becomes fully active with functions as set via the interface or as for Stand Alone operation. Control instructions may be sent to the device 500µs after the first application of power. The Power-Down instruction may be sent to the device at any time to select this mode.

Stand-Alone Operation

If the default conditions established by initialisation are acceptable, Stand-Alone operation can be used. In this mode, the functions remain as set during initialisation with the PSLAC only able to change between power-up and power-down modes, excepting that the SI pin enables the C Filter with adaption (SI Pin high) or disables the filter totally (SI Pin low). Stand-Alone operation is selected by holding the $\overline{CS}$ pin low for greater than 8 periods of the clock applied to the DCLK pin. Note, this is easily achieved by connecting the DCLK pin to the adjacent MCLK pin with Power-Up and Power-Down instructions generated by holding the DI/O pin high or low, respectively.

Normal Operation

For Normal Operation, control information is sent to the MV3010 as 8 bit bytes input on the DI/O pin, strobed under the control of the DCLK clock and $\overline{CS}$ pulse. All the functions of the PSLAC can now be set via the Control Interface.

Data entered to the device will be one of two types. Most of the time data will consist of Control Codes to change the device functional status. Some of these Control Codes require subsequent Data bytes to be entered as part of the instruction, or will cause subsequent output of Data relevant to the Control Code.

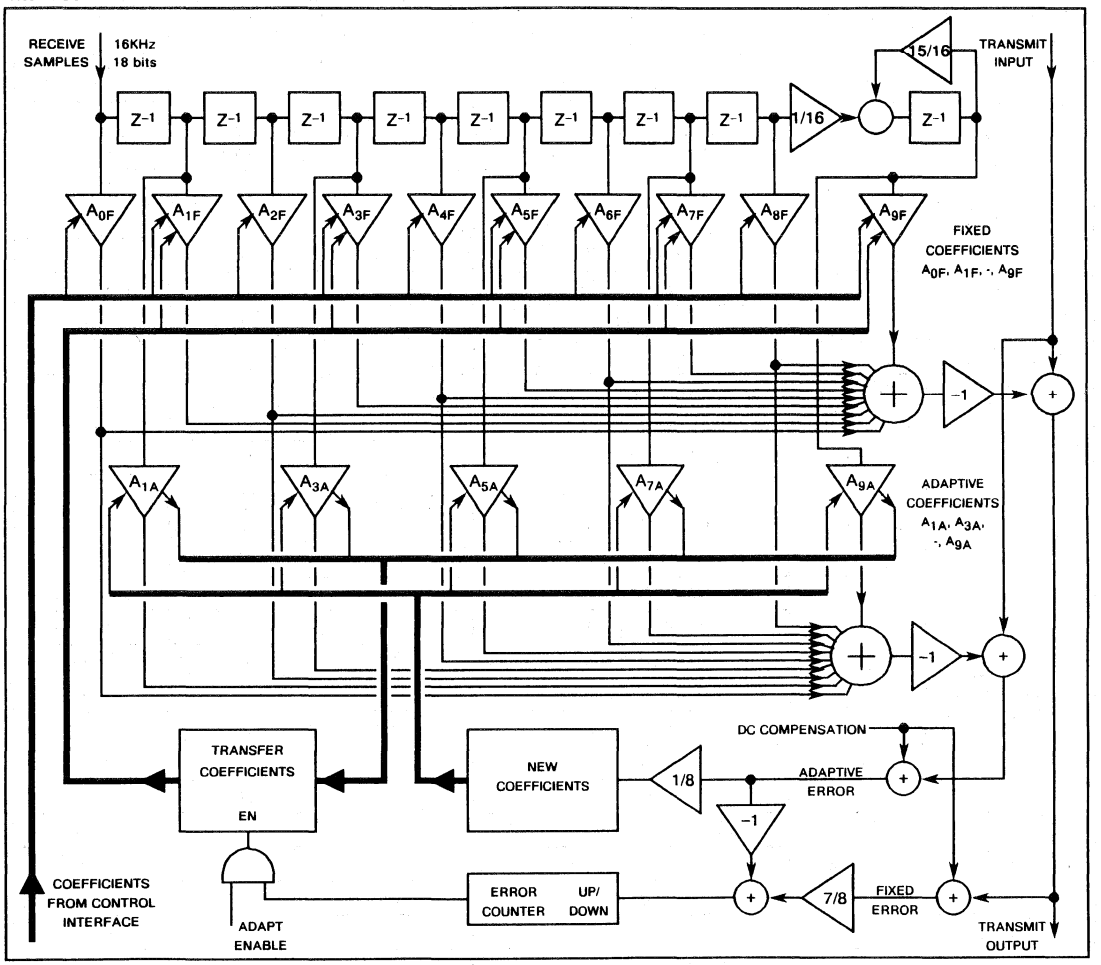


Fig.9 PSLAC conceptual C Filter representation (9 tap FIR + 1 tap IIR).

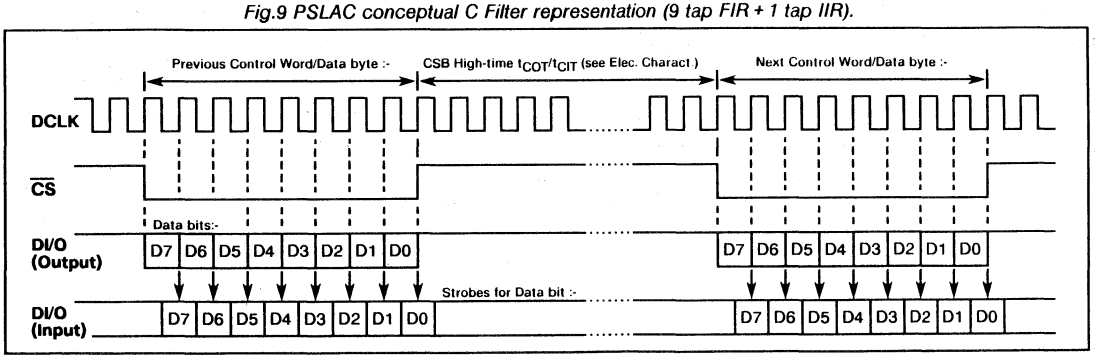


Fig.10 PSLAC control interface timing diagram, normal operation.

INSTRUCTION DESCRIPTION				MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES
Operating Mode	Set Power-Up			PU	FF	None
	Set Power-Down			PD	00	None
PCM Slot Address	Transmit	Read		STR	75	1 - Output
		Write	Time Slot	STWT	20 to 3F	None
			Clock offset	STWC	60 to 67	None
	Receive	Read		SRR	7D	1 - Output
		Write	Time Slot	SRWT	40 to5F	None
			Clock offset	SRWC	68 to 6F	None
Gain Adjust	Transmit, G_X	Read Coefficient		GTR	71	2 - Output
		Write Coefficient		GTW	72	2 - Input
	Receive, G_R	Read Coefficient		GRR	79	2 - Output
		Write Coefficient		GRW	7A	2 - Input
Filter Commands	Enable Selected Filters			FE	80 to 87	None
	Transmit	Read Coefficients		FTR	A7	8 - Output
		Write Coefficients		FTW	A4	8 - Input
	Receive	Read Coefficients		FRR	AB	8 - Output
		Write Coefficients		FRW	A8	8 - Input
	Cancellation	Control Filter Modes		FCC	BC to BF	None
		Read Coefficients		FCR	A3	20 - Output
		Write Coefficients		FCW	A0	20 - Input
		Read Double - Talk		FCDR	A1	2 - Output
		Write Double - Talk		FCDW	A2	2 - Input
Digital I/O's and Status Input pin (SI)	Digital I/O Configuration	Read Status		IOCR	C1	1 - Output
		Write Status		IOCW	D1	1 - Input
	Digital I/O Data	Read		IODR	C8	1 - Output
		Write		IODW	D8	1 - Input
PCM	Set Coding Scheme			PC	B8 to BB	None
	Association	Read		PAR	77	1 - Output
		Write		PAW	90 to 9F	None
Diagnostic	Reset			DR	B0	None
	High Pass Filter Disable			DHD	B3	None
	Receive	Attenuate Path		DRA	B1	None
		Disable Path		DRD	B2	None
	Loop	Analog		DLA	B7	None
		Digital		DLD	B4	None
	Correlator	Disable		DCD	B5	None

Fig. 11 PSLAC Control Instructions - see also Tables 6 to 16.

Data which is requested from the device is output on the DI/O pin, any attempted input of data being ignored until all data bytes have been output (any input driving DI/O will thus corrupt the output data). Fig. 10 shows the nominal signal timing.

The normal programming sequence is for a Code byte to be sent to the device first. This may be followed by a number of Data bytes sent to/read from the device depending on the specific Control Code preceeding them. If the Control Code requires loading of associated Data bytes on DI/O, then programming must continue with the relevant number of data bytes after the Control Code.

All subsequent bytes after the Control Code that are expected to be data will be treated as data for that code. No more Control Codes will be accepted until all data has been entered. The only exception to this is that the programming sequence will be aborted and the device will enter Power-Down mode if a Power-down instruction is sent instead of an input data byte (there is no all zeros data byte so confusion is avoided). Programming of the device continues normally after the last data byte has been entered, or output if that was the last Control Code.

Figure 11 shows the various Control Codes available with Figure 12 a Control Code Map. The effect of each code is described in Tables 6 to 16.

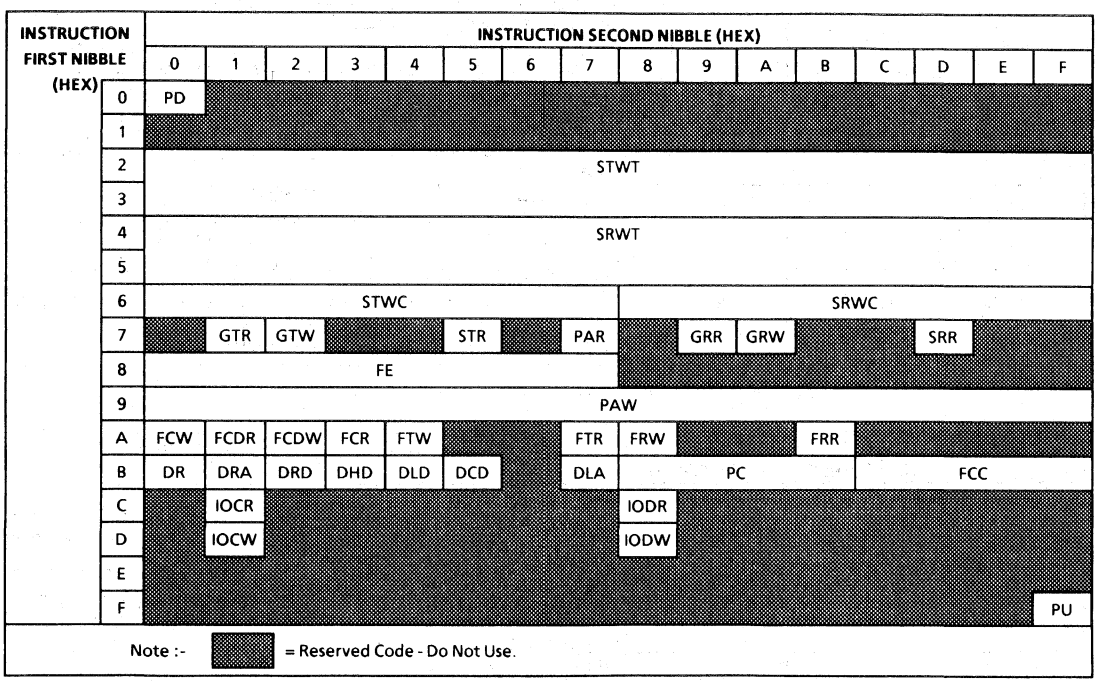


Fig.12 PSLAC control instructions - see also Tables 6 to 16.

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
PU	FF	None	**Power-Up.** This instruction takes the device out of Power-Down. It would normally be preceeded by instructions to configure the device. It has no effect if the device is not in power-down mode.
PD	00	None	**Power-Down.** This instruction puts the device into Power-Down mode. The transmit PCM outputs (DXA and DXB) go into their high impedance state and the analog output (VOUT) goes to V_{AGND}. The device is still programmable in this mode.

Table 6 Operating mode instructions.

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
STR	75	1-Output	**Slot Address - Transmit - Read.** This instruction causes the device to output a data byte which contains the transmit slot address. The data byte contains the 5 Time Slot address bits (MSBs) followed by the 3 Clock Offset bits. For example, if the hex data byte is B1, then the Time Slot has been set to 22 and the Clock Offset has been set to 1; i.e. the start of the transmit PCM output is offset by 177 (=22x8+1) clock cycles from FSX.
STWT	20 to 3F	None	**Slot Address - Transmit - Write - Time Slot.** This instruction defines the Transmit Time Slot address. The 3 msb's define the Code type, and the 5 LSBs set the Time Slot. For example the hex code 2A sets the Time Slot address to 10.
STWC	60 to 67	None	**Slot Address - Transmit - Write - Clock Offset.** This instruction defines the Transmit Clock Offset. The 5 MSBs define the Code type, and the 3 LSBs set the Clock Offset. For example the hex code 63 sets the Clock Offset to 3.
SRR	7D	1-Output	**Slot Address - Receive - Read.** This instruction causes the device to output a data byte which contains the receive slot address. The data byte contains the 5 Time Slot address bits (MSBs) followed by the 3 Clock Offset bits. For example, if the hex data byte is B1, then the Time Slot has been set to 22 and the Clock Offset has been set to 1, i.e. the start of the receive PCM input is offset by 177 (=22x8+1) clock cycles from FSR.
SRWT	40 to 5F	None	**Slot Address - Receive - Write - Time Slot.** This instruction defines the Receive Time Slot address. The 3 MSBs define the Code type, and the 5 LSBs set the Time Slot. For example the hex code 4A sets the Time Slot address to 10.
SRWC	68 to 6F	None	**Slot Address - Receive - Write - Clock Offset.** This instruction defines the Receive Clock Offset. The 5 MSBs define the Code type, and the 3 LSBs set the Clock Offset. For example the hex code 6B sets the Clock Offset to 3.

Table 7 PCM Time Slot and Clock Offset instructions.

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
GTR	71	2-Output	**Gain - Transmit - Read.** This instruction causes the device to output 2 data bytes which contain the Transmit Gain information, G_X, in the format shown in Table 9.
GTW	72	2-Input	**Gain - Transmit - Write.** This instruction sets the Transmit Gain, G_X, to the value defined by two successive data bytes, which must be entered in the format shown in Table 9.
GRR	79	2-Output	**Gain - Receive - Read.** This instruction causes the device to output 2 data bytes which contain the Receive Gain information, G_R, in the format shown in Table 9.
GRW	7A	2-Input	**Gain - Receive - Write.** This instruction sets the Receive Gain, G_R, to the value defined by two successive data bytes, which must be entered in the format shown in Table 9.

Table 8 Transmit and Receive Gain instructions.

DATA BYTE FORM									DATA DESCRIPTION
BYTE No.	BIT No D7	D6	D5	D4	D3	D2	D1	D0	These bytes are in the form of a 2s' complement number in the range ±2 which are used to construct the gain Coefficients as follows:- $G = -G_1 \times 2^1 + G_0 \times 2^0 + G_{-1} \times 2^{-1} + G_{-2} \times 2^{-2} + ... + G_{-10}2^{-10}$ The Receive Gain is $G_R = G$ i.e. –2 to +2. The Transmit Gain is $G_X = 2 \times (G + 1)$ i.e. –2 to +6.
1	1	G_1	G_0	G_{-1}	G_{-2}	G_{-3}	G_{-4}	G_{-5}	
2	1	G_{-6}	G_{-7}	G_{-8}	G_{-9}	G_{-10}	X	X	
1 = +5V, X = Dont Care (0/1)									

Table 9 Transmit and Receive Gain data bytes (coefficients).

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
FE	80 to 87	None	**Filter - Enable.** This instruction allows the C Filter, Transmit Filter and Receive Filter to be enabled or disabled. The instruction has the format:- D7 D6 D5 D4 D3 D2 D1 D0 1 0 0 0 0 CF XF RF If CF is 1 then the C Filter is enabled. If it is 0 then the C Filter is disabled (i.e. Cancellation subtracts zero). If XF is 1 then the X Filter is enabled. If it is 0 then the X Filter is disabled (i.e. the transfer function is set to 1). If RF is 1 then the R Filter is enabled. If it is 0 then the R Filter is disabled (i.e. the transfer function is set to 1). N.B. Disabling a filter does not change its coefficients.
FTR	A7	8-Output	**Filter - Transmit - Read.** This instruction causes the device to output 8 data bytes which represent the 4 numbers corresponding to the 4 Transmit Filter coefficients that have the format shown in Table 11.
FTW	A4	8-Input	**Filter - Transmit - Write.** This instruction sets the 4 Transmit Filter coefficients to the 4 numbers, represented by the 8 data bytes, of the format shown in Table 11.
FRR	AB	8-Output	**Filter - Receive - Read.** This instruction causes the device to output 8 data bytes which represent the 4 numbers corresponding to the 4 Receive Filter coefficients that have the format shown in Table 11.
FRW	A8	8-Input	**Filter - Receive - Write.** This instruction sets the 4 Receive Filter coefficients to the 4 numbers, represented by the 8 data bytes, of the format shown in Table 11.
FCC	BC to BF	None	**Filter - Cancellation - Control.** This instruction allows the automatic adaption of the C Filter to be enabled or disabled. There is a 2-bit field in the instruction which allows adaption to be enabled with or without polling the SI pin. The instruction has the format:- D7 D6 D5 D4 D3 D2 D1 D0 1 0 1 1 1 1 CD CA If CD is 1 then adaption of the C Filter is disabled. If CD is 0 then adaption is enabled if either CA is 1 or if the SI pin is high.
FCR	A3	20 - Output	**Filter - Cancellation - Read.** This instruction causes the device to output 20 data bytes which represent the 10 numbers corresponding to the 10 Cancellation Filter coefficients that have the format shown in Table 12.
FCW	A0	20 - Input.	**Filter - Cancellation - Write.** This instruction sets the 10 Cancellation Filter coefficients to the 10 numbers, represented by the 20 data bytes, of the format shown in Table 12.
FCDR	A1	2 - Output	**Filter - Cancellation - Double Talk - Read** This instruction causes the device to output 2 data bytes which represent the double talk detector coefficient as shown in Table 13.
FCDW	A2	2 - Input	**Filter - Cancellation - Double Talk - Write** This instruction sets the double-talk detector coefficient to the number represented by the two data bytes as shown in Table 13.

Table 10 Filter instructions.

DATA BYTE FORMAT									DATA DESCRIPTION
BYTE No.	BIT No.								
	D7	D6	D5	D4	D3	D2	D1	D0	
1	1	A_{31}	A_{30}	A_{3-1}	A_{3-2}	A_{3-3}	A_{3-4}	A_{3-5}	These bytes contain four 2s' complement numbers each in the range ±2 which are used to construct the filter coefficients as follows:-
2	1	A_{3-6}	A_{3-7}	A_{3-8}	A_{3-9}	A_{3-10}	X	X	
3	1	A_{21}	A_{20}	A_{2-1}	A_{2-2}	A_{2-3}	A_{2-4}	A_{2-5}	$A_m = -A_{m1} \times 2^1 + A_{m0} \times 2^0 + A_{m-1} \times 2^{-1} + A_{m-2} \times 2^{-2} + ... + A_{m-10} 2^{-10}$
4	1	A_{2-6}	A_{2-7}	A_{2-8}	A_{2-9}	A_{2-10}	X	X	
5	1	A_{11}	A_{10}	A_{1-1}	A_{1-2}	A_{1-3}	A_{1-4}	A_{1-5}	with m = 0,1,2,3 for the four coefficients.
6	1	A_{1-6}	A_{1-7}	A_{1-8}	A_{1-9}	A_{1-10}	X	X	The transfer function for the filters is:-
7	1	A_{01}	A_{00}	A_{0-1}	A_{0-2}	A_{0-3}	A_{0-4}	A_{0-5}	$H(Z) = A_0 + A_1 Z^{-1} + A_2 Z^{-2} + A_3 Z^{-3}$
8	1	A_{0-6}	A_{0-7}	A_{0-8}	A_{0-9}	A_{0-10}	X	X	where the Z transformation is at 16kHz i.e. $Z = \exp(-j2\pi ft)$ with t = 1/16kHz
1 = +5V, X = Dont Care (0/1)									

Table 11 Transmit and Receive Filter data bytes (coefficients).

DATA BYTE FORMAT									DATA DESCRIPTION
BYTE No	BIT No								
	D7	D6	D5	D4	D3	D2	D1	D0	
1	1	A_{81}	A_{80}	A_{8-1}	A_{8-2}	A_{8-3}	A_{8-4}	A_{8-5}	These bytes contain ten 2s' complement numbers each in the range ±2 which are used to construct the filter coefficients as follows:-
2	1	A_{8-6}	A_{8-7}	A_{8-8}	A_{8-9}	A_{8-10}	X	X	
3	1	A_{61}	A_{60}	A_{6-1}	A_{6-2}	A_{6-3}	A_{6-4}	A_{6-5}	$A_m = -A_{m1} \times 2^1 + A_{m0} \times 2^0 + A_{m-1} \times 2^{-1} + A_{m-2} \times 2^{-2} + ... + A_{m-10} 2^{-10}$
4	1	A_{6-6}	A_{6-7}	A_{6-8}	A_{6-9}	A_{6-10}	X	X	
5	1	A_{41}	A_{40}	A_{4-1}	A_{4-2}	A_{4-3}	A_{4-4}	A_{4-5}	with m = 0,1,2,3,...,9 for the ten coefficients.
6	1	A_{4-6}	A_{4-7}	A_{4-8}	A_{4-9}	A_{4-10}	X	X	The transfer function for the filter is:-
7	1	A_{21}	A_{20}	A_{2-1}	A_{2-2}	A_{2-3}	A_{2-4}	A_{2-5}	$H(Z) = A_0 + A_1 Z^{-1} + A_2 Z^{-2} + ... + A_8 Z^{-8} + \{[A_9 Z^{-9}] \div [16 - 15 Z^{-1}]\}$
8	1	A_{2-6}	A_{2-7}	A_{2-8}	A_{2-9}	A_{2-10}	X	X	where the Z transformation is at 16kHz i.e. $Z = \exp(-j2\pi ft)$ with t = 1/16kHz
9	1	A_{01}	A_{00}	A_{0-1}	A_{0-2}	A_{0-3}	A_{0-4}	A_{0-5}	
10	1	A_{0-6}	A_{0-7}	A_{0-8}	A_{0-9}	A_{0-10}	X	X	Note that only the odd coefficients (A9, A7, A5, A3, A1) adapt. Bits listed as 1 = +5V and X = Dont Care (0 or 1).
11	1	A_{91}	A_{90}	A_{9-1}	A_{9-2}	A_{9-3}	A_{9-4}	A_{9-5}	
12	1	A_{9-6}	A_{9-7}	A_{9-8}	A_{9-9}	A_{9-10}	X	X	
13	1	A_{71}	A_{70}	A_{7-1}	A_{7-2}	A_{7-3}	A_{7-4}	A_{7-5}	
14	1	A_{7-6}	A_{7-7}	A_{7-8}	A_{7-9}	A_{7-10}	X	X	
15	1	A_{51}	A_{50}	A_{5-1}	A_{5-2}	A_{5-3}	A_{5-4}	A_{5-5}	
16	1	A_{5-6}	A_{5-7}	A_{5-8}	A_{5-9}	A_{5-10}	X	X	
17	1	A_{31}	A_{30}	A_{3-1}	A_{3-2}	A_{3-3}	A_{3-4}	A_{3-5}	
18	1	A_{3-6}	A_{3-7}	A_{3-8}	A_{3-9}	A_{3-10}	X	X	
19	1	A_{11}	A_{10}	A_{1-1}	A_{1-2}	A_{1-3}	A_{1-4}	A_{1-5}	
20	1	A_{1-6}	A_{1-7}	A_{1-8}	A_{1-9}	A_{1-10}	X	X	

Table 12 C Filter data bytes (coefficients).

DATA BYTE FORMAT									DATA DESCRIPTION
BYTE No	BIT No								
	D7	D6	D5	D4	D3	D2	D1	D0	
1	1	A_1	A_0	A_{-1}	A_{-2}	A_{-3}	A_{-4}	A_{-5}	These bytes are in the form of a 2s' complement number in the range ± 2.
2	1	A_{-6}	A_{-7}	A_{-8}	A_{-9}	A_{-10}	X	X	$A = -A_1 \times 2^1 + A_0 \times 2^0 + A_{-1} \times 2^{-1} .... + A_{-10} \cdot 2^{-10}$
1 = +5V, X = Dont Care (0,1)									The double talk detector compares the incoming RX signal level with the fixed error signal multiplied by the double talk coefficient (DTC)
									where DTC = 4 × A
									If the RX signal is the smaller then adaption is frozen.

Table 1 Double Talk Detector bytes (Coefficient).

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
IOCR	C1	1-Output	**Digital I/O - Configuration - Read.** The data byte which is output by the device after this instruction indicates which of the Digital I/O pins are inputs, which are outputs. These have the the format:- D7 D6 D5 D4 D3 D2 D1 D0 CC1 CC2 CC3 CC4 CC5 X X X If CCn is 0 then the CPn pin is an output. If CCn is 1 then the CPn pin is an input (n = 1, 2, 3, 4, 5).
IOCW	D1	1-Input	**Digital I/O - Configuration - Write.** This instruction configures the Digital I/O pins to be inputs or outputs according to the input data byte which has the format:- D7 D6 D5 D4 D3 D2 D1 D0 CC1 CC2 CC3 CC4 CC5 R2 R1 R0 If CCn is 0 then the CPn pin is an output. If CCn is 1 then the CPn pin is an input (n = 1, 2, 3, 4, 5). Note the R2-R0 bits are reserved and should be set to 1, and that first application of power sets all Digital I/O pins to inputs.
IODR	C8	1-Output	**Digital I/O and Status Input - Data - Read.** The data byte which is output by the device after this instruction indicates the status of the Digital I/O pins, C Filter Oscillation Quench and SI pin. These have the format:- D7 D6 D5 D4 D3 D2 D1 D0 CP1 CP2 CP3 CP4 CP5 X Q SI If the CPn pin is configured as an input then the CPn bit is 1 or 0 depending on whether the input is high or low. If the CPn pin is configured as an output then the CPn bit is 1 or 0 depending on whether the output is high or low (n = 1, 2, 3, 4, 5). The Q bit will normally read 0. If loop oscillation has been detected and the pre-programmed coefficients returned to the adaptive filter then this bit will read 1. This command will reset the Q bit to 0. The SI bit is 1 (0) when the SI pin is high (low).
IODW	D8	1-Input	**Digital I/O - Data - Write.** This instruction controls the output levels of those Digital I/O pins configured as outputs according to the input data byte which has the format:- D7 D6 D5 D4 D3 D2 D1 D0 CP1 CP2 CP3 CP4 CP5 R2 R1 R0 If the CPn pin is configured as an output then it will go high or low depending on whether the CPn bit is 1 or 0. If the CPn pin is configured as an input then the corresponding CPn bit should be held at 0 (n = 1, 2, 3, 4, 5). Note the R2-R0 bits are reserved and should be set to 1.

Table 14 Digital I/O and Status Input instructions.

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
PC	B8 to BB	None	**PCM - Code.** This instruction defines the PCM coding scheme used by the device. The instruction has the format:- D7 D6 D5 D4 D3 D2 D1 D0 1 0 1 1 1 0 C1 C0 where C1, C0 select the coding scheme shown by the table:- C1C0 Code 0 0 Linear (16 bits) 0 1 μ-law (8 bits) 1 0 A-law (8 bits) 1 1 Reserved-do not use.
PAR	77	1-Output	**PCM - Association - Read.** The data byte output subsequent to this instruction indicates whether PCM data is associated with the A or B pins (DXA or DXB and DRA or DRB) and with the first or second segment of 256 bits. The data byte has the format:- D7 D6 D5 D4 D3 D2 D1 D0 X X X X R_B X_B R_{SA} X_{SA} $R_B = 1$ means the DRB pin is selected, $R_B = 0$ the DRA pin. $X_B = 1$ means the DXB pin is selected, $X_B = 0$ the DXA pin. If the R_{SA} bit is 0 then the receive segment address is 0 and the receive PCM is associated with the first segment of 256 bits (the standard condition). If it is 1 then the receive PCM is associated with the second segment of 256 bits (Expanded Mode). Likewise, if $X_{SA} = 0$, the segment address is 0 and the transmit PCM is associated with the first segment of 256 bits. If $X_{SA} = 1$ the transmit PCM is associated with the second segment of 256 bits.
PAW	90 to 9F	None	**PCM - Association - Write.** This instruction programs the PCM data association to the A or B pins (DXA or DXB and DRA or DRB) and to the first or second segment of 256 bits. The instruction has the format:- D7 D6 D5 D4 D3 D2 D1 D0 1 0 0 1 R_B X_B R_{SA} X_{SA} $R_B = 1$ selects the DRB pin, $R_B = 0$ selects the DRA pin. $X_B = 1$ selects the DXB pin, $X_B = 0$ selects the DXA pin. If the R_{SA} bit is 0 then the receive segment address is 0 and the receive PCM is associated with the first segment of 256 bits (the standard condition). If it is 1 then the receive PCM is associated with the second segment of 256 bits (Expanded Mode). Likewise, if $X_{SA} = 0$, the segment address is 0 and the transmit PCM is associated with the first segment of 256 bits. If $X_{SA} = 1$ the transmit PCM is associated with the second segment of 256 bits.

Table 15 PCM instructions.

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
DR	B0	None	**Diagnostic - Reset.** This instruction clears any diagnostic conditions that are set up.
DHD	B3	None	**Diagnostic - High Pass Filter - Disable.** This instruction disables the 50/60Hz notch and DC reject filters.
DRA	B1	None	**Diagnostic - Receive - Attenuate.** This instruction adds 6dB attenuation to the Receive Path.
DRD	B2	None	**Diagnostic - Receive - Disable Path.** This instruction disables the Receive Path. This means that $V_{OUT} = V_{OO}$ regardless of the receive PCM data input to the device.
DLA	B7	None	**Diagnostic - Loop - Analog.** This instruction sets the PSLAC to Analog Loop Test Mode which internally switches the transmit signal from D_2 to I_1 (see Fig.3), to the VOUT pin, instead of the normal PCM receive data (Note 1).
DLD	B4	None	**Diagnostic - Loop - Digital.** This instruction sets the PSLAC to Digital Loop Test Mode. The Expander output is switched to the Compressor input such that input PCM replaces the normal PCM output (Note 1).
DCD	B5	None	**Diagnostic - Correlator - Disable.** This instruction disables the signal correlator associated with the adaptive cancellation algorithm. This may be done for test purposes or to allow pre-programming using the measurement method.

NOTES : 1. DLA and DLD are mutually exclusive. Selecting one Loop Test mode resets the other.

Table 16 Diagnostic instructions.

APPLICATIONS

The circuit schematic of Fig. 13 shows the basic application for the MV3010 in a Line Card architecture. This circuit uses one of the Subscriber Line Interface Circuits (SLIC) to interface to the 2-wire (subscriber) Line. For details on how these devices are used to control the line status and transmission parameters, refer to the SL373, SL374, SL376, SL7950 and SL7953 data sheets. Further information is given in Application Note AN82.

Both analog and digital interfacing is shown in Figure 13. The analog input is kept about 0V due to the low impedance output of the SLIC, and the DC bias of the analog output is blocked by the series capacitor, C5. Networks Z_{TX} and Z_{GR} are used to set nominal Transmit and Receive impedances of the Line Card respectively, as discussed in the related documents mentioned earlier. Modifications to gains and frequency response can be carried out in the PSLAC as described in the Functional Description section. Note that in order to ensure the PSLAC meets/exceeds all CCITT transmission parameters (see Electrical Characteristics), the split supply pins are separately routed and decoupled at the system power supplies. This reduces coupling of any digital switching transients into the analog path. Optimum transmission performance is achieved when using the supply decoupling components shown.

The SLIC digital inputs are DC level controlled, TTL compatible and control the SLIC functions as described in the related Data Sheets. Since the PSLAC has latched outputs (programmed as outputs), then these inputs can be directly connected to the PSLAC in any order. The $\overline{DET}$ output of the SLIC can also be connected directly to the PSLAC. Thus, the SLIC operating modes are controlled via the PSLAC I/O pins and the Line Status read via the SI pin. The Line Card is now fully controlled via the PSLAC Control Interface, with microprocessor/controller interface options as described in Application Note AN42.

The PCM Interface can be configured to give a variety of system architectures. This is also discussed further in PABX/Line Card Control Circuit Applications Note AN42.

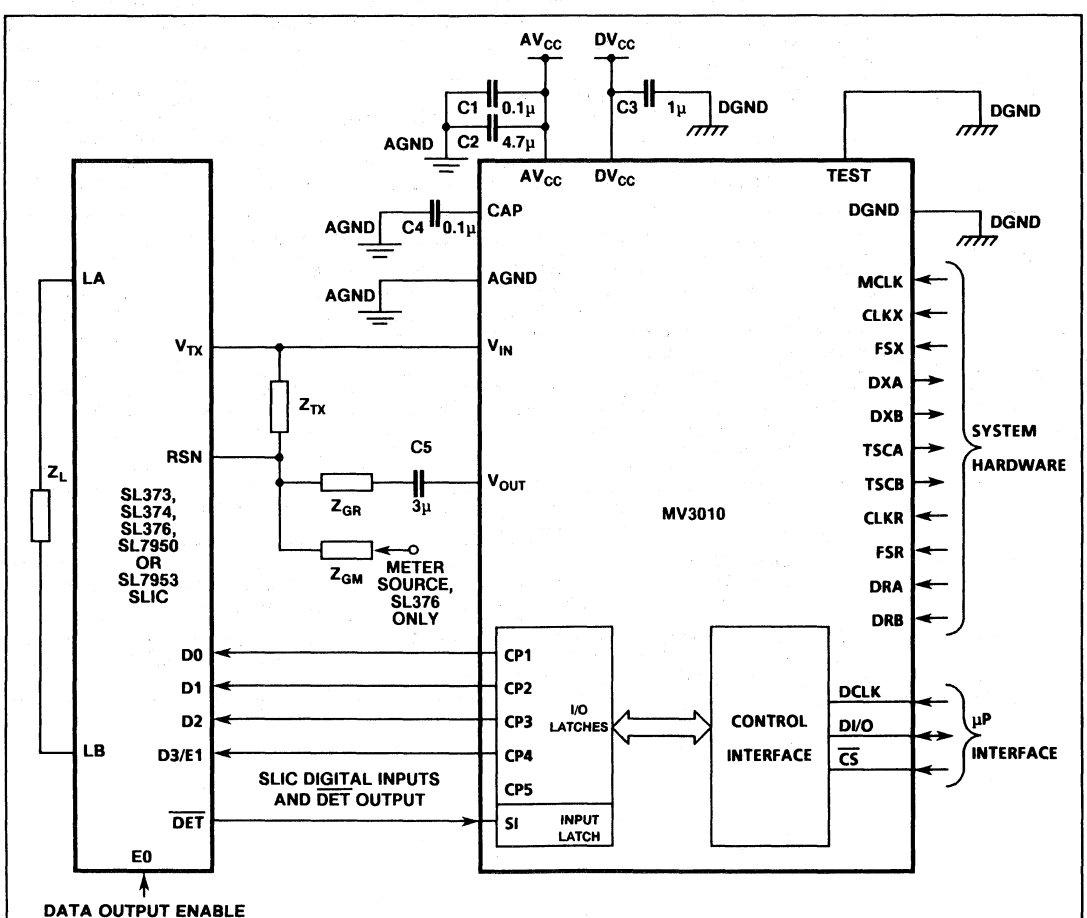


Fig. 13: Line card application circuit showing SLIC interface.

PIN DESCRIPTIONS

Pin name	Pin no.	Pin name and description
CAP	1	**Capacitor (Analog Node).** A capacitor of 0.1µF should be connected between this pin and analog ground (AGND pin). This is used to decouple the internal voltage reference.
V_{IN}	2	**Input Voltage (Analog Input).** The analog voltage input at this pin is sampled, processed, digitally encoded and then output as PCM data on either DXA or DXB. This signal is referenced to AGND and there is an input impedance of 30kΩ to $\frac{1}{2}V_{REF}$ (≈1.66V).
AGND	3	**Analog Ground (Power Input).** This is the ground reference pin for the analog input (V_{IN} pin) and analog output (V_{OUT} pin). Care should be taken to minimise the noise at this pin.
V_{OUT}	4	**Output Voltage (Analog Output).** The analog voltage at this pin is derived from the PCM data input on either DRA or DRB. This PCM data is processed digitally, decoded, converted to analog and then output here. This signal is referenced to AGND but has a DC offset of nominally 2.5V.
SI	5	**Status In (Digital Input).** The data sampled at this input can be read out on the DI/O pin. This allows information about the status of the telephone line to be passed on to a line card controller. This pin can also be used to control the operation of the C-Filter (see Table 10).
CP1 CP2 CP3 CP4 CP5	6 7 8 9 10	**Control Port 1 to 5 (Digital I/O with Pullups).** These pins are independently programmable as either inputs or outputs through the control stream input on DI/O. Pins which are programmed as outputs are also controlled by DI/O. Pins which are programmed as inputs can be read on DI/O. There are pullups of 150kΩ on these pins. These pins allow a line card controller to monitor and control the line card via the PSLAC and mean that a single hardware design for a line card can be configured through software for a number of different requirements.
TSCA TSCB	11 18	**Time Slot Control A, B (Open Drain Pulldown Outputs).** The TSCA or TSCB pins are pulled low when PCM data is output on DXA or DXB respectively. These pins on different devices may be connected together with a single pull-up resistor (wire-ored) to generate an enable signal for an output buffer on a line card.
DXA DXB	12 17	**Digital Transmit A, B (Three-State Outputs).** These are the PCM data outputs, which can be 8 bit µ-law, 8 bit A-law or 16 bit linear code. Either DXA or DXB is used as programmed via the serial control input at DI/O. Bit and frame synchronisation are established by CLKX and FSX with the start of the PCM burst relative to FSX determined by serial Control Codes via DI/O. A PCM data word is output once every 125µs, with the pins high impedance between PCM bursts and in Power-Down Mode.
TEST	13	**Test Pin (Internal Connection).** This pin must be connected to DGND during normal operation.
DRA DRB	14 21	**Digital Receive A, B (Digital Inputs).** These are the PCM data inputs, which can be 8 bit µ-law, 8 bit A-law or 16 bit linear coding. Either DRA or DRB is used as programmed via the serial control input at DI/O. Bit and frame synchronisation are established by CLKR and FSR, with the position of the first sampled bit relative to FSR determined by serial Control Codes via DI/O. A data word is sampled once every 125µs.
CLKX	15	**Transmit Clock (Digital Input).** The clock input at this pin establishes bit synchronisation of the PCM data output on DXA and DXB. The clock frequency must be between 64kHz and 4.096MHz and there must be an integral number of clock cycles between pulses on FSX. This clock should be phase locked to MCLK.
FSX	16	**Transmit Frame Synchronisation (Digital Input).** The pulse input at this pin establishes the frame synchronisation of the PCM data output on DXA and DXB. There should be 125µs between pulses and the pulses should be synchronised with CLKX.
CLKR	19	**Receive Clock (Digital Input).** The clock input at this pin strobes the samples of PCM data input on DRA and DRB. The clock frequency must be between 64kHz and 4.096MHz with an integral number of cycles between FSR pulses. This clock should be phase locked to MCLK.
FSR	20	**Receive Frame Synchronisation (Digital Input).** The pulse input at this pin establishes the frame synchronisation on the PCM data input on DRA and DRB. There should be 125µs between pulses and the pulses should be synchronised with CLKR.

PIN DESCRIPTIONS (continued)

Pin name	Pin No.	Pin name and description
DGND	22	**Digital Ground (Power Input).** 0V supply.
$\overline{CS}$	23	**Chip Select (Digital Input).** This input should be taken low to enable the chip to input or output serial Control or Data bytes, via DI/O, when strobed with DCLK. If held low for more than 8 cycles of DCLK it will force the device into stand-alone operation.
DI/O	24	**Data In/Out (Digital Input/Output).** Serial Control Codes and Data Bytes are input and output via this pin when $\overline{CS}$ is low. Input data is sampled by DCLK and output data is clocked out by DCLK. A common data input/output line can be used by a number of devices.
DCLK	25	**Data Clock (Digital Input).** This clock strobes serial input and clocks serial output data via DI/O, in association with the $\overline{CS}$ pin. The clock can run at frequencies from DC to 2.048MHz.
MCLK	26	**Master Clock (Digital Input).** This clock controls the sampling for the A/D conversion, signal reconstruction for the D/A conversion, the DSP functions and must be 2.048MHz phase locked with CLKX and CLKR.
DV_{CC}	27	**Digital Positive Supply Voltage (Power Input).** +5V.
AV_{CC}	28	**Analog Positive Supply Voltage (Power Input).** +5V.

RECOMMENDED OPERATING CONDITIONS

Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value			Units
		Min.	Typ.	Max.	
Analog supply voltage	AV_{CC}	4.75	5	5.25	V
Digital ground voltage	V_{DGND}	−0.1	0	0.1	V
Digital supply voltage	DV_{CC}	4.75	5	5.25	V
Ambient temperature	T_{AMB}	0		70	°C
Output loading	C_O			150	pF

ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless otherwise specified) :-

Supply Characteristics -Voltages are with respect to analog ground (V_{AGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Active supply current (power-up mode)	I_{CCA}		30	45	mA	Unloaded
Standby supply current (power-down mode)	I_{CCS}		6	8	mA	Unloaded
Analog power supply (AV_{CC}) rejection ratio, V_{IN}/V_{OUT}	P_{SRA}		50		dB	f = 1.02kHz, 100mV p-p on supply, Note 1.
Digital power supply (DV_{CC}) rejection ratio, V_{IN}/V_{OUT}	P_{SRD}		50		dB	f = 1.02kHz, 100mV p-p on supply, Note 1.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Notes 1. For Transmit Path the digital output signal is converted to an equivalent signal amplitude at V_{IN}.

Analog Static Characteristics - Voltages are with respect to analog ground (V_{AGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Pin capacitance	C_P		8	10	pF	$0<V<AV_{CC}$, DV_{CC}
V_{IN} input impedance	Z_I	20	30		kΩ	$-3V<V<+3V$
V_{IN} input bias	V_{BI}		$\frac{2}{3}V_{REF}$		V	V_{REF} Internal Reference = 2.5V, V_{IN} = O/C
V_{IN} input offset voltage	V_{IO}	−5		+5	mV	Note 1.
V_{IN} input voltage range	V_{IA}	−3		+3	V	
V_{OUT} output impedance	Z_O			20	Ω	$1V<V<4V$
V_{OUT} output offset voltage	V_{OO}	2.3	2.5	2.7	V	
V_{OUT} output voltage range	V_{OA}	$V_{OO}-1.5$		$V_{OO}+1.5$	V	$R_L = 10k\Omega$, $C_L = 50pF$

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Notes. 1. Full functional operation is possible with $-0.25V \leq V_{IO} \leq +0.25V$, full transmission performance is not guaranteed.

Analog Dynamic Characteristics - Voltages are with respect to analog ground (V_{AGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Absolute gain	G_{ABS}	−0.15		+ 0.15	dB	Transmit or Receive Path, f = 1.02kHz sine, 0dBm0 Signal Level
Transmit 0dBm0 level	V_{TO}	4.11 4.08	4.18 4.15	4.25 4.22	$V_{P/P}$	A-Law μ-Law
Receive 0dBm0 level	V_{RO}	2.05 2.04	2.09 2.075	2.12 2.11	$V_{P/P}$	A-Law μ-Law
Transmit gain	G_T			13	dB	All CCITT G.714 Specifications - as listed in the following rows
Receive gain	G_R	−12			dB	All CCITT G.714 Specifications - as listed in the following rows
Frequency response, transmit (As CCITT G.714.7, see Figure 14) f = 0Hz = 50 = 60 = 200 = 300-3000 = 3300 = 3400 = 4000 >4600	FR_T	- - - −1.0 −0.125 −0.35 −0.8 - -		−80 −25 −25 0.0 + 0.125 + 0.125 0.0 −17.5 −35.0	dB dB dB dB dB dB dB dB dB	Note 1, Note 3, Reference = 1kHz 0dBm0 signal level.
Frequency response receive (As CCITT G.714.7,see Figure 14) f = 0Hz = 200 = 300-3000 = 3300 = 3400 = 4000 >4600	FR_R	- −1.0 −0.125 −0.35 −0.8 - -		−80 0.0 + 0.125 + 0.125 0.0 −17.5 −35.0	dB dB dB dB dB dB dB	Note 2, Note 3, Reference = 1kHz 0dBm0 signal level.
Absolute group delay, transmit	GD_{AT}			360	μs	Note 1, Note 3, Min. delay 1kHz to 2.6kHz
Absolute group delay, receive	GD_{AR}			240	μs	Note 2, Note 3, Min. delay 1kHz to 2.6kHz
Delay distortion, transmit (Figure 15) f = 500-600Hz = 600-1000 = 1000-2600 = 2600-2800	DD_T			700 350 120 700	μs μs μs μs	Note 1, Note 3, Relative to the minimum delay of the transmit side.
Delay distortion, receive (Figure 15) f = 500-600Hz = 600-1000 = 1000-2600 = 2600-2800	DD_R			700 350 120 700	μs μs μs μs	Note 2, Note 3, Relative to the minimum delay of the receive side.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Notes:- 1. G_X = 0 to + 13dB.

2. G_R = 0 to −12dB.

3. All programmable filters disabled.

Analog Dynamic Characteristics - continued - Voltages are with respect to analog ground (V_{AGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Idle channel noise, transmit	NI_{TA} $NI_{T\mu}$			−67 −75	dBm0p dBm0p	A-law Psophometrically μ-law Weighted, Note 1.
Idle Channel Noise, Receive	NI_R			−84	dBmp	Psophometrically Weighted, Note2, Note 6.
Out of band signal rejection 4600Hz-30kHz, transmit	RJ_{TH}	35			dB	Note 1, V_{IN} = −25dBm0
Out of band signal generation, receive 4600Hz-100kHz	GN_{RH}			−35	dBm0	Note 2, PCM In 0dBm0, 300-3400Hz
Spurious In band signals, transmit	GN_{TL}			−46	dB	Applied f = 700-1100Hz, 0dBm0, Note 1.
Spurious In band signals, receive	GN_{RL}			−46	dB	Applied f = 700-1100Hz, 0dBm0, Note 2.
Transmit gain variation with level, sinusoid input (As CCITT G.714.15 method 2, see Figure 16)	G_{XLS}	−0.2 −0.4 −1.2		+ 0.2 + 0.4 + 1.2	dB dB dB	+ 3 to −40dBm0 }−10dBm0 −40 to −50dBm0 }Ref. −50 to −55dBm0 }Level. Note 1, Note 3, Note 4.
Transmit gain variation with level, band limited noise (CCITT O.131) input (As CCITT G.714.15 method 1, see Figure 17)	G_{XLN}	−0.2 −0.4		+ 0.2 + 0.4	dB dB	−10 to −55dBm0 }−10dBm0 −55 to −60dBm0 }Ref.Level Note 3, Note 5.
Transmit gain variation with level, band limited noise (CCITT O.131) input (As CCITT G.714.15 method 1, see Figure 17)	G_{XLNA}	−0.2 −0.4		+ 0.2 + 0.4	dB dB	−10 to −50dBm0 }−10dBm0 −50 to −60dBm0 }Ref.Level + 12dB < $G_X \leq$ + 13dB, Note 3.
Receive gain variation with level , sinusoid input (As CCITT G.714.15 method 2, see Figure 16)	G_{RLS}	−0.2 −0.4 −1.2		+ 0.2 + 0.4 + 1.2	dB dB dB	+ 3 to −40dBm0 }−10dBm0 −40 to −50dBm0 }Ref. −50 to −55dBm0 }Level. Note 2, Note 3, Note 4.
Receive gain variation with level, band limited noise (CCITT O.131) input (As CCITT G.714.15 method 1, see Figure 17)	G_{RLN}	−0.2 −0.4		+ 0.2 + 0.6	dB dB	−10 to −50dBm0 }−10dBm0 −50 to −55dBm0 }Ref.Level Note 2, Note 3.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Notes:- 1. G_X = 0 to + 13dB.
2. G_R = 0 to −12dB.
3. All programmable filters are disabled.
4. Non-production test. Figures are included for guidance only.
5. G_X = 0 to + 12dB.
6. μ-Law coding = + 0 code, A-Law coding = + 1 code.

Analog Dynamic Characteristics - continued - Voltages are with respect to analog ground (V_{AGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Transmit gain variation with supplies	G_{XVCC}		0.05		dB/V	$AV_{CC} \pm 5\%$, $DV_{CC} \pm 5\%$, Note 1.
Receive Gain Variation with Supplies	G_{RVCC}		0.05		dB/V	$AV_{CC} \pm 5\%$, $DV_{CC} \pm 5\%$, Note 2.
Transmit gain variation with temperature	G_{XTMP}	−0.1		+ 0.1	dB	T_A = 0-70°C, Note 1.
Receive gain variation with temperature	G_{RTMP}	−0.1		+ 0.1	dB	T_A = 0-70°C, Note 2.
Signal to Total distortion ratio transmit, noise (CCITT O.131) input (As CCITT G.714.14 method 1, see Figure 19)	STD_{TX1}	26.8 34.4 32.7 28.1 13.1			dB dB dB dB dB	−3dBm0 } −6 to −27dBm0 }Note 1, −34dBm0 }Note 3. −40dBm0 } −55dBm0 }
Signal to total distortion ratio transmit, sinusoid input. (As CCITT G.714.14, method 2, see Figure 18)	STD_{TX2}	35 29 24			dB dB dB	0 to −30dBm0 } −40dBm0 }f = 1020Hz −45dBm0 } Note 1, Note 3, Note 4.
Signal to total distortion ratio receive, noise (CCITT O.131) input (As CCITT G.714.14, method 1, see Figure 19)	STD_{RX1}	27.8 35.4 33.7 29.1 14.1			dB dB dB dB dB	−3dBm0 } −6 to −27dBm0 }Note 2, −34dBm0 }Note 3. −40dBm0 } −55dBm0 }
Signal to total distortion ratio receive, sinusoid input. (As CCITT G.714.14 method 2, see Figure 18)	STD_{RX2}	36 30 25			dB dB dB	0 to −30dBm0 } −40dBm0 }f = 1020Hz −45dBm0 } Note 2, Note 3, Note 4.
Crosstalk, transmit to receive	XT_{TR}			−60	dB	Note 1, Note 2, Note 3.
Crosstalk, receive to transmit	XT_{RT}			−60	dB	Note 1, Note 2, Note 3.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Notes:- 1. G_X = 0 to + 13dB.
2. G_R = 0 to −12dB.
3. All programmable filters are disabled.
4. Non-production test. Figures are included for guidance only.

Digital Static Characteristics - Voltages are with respect to digital ground (V_{DGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Input leakage current	I_{IL}			10	µA	$0<V<DV_{CC}$
Output high voltage	V_{OH}	2.4		DV_{CC}	V	I_{OH} (Source) = –400µA
Output low voltage	V_{OL}	0		0.4	V	I_{OL} (Sink) = 2mA
Output leakage current	I_{OL}			10	µA	$0<V<DV_{CC}$
Input high voltage	V_{IH}	2.0	2.4	DV_{CC}	V	
Input low voltage	V_{IL}	0	0.4	0.8	V	

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Digital Dynamic Characteristics - Voltages are with respect to digital ground (V_{DGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Master clock period	t_{MCP}	0.48826	0.48828	0.48831	µs	Figure 20.
Master clock rise time	t_{MR}		20		ns	Figure 20.
Master clock high time	t_{MH}	50	236		ns	Figure 20.
Master clock fall time	t_{MF}		20		ns	Figure 20.
Master clock low time	t_{ML}	50	236		ns	Figure 20.
Transmit PCM clock period	t_{TCP}	244	488	15626	ns	Figure 22.
Transmit PCM clock rise time	t_{TCR}			20	ns	Figure 22.
Transmit PCM clock high time	t_{TCH}	100			ns	Figure 22.
Transmit PCM clock fall time	t_{TCF}			20	ns	Figure 22.
Transmit PCM clock low time	t_{TCL}	100			ns	Figure 22.
Transmit PCM frame sync. set-up time	t_{TFS}	50			ns	Figure 22.
Transmit PCM frame sync. hold time	t_{TFH}	30			ns	Figure 22.
Transmit PCM active delay	t_{TAD}	70		170	ns	Figure 22.
Transmit PCM passive delay	t_{TPD}			70	ns	Figure 22.
Transmit PCM output hold time	t_{TOH}	30			ns	Figure 22.
Transmit PCM output delay	t_{TOD}			100	ns	Figure 22.
TSC low delay	t_{TLD}			150	ns	Figure 22.
TSC high delay	t_{THD}			150	ns	Figure 22.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Digital Dynamic Characteristics - continued - Voltages are with respect to digital ground (V_{DGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Receive PCM clock period	t_{RCP}	244	488	15626	ns	Figure 21.
Receive PCM clock risetime	t_{RCR}			20	ns	Figure 21.
Receive PCM clock high time	t_{RCH}	100			ns	Figure 21.
Receive PCM clock fall time	t_{RCF}			20	ns	Figure 21.
Receive PCM clock low time	t_{RCL}	100			ns	Figure 21.
Receive PCM frame sync set-up time	t_{RFS}	50			ns	Figure 21.
Receive PCM frame sync. hold time	t_{RFH}	30			ns	Figure 21.
Receive PCM input set-up time	t_{RIS}	50	$\frac{1}{2}t_{RCP}$		ns	Figure 21.
Receive PCM input hold time	t_{RIH}	30	$\frac{1}{2}t_{RCP}$		ns	Figure 21.
Data clock period	t_{DCP}	450			ns	Figures 23 & 24.
Data clock rise time	t_{DCR}		25	50	ns	Figures 23 & 24.
Data clock high time	t_{DCH}	150			ns	Figures 23 & 24.
Data clock fall time	t_{DCF}		25	50	ns	Figures 23 & 24.
Data clock low time	t_{DCL}	150			ns	Figures 23 & 24.
$\overline{CS}$ falling hold time	t_{CFH}	150			ns	Figures 23 & 24.
$\overline{CS}$ falling set-up time	t_{CFS}	50			ns	Figures 23 & 24.
$\overline{CS}$ rising hold time	t_{CRH}	50			ns	Figures 23 & 24.
$\overline{CS}$ rising set-up time	t_{CRS}	50			ns	Figures 23 & 24.
$\overline{CS}$ low time	t_{CLT}		$8t_{DCP}$		ns	Figures 23 & 24, Note 1.
$\overline{CS}$ high time, input mode	t_{CIT}	$7 \times t_{MCP}$			ns ns	Command or data codes } Figure 23.
$\overline{CS}$ high time, output mode	t_{COT}	$7 \times t_{MCP}$			ns ns	Command or data codes } Figure 24.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Notes:- 1. If $\overline{CS}$ is tied low then the MV3010 will operate in Stand Alone Mode.

Digital Dynamic Characteristics - continued - Voltages are with respect to digital ground (V_{DGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
DI/O input set-up time	t_{DIS}	50	$t_{DCP}/2$		ns	Figure 23.
DI/O input hold time	t_{DIH}	30	$t_{DCP}/2$		ns	Figure 23.
DI/O active delay	t_{DAD}			100	ns	Figure 24.
DI/O passive delay	t_{DPD}			100	ns	Figure 24.
DI/O output hold time	t_{DOH}	30	50		ns	Figure 24.
DI/O output delay	t_{DOD}		100	150	ns	Figure 24.
CP1-CP5 I/O output mode, data false delay Time	t_{LOF}	0			ns	Figure 25.
CP1-CP5 I/O output mode, data valid delay Time	t_{LOV}			$4 \times t_{MCP}$	ns	Figure 25.
CP1-CP5 I/O input mode and SI pin, data set-up time	t_{LIS}	0			ns	Figure 25.
CP1-CP5 I/O input mode and SI pin, data hold time	t_{LIH}	$4 \times t_{MCP}$			ns	Figure 25.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

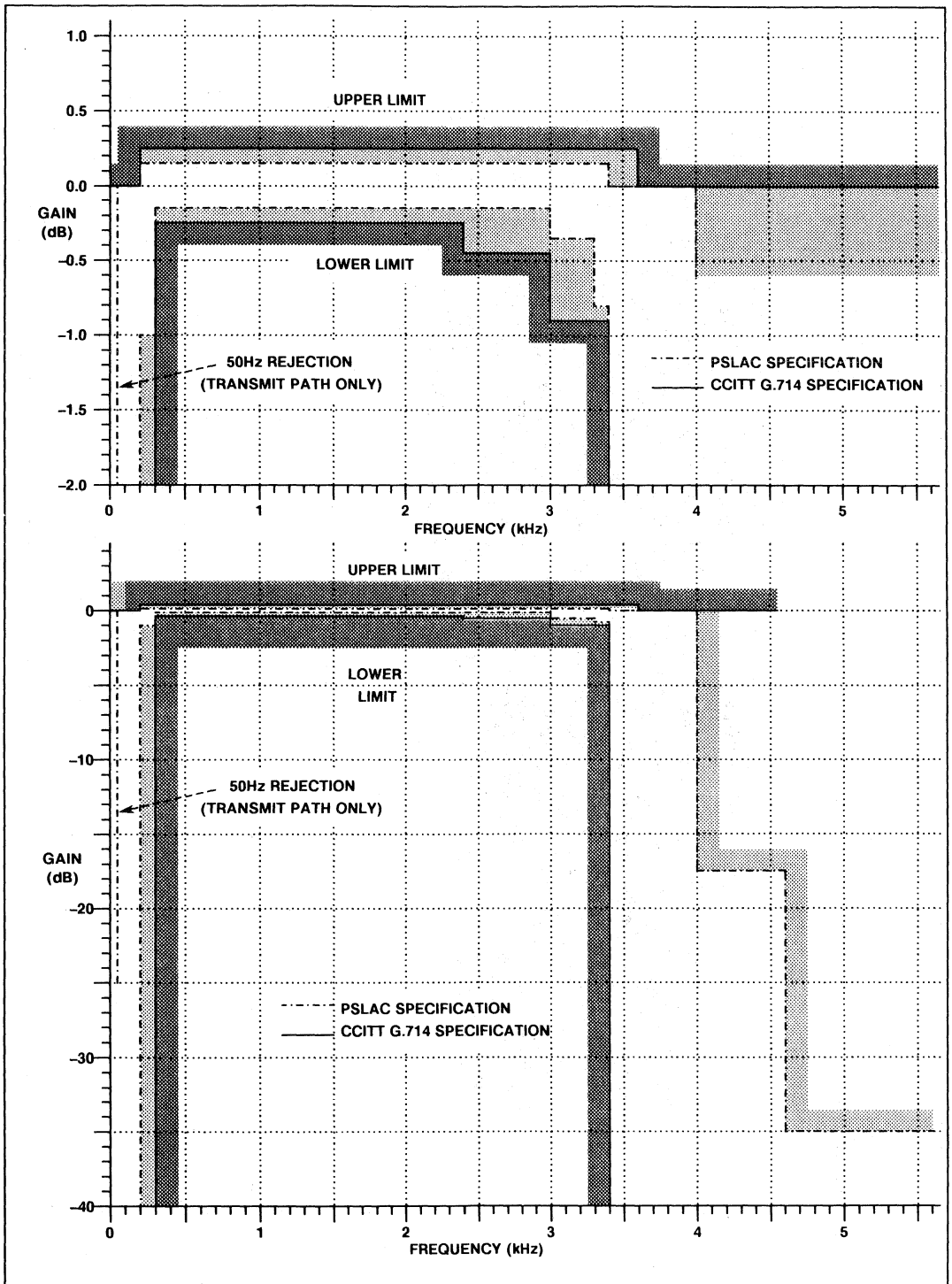


Fig. 14 PSLAC frequency response.

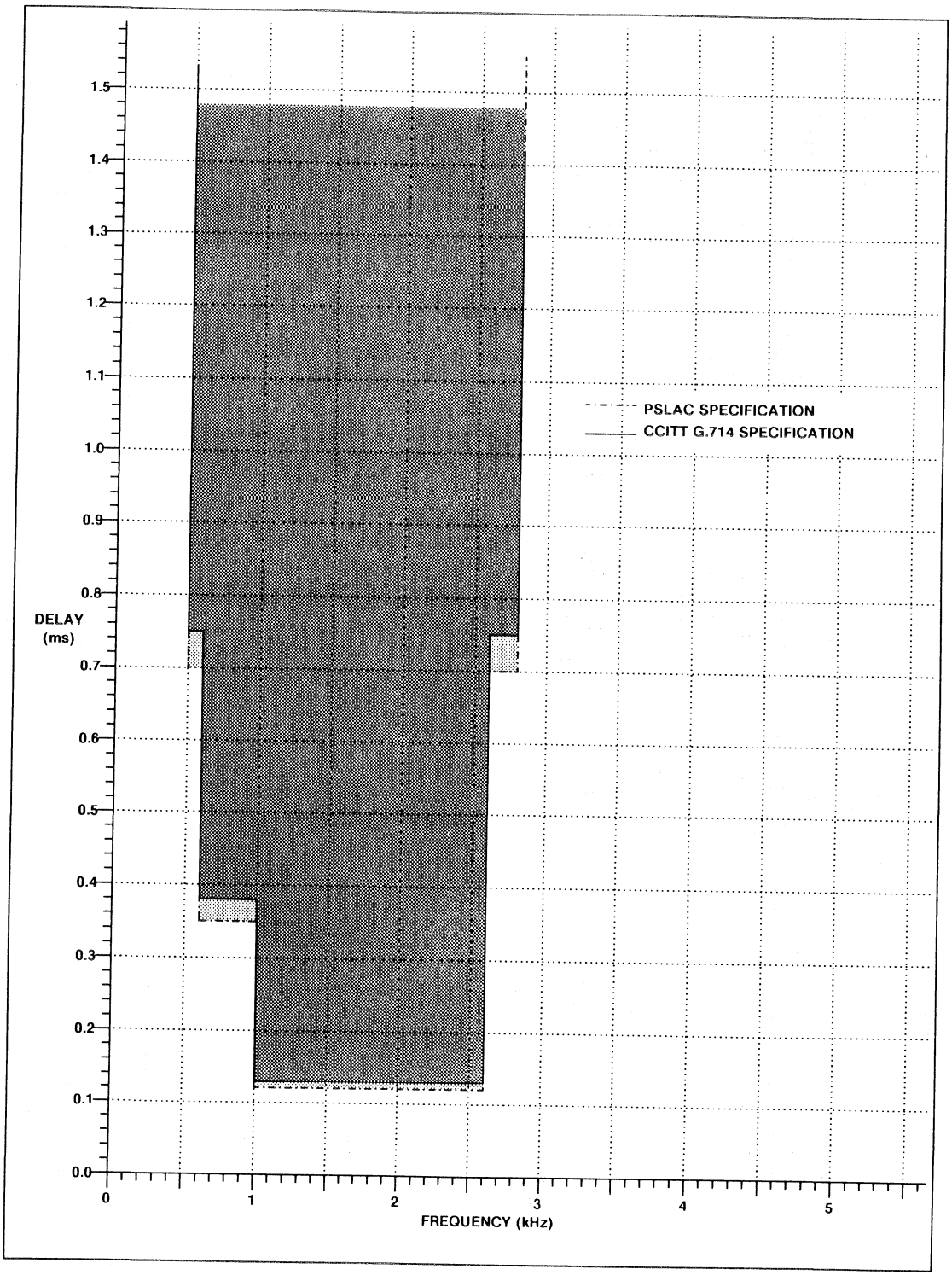


Fig.5 PSLAC delay distortion v. frequency.

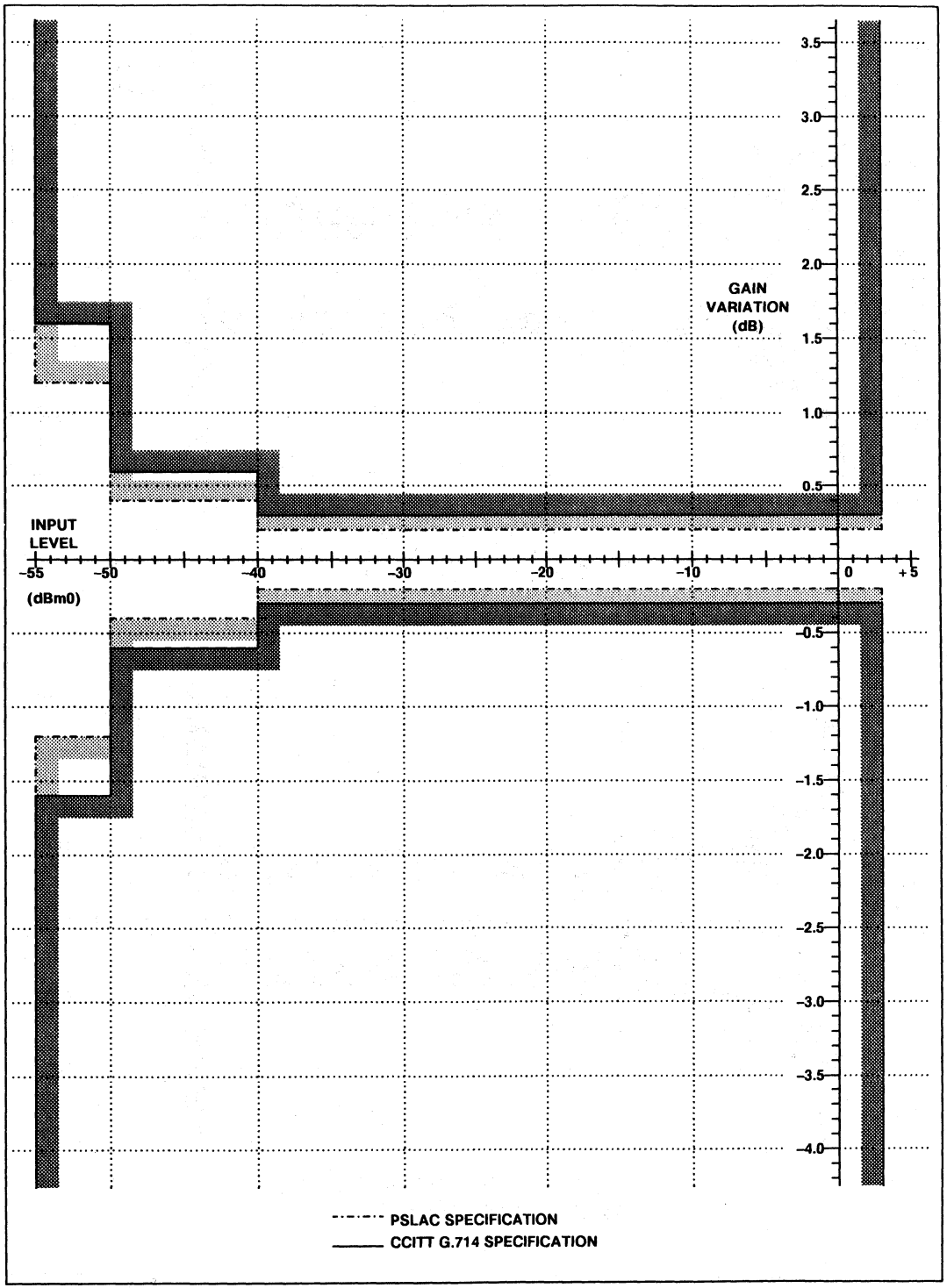


Fig. 16 PSLAC gain variation v. level (sinusoid - Method 2 CCITT G.714.15).

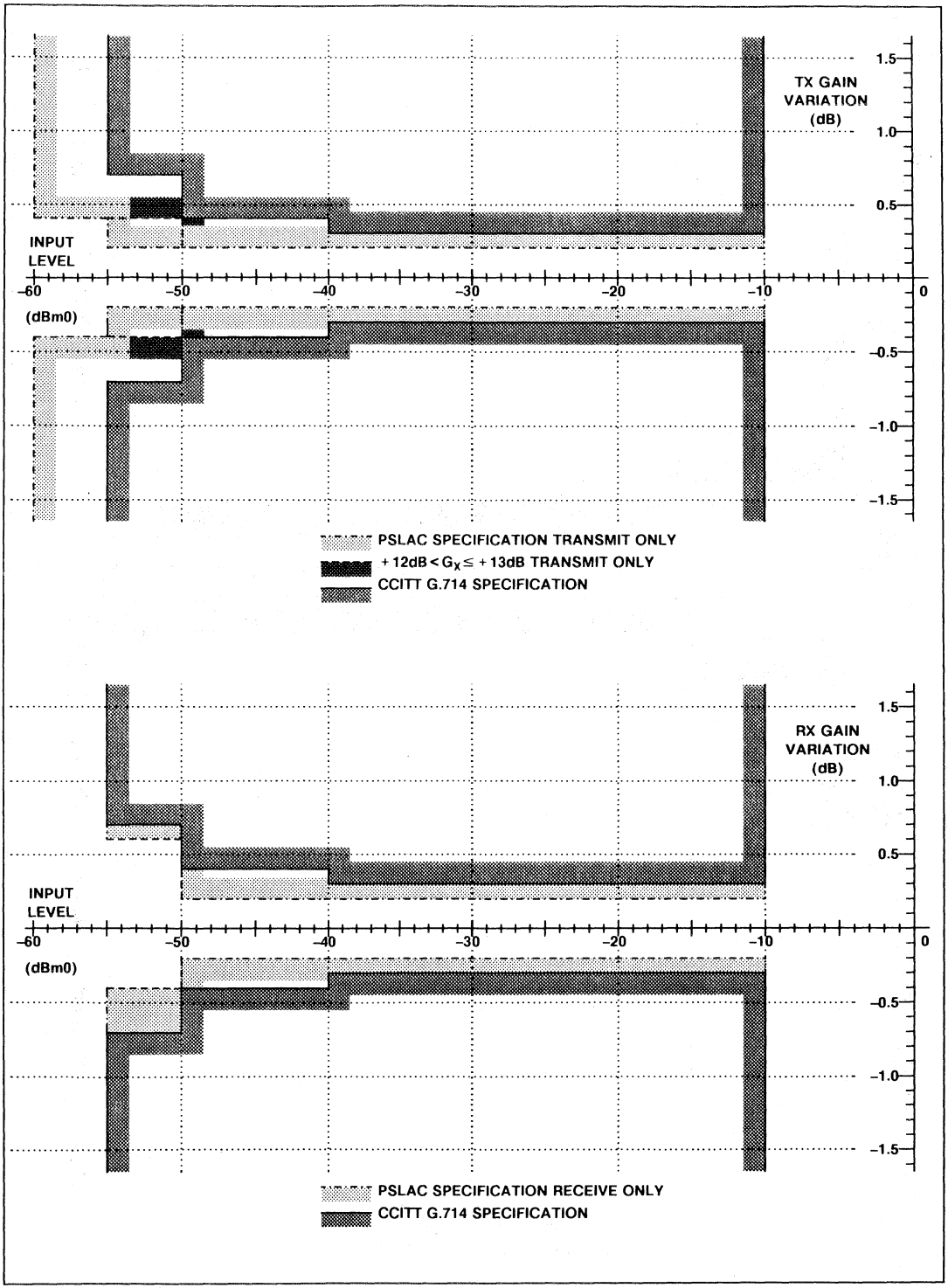


Fig.17 PSLAC gain variation v. level (Noise, O.131 - Method 1 CCITT G.714.15).

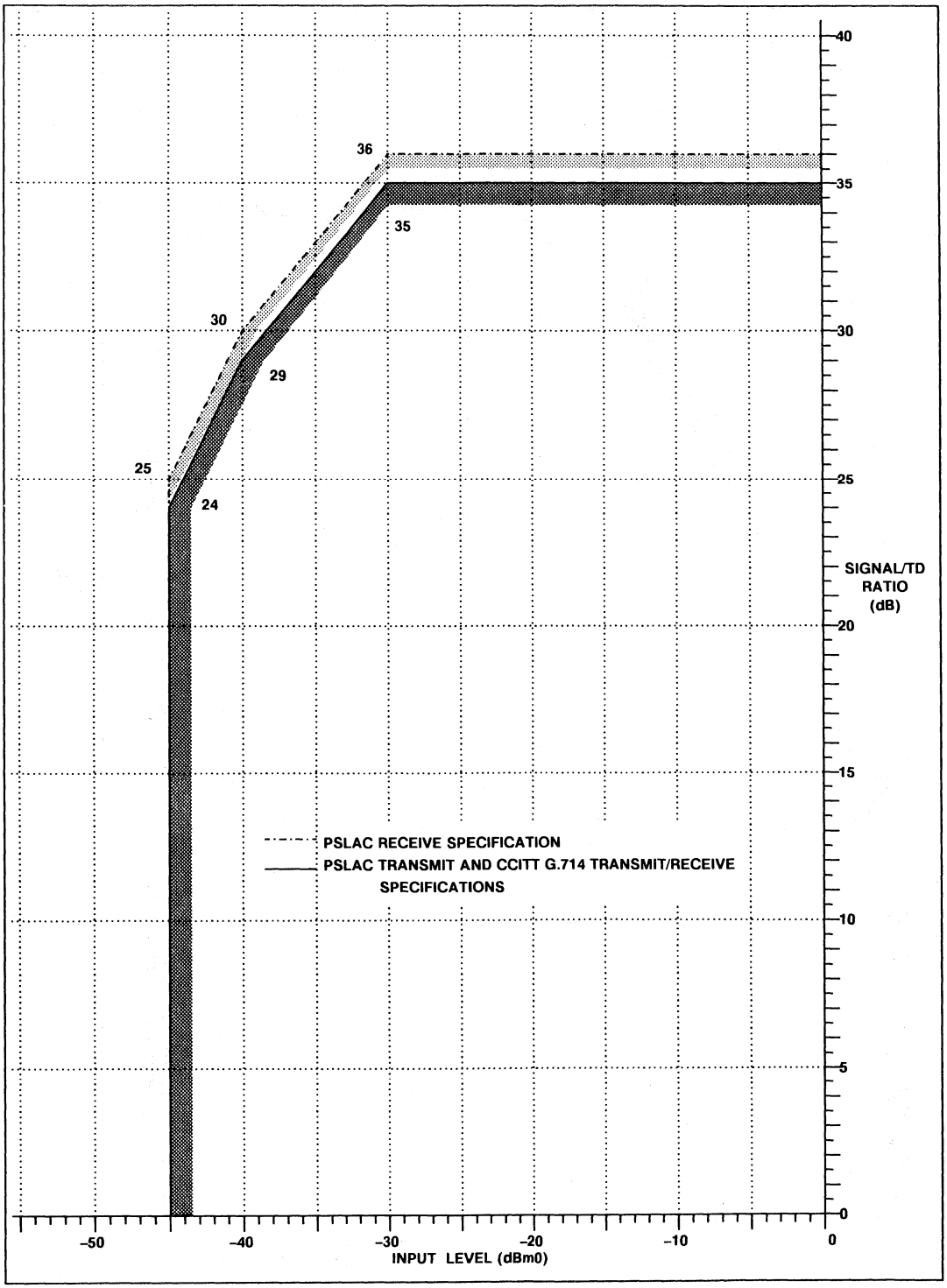


Fig.18 PSLAC signal to total distortion ratio v. level (Sinusoid Method 2 CCITT G.714.14).

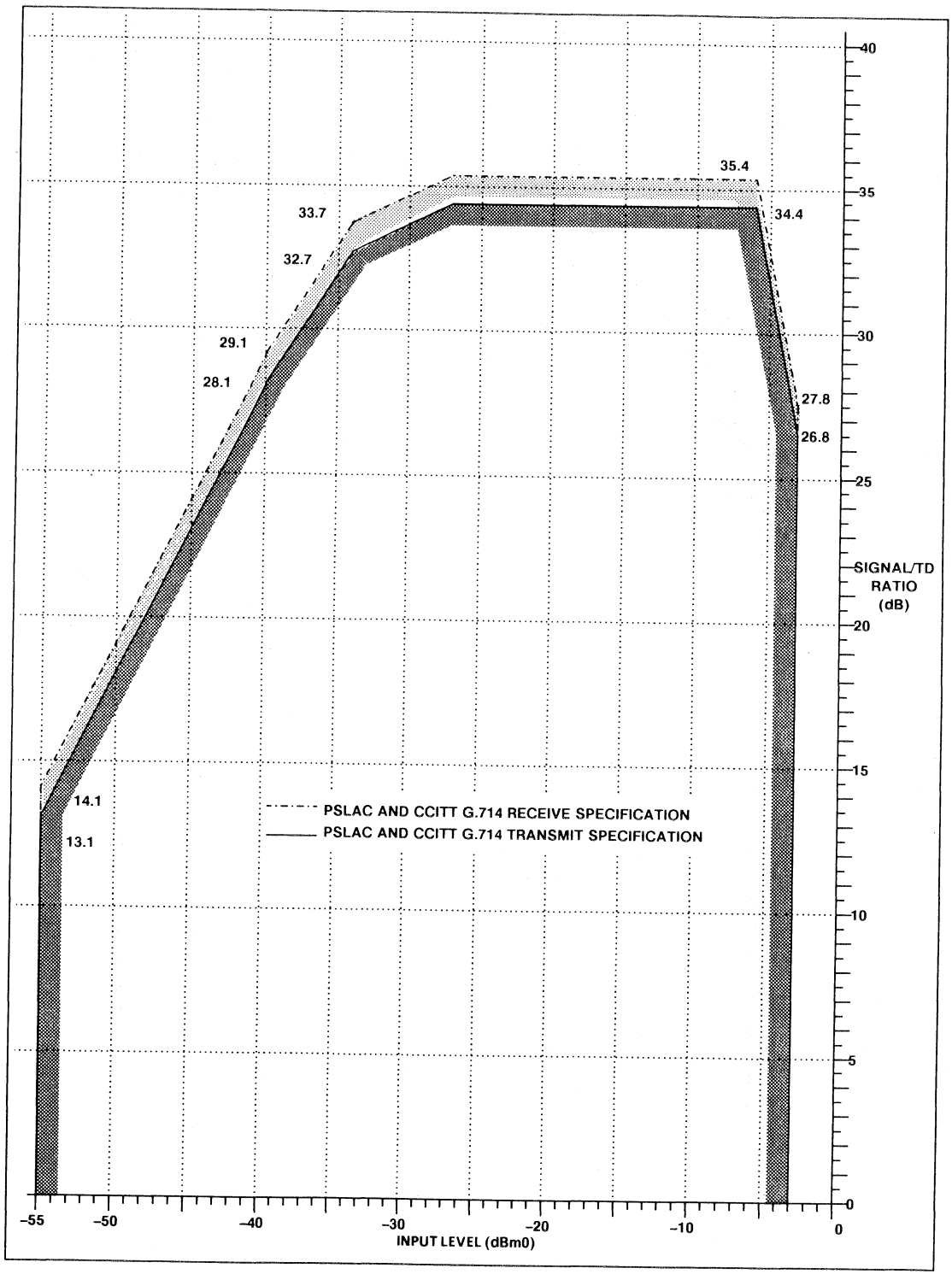


Fig.19 : PSLAC signal to total distortion ratio v. level (Noise, 0.131 - Method 1 CCITT G.714.14).

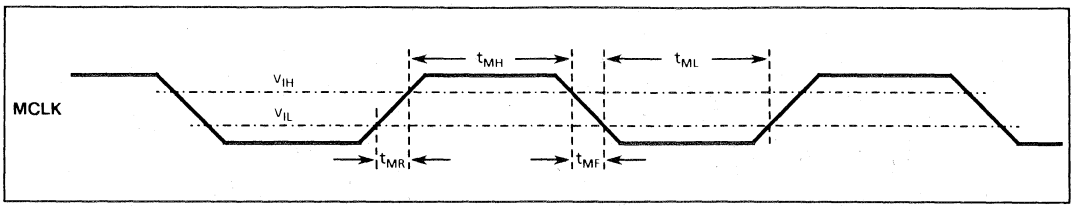


Fig.20 Master clock timing diagram.

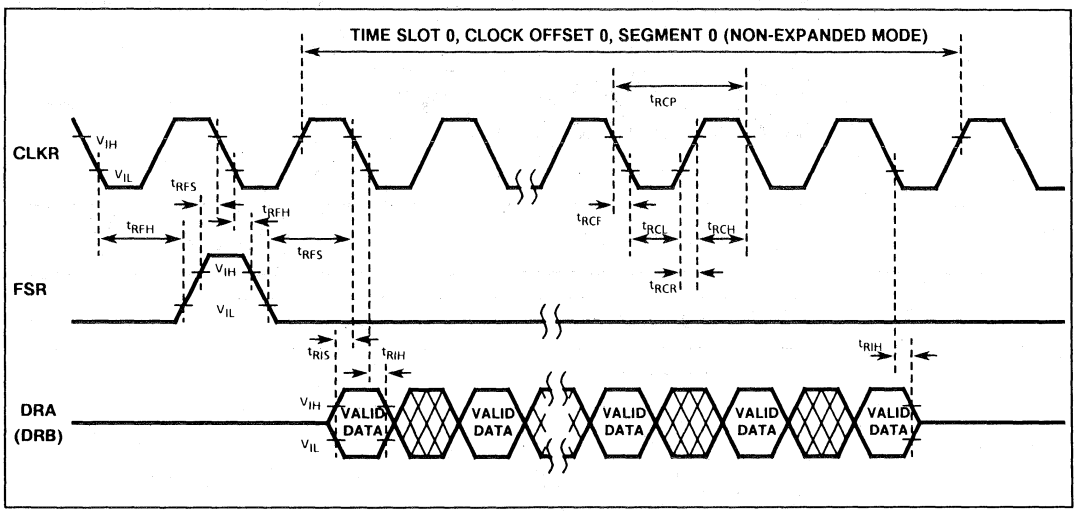


Fig.21 PCM data receive timing diagram.

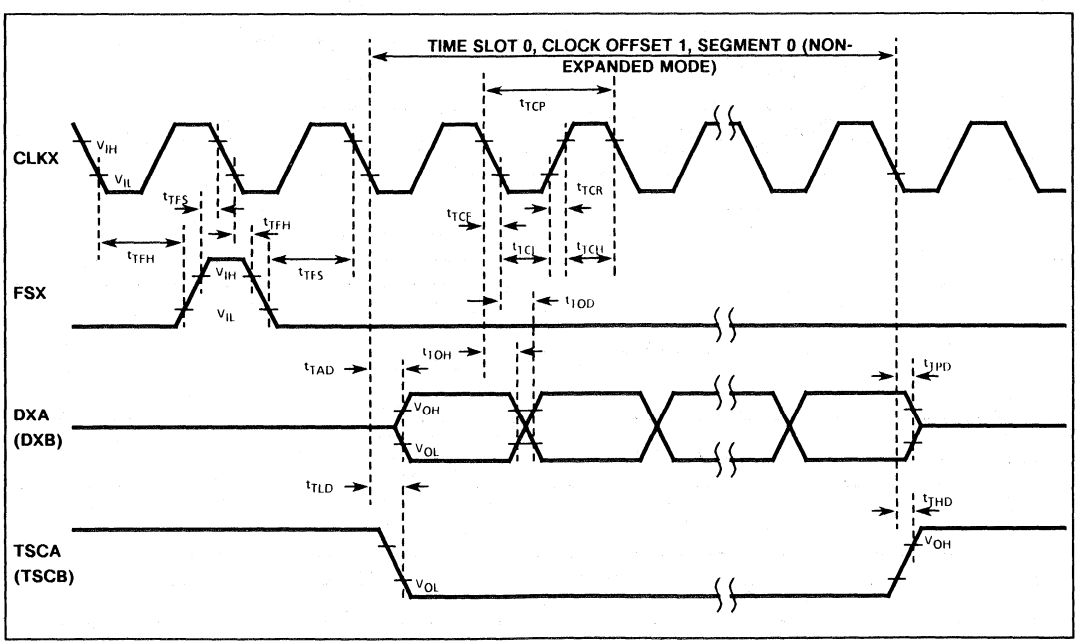


Fig.22 PCM data transmit timing diagram.

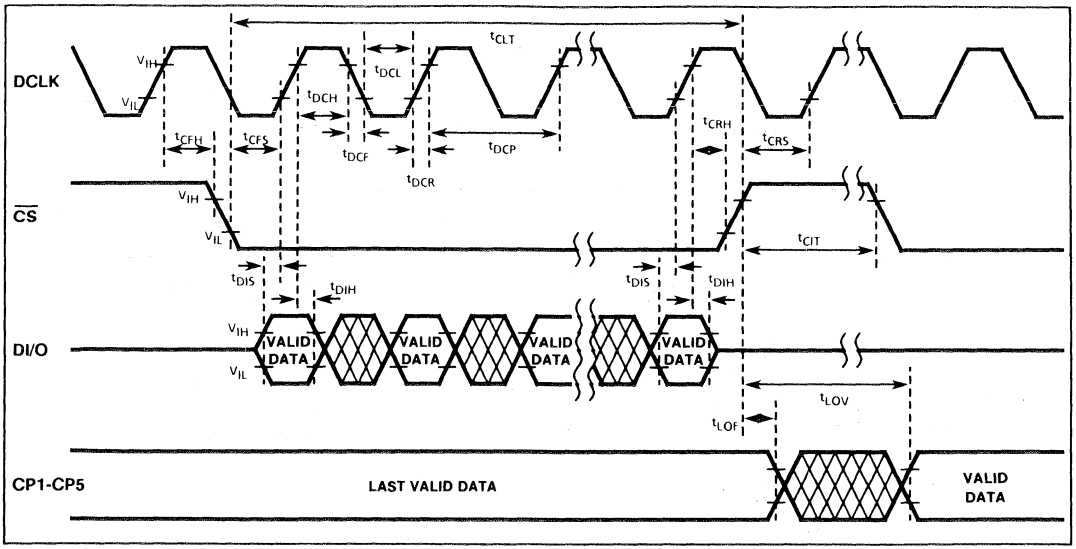


Fig.23 Control interface input data timing diagram.

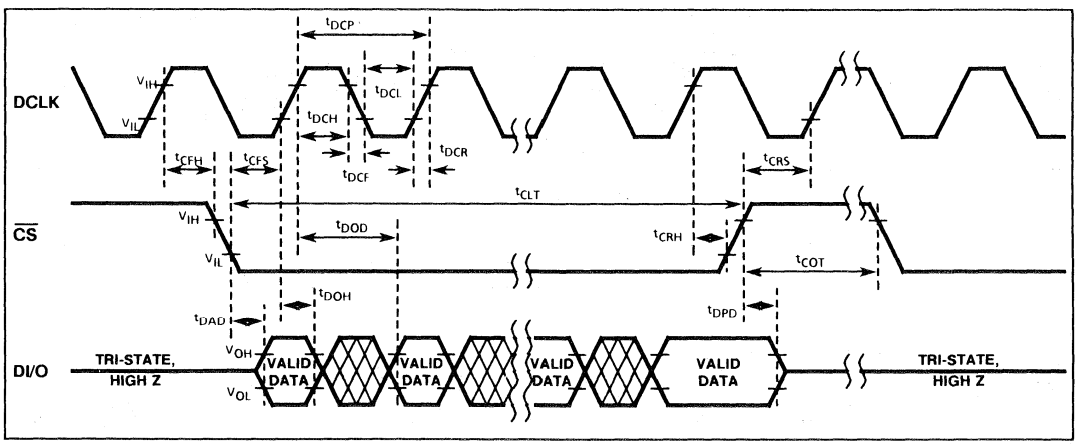


Fig.24 Control interface output data timing diagram.

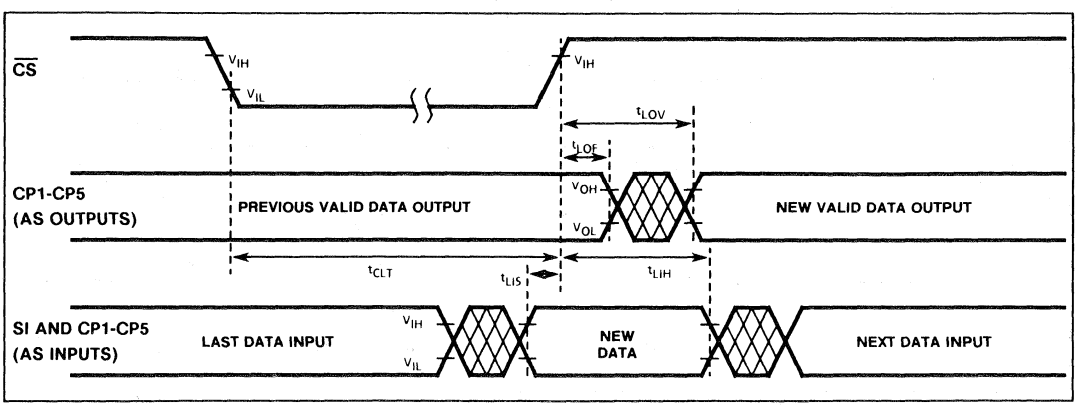


Fig.25 I/O latches and SI timing diagram.

ABSOLUTE MAXIMUM RATINGS

Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value		Units
		Min.	Max.	
Analog supply voltage	AV_{CC}	−0.5	+ 5.7	V
Digital supply voltage	DV_{CC}	−0.5	+ 5.7	V
Storage temperature	T_S	−65	+ 125	°C
Input voltage - except V_{IN} pin	V_I	−0.3	DV_{CC} + 0.3	V
Input voltage - V_{IN} pin	V_{VIN}	−3.3	+ 3.3	V
Output voltage - except V_{OUT} pin	V_O	−0.3	DV_{CC} + 0.3	V
Output voltage - V_{OUT} pin	V_{VOUT}	−0.3	AV_{CC} + 0.3	V
Clamp current (sink or source beyond power supply)	I_K		100	mA
Package power dissipation	P_P		800	mW

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

PCBAN111

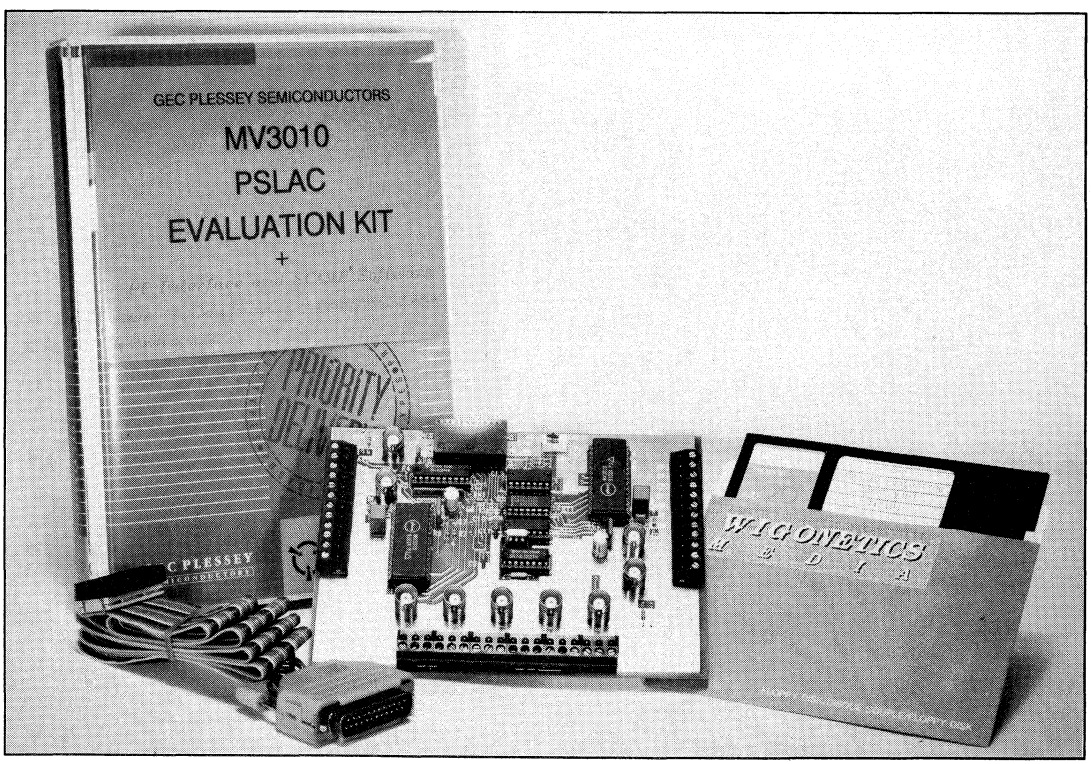
MV3010 SLAC EVALUATION PACKAGE

Now available from GPS is a complete evaluation package for the MV3010 Subscriber Line Audio Circuit (SLAC). The package includes both hardware and supporting software for use with IBM PCs or compatibles.

Hardware for the evaluation package consists of a circuit board containing two SLAC devices with full and flexible access to all analog and digital ports. The software (SCAMP) of the evaluation package can be used to fully control/monitor all programmable features of both SLACs. These features are discussed fully in Applications Note AN111 which is available separately. Lastly, the PCBAN111 evaluation package can be interfaced with the SLIC (Subscriber Line Interface Circuit) evaluation board, PCBAN114, to facilitate evaluation of a complete Line card circuit design.

FEATURES

- Full and Flexible Access to all Analog and Digital Ports of both SLACs of the Hardware.
- Hardware May Be Run as a Stand Alone Board or Interfaced to an IBM PC or Compatible.
- Full Software Control of the Evaluation Board via the SCAMP Software Running on the PC.
- Automated C Filter Preprogramming Software Routine Available within SCAMP.
- Automated Measurement and Display of Echo Return Loss Performance for the Chosen Line Interface Circuit.
- Easy To Use Menu Driven Software.
- Single Screen for each SLAC Status Readily Displayed by the SCAMP Software.
- Interfaces Directly to the PCBAN114 SLIC Evaluation Board.
- Application Note AN111 fully Describes the Operation and Uses of the Evaluation Package.



The PCBAN111 evaluation package.

DS3140-1.0

MV8870 / MV8870-1

INTEGRATED DTMF RECEIVER

The MV8870 / MV8870-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in GPS's double-poly ISO2-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code.

External component count is minimised by on-chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

The MV8870 and MV8870-1 are functionally identical, but differ in Electrical Characteristics.

FEATURES

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality

APPLICATIONS

- Receiver Systems for BT or CEPT Specifications
- Paging Sytems
- Repeater Systems / Mobile Radio
- Credit Card Systems
- Remote Control

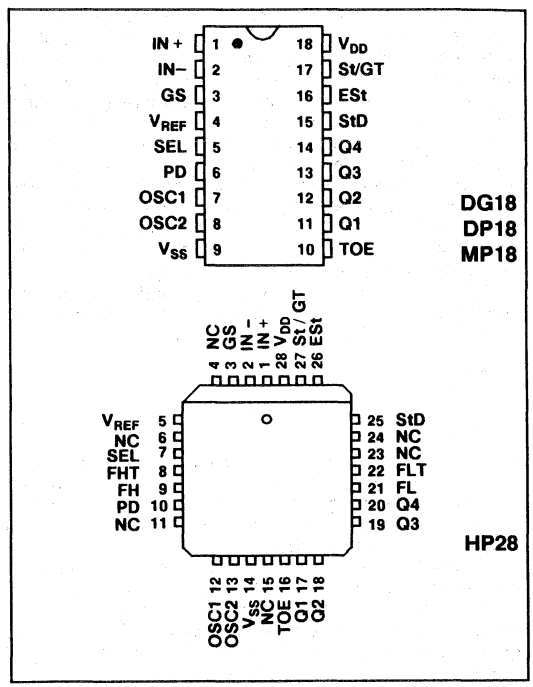


Fig.1 Pin connections - top view

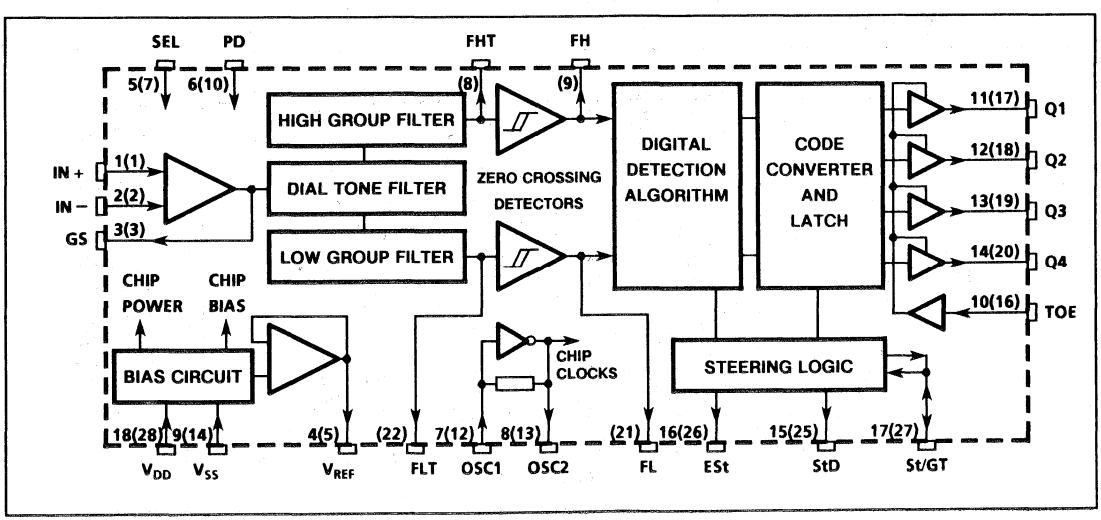


Fig. 2 Functional block diagram (Pin numbers in brackets refer to HP package)

FUNCTIONAL DESCRIPTION

The MV8870 / MV8870-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low tone groups, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor band-pass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Fig.3). Each filter is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

For testing and monitoring, the high and low group filter and zero crossing detector outputs are made available via FHT, FH, FLT and FL (HP package only).

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognises the simultaneous presence of two valid tones (this is referred to as the 'Signal Condition' in some industry specifications) the Early Steering output (ESt) will go to an active state. Any subsequent loss of signal condition will cause the ESt pin to go to its inactive state (see Fig.5).

Steering Circuit

Before registration of a decoded tone-pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes the voltage at the St/GT pin ($V_{St/GT}$) to rise as the capacitor discharges (see Figs.4 and 5).

Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), $V_{St/GT}$ reaches the threshold (V_{TSt}) of the steering logic which allows it to register the tone pair and strobe the corresponding 4-bit code into the output latch (see Fig.6). At this point the St/GT pin is activated as an output and drives $V_{St/GT}$ to V_{DD} (see Fig.5).

St/GT continues to drive high as long as ESt remains high. After a short delay (t_{DP}) to allow the output latch to settle, the delayed steering output pin (StD) goes high to indicate that the code for a new received tone-pair is available. The contents of the output latch are output onto the output bus (Q1 to Q4 pins) when the three-state output enable (TOE) pin is high.

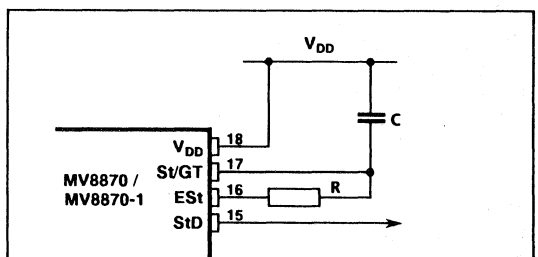


Fig. 4 Basic Steering Circuit

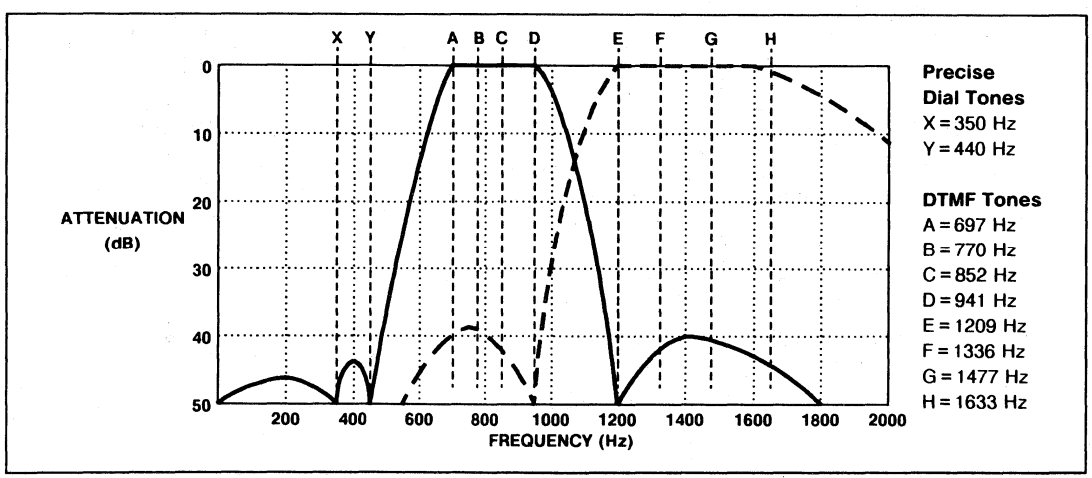


Fig. 3 Filter response

The steering circuit works in reverse to validate the interdigit pause between signals. Thus as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop-out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

APPLICATIONS

A simple application circuit is shown in Fig.7. This has a symmetric guard time circuit, a single-ended analog input and a dedicated crystal oscillator.

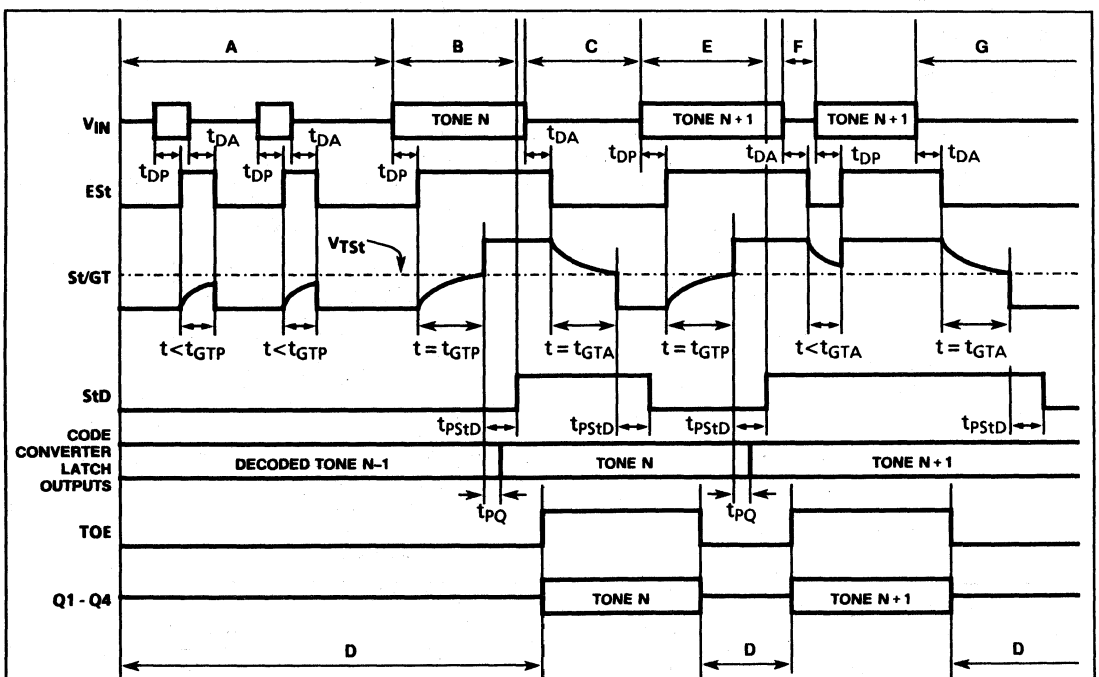
Guard Time Adjustment

In many situations not requiring seperate selection of tone duration and interdigit pause, the simple steering circuit shown in Fig.7 is applicable. Component values are chosen according to the formulae (see Figs. 4, 8a and 8b):-

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see Dynamic Characteristics and Fig.5) and t_{REC} is the minimum signal duration to be recognised by the receiver. Likewise t_{DA} is a device parameter (Fig.5) and t_{ID} is the minimum time taken to recognise an interdigit pause. A value for C2 of 0.1μF is recommended for most applications, leaving R3 to be selected by the designer.

Different steering arrangements may be used to select independantly the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal conditions long enough to be registered. Alternatively a relatively short t_{REC} with a long t_{ID} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figs. 8a and 8b.



EXPLANATION OF EVENTS

A. Tone bursts detected, but tone duration invalid and output latch unchanged.
B. Tone N detected, tone duration valid, output latch updated and new data signalled by StD.
C. End of tone N detected, tone absent duration valid, but output latch not updated until next valid tone.
D. Outputs switched to high impedance.
E. Tone N + 1 detected, tone duration valid, tone decoded, output latch updated (although outputs are currently high impedance) and new data signalled by StD.
F. Acceptable dropout of tone N + 1, tone absent duration invalid, StD and output latch unchanged.
G. End of tone N + 1 detected, tone absent duration valid, StD goes low but output latch not updated until next valid tone.

NOTES

1. t_{DP} time for valid tone present is a device parameter (see Electrical Characteristics).
2. t_{DA} time for valid tone absent is a device parameter (see Electrical Characteristics).
3. t_{GTP} and t_{GTA} are adjustable via external RC network at pins 16 and 17 (see Fig.4).
4. t_{PStD} and t_{PQ} are propagation delays given in the Electrical Characteristics.

Fig. 5 Timing Diagram.

f_{LOW}	f_{HIGH}	DIGIT	TOE	SELECT = L				SELECT = H			
				Q4	Q3	Q2	Q1	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1	0	0	0	1
697	1336	2	H	0	0	1	0	0	0	1	0
697	1477	3	H	0	0	1	1	0	0	1	1
770	1209	4	H	0	1	0	0	0	1	0	0
770	1336	5	H	0	1	0	1	0	1	0	1
770	1477	6	H	0	1	1	0	0	1	1	0
852	1209	7	H	0	1	1	1	0	1	1	1
852	1336	8	H	1	0	0	0	1	0	0	0
852	1477	9	H	1	0	0	1	1	0	0	1
941	1209	0	H	1	0	1	0	0	0	0	0
941	1336	*	H	1	0	1	1	1	0	1	0
941	1477	#	H	1	1	0	0	1	0	1	1
697	1633	A	H	1	1	0	1	1	1	0	0
770	1633	B	H	1	1	1	0	1	1	0	1
852	1633	C	H	1	1	1	1	1	1	1	0
941	1633	D	H	0	0	0	0	1	1	1	1
-	-	Any	L	Z	Z	Z	Z	Z	Z	Z	Z

Fig. 6 Functional decode table

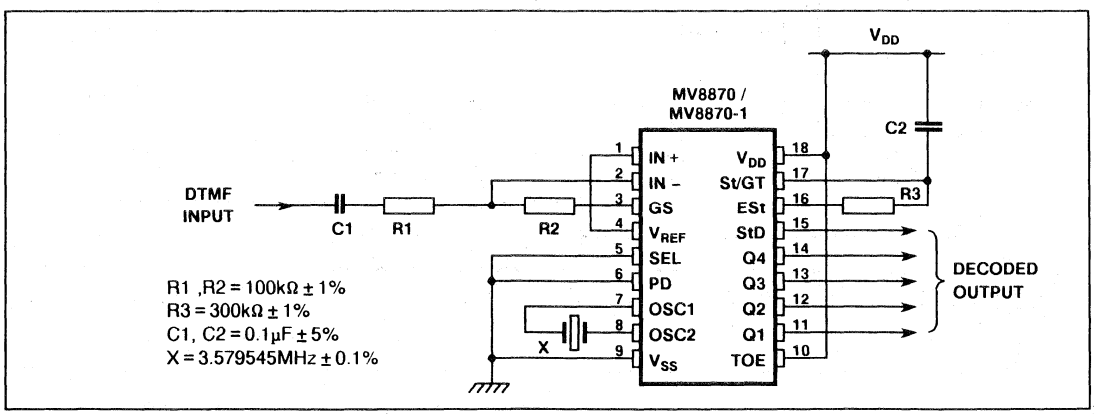


Fig. 7 Simple application circuit; single ended input.

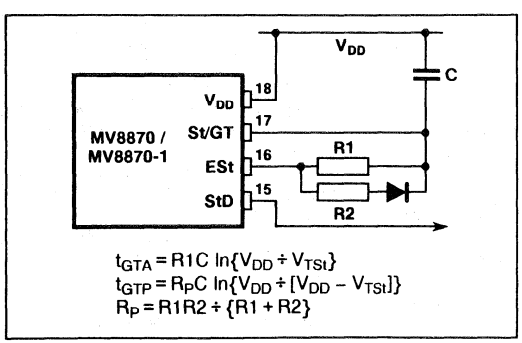


Fig. 8a Guard time adjustment ($t_{GTP} < t_{GTA}$)

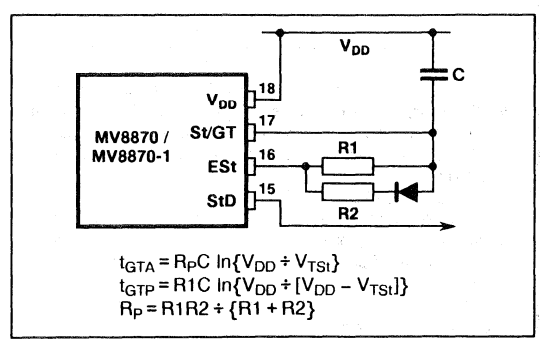


Fig. 8b Guard time adjustment ($t_{GTP} > t_{GTA}$)

Differential Input Configuration

The input arrangement of the MV8870 / MV8870-1 provides a differential input op. amp. and a bias source (V_{REF}) to bias the inputs at mid-rail. The gain may be adjusted through a feedback resistor from the op. amp. output (GS). In a single-ended configuration the input pins are connected as shown in Fig. 7 where the op. amp. is connected to give unity gain and the V_{REF} pin biases the input at (V_{DD} ÷ 2).

Fig.9 shows the differential configuration. In this circuit gain is adjusted through the feedback resistor R5.

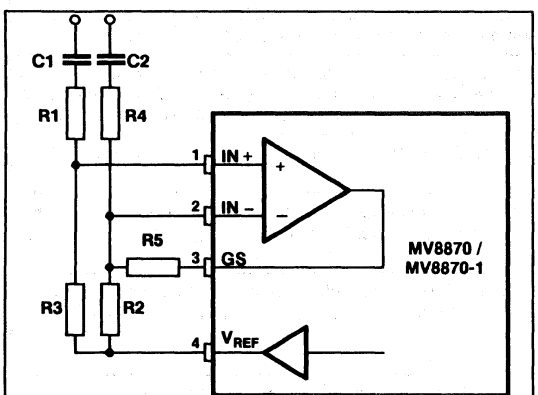
Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.58MHz crystal which is normally connected as shown in Fig. 7. However it is possible to configure several MV8870 / MV8870-1 devices to use only a single oscillator crystal.

The devices are chained together with the oscillator output of the first device in the chain capacitively coupled to the oscillator input of the second device and so on down the chain. The details are shown in Fig.10. Precision balancing capacitors are not required as problems of unbalanced loading are not a concern.

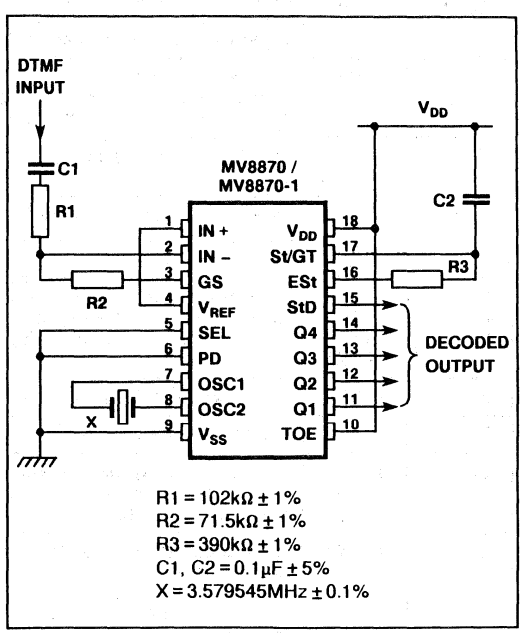
Receiver System For BT Specification POR 1151

The circuit shown in Fig.11 illustrates the use of the MV8870-1 in a typical receiver system. The BT specification defines the non-operate level as input signals below –34 dBm. This is obtained by choosing R1 and R2 to give 3dB of attenuation so that an input of –34 dBm corresponds to –37 dBm at the op. amp. output pin (GS). The tolerances on R3 and C2 give a tolerance on guard time of 6%. For better performance the non-symmetric guard time circuit shown in Fig.12 is recommended.



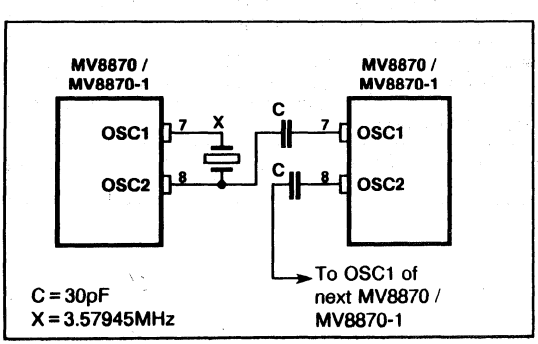
Differential Input Amplifier
C1 = C2 = 0.01µF
R1 = R4 = R5 = 100kΩ Resistors are ± 1%
R2 = 60kΩ Capacitors are ± 5%
R3 = R2R5 ÷ (R2 + R5)
Voltage Gain ($A_V$diff) = R5 ÷ R1
Input Impedance
$Z_{INDIFF} = 2[R1^2 + (1 \div \omega C)^2]^{1/2}$

Fig. 9 Differential input configuration.



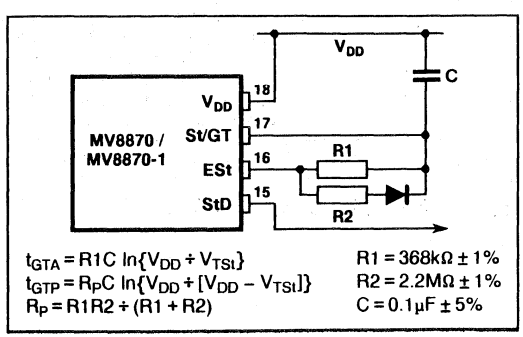
R1 = 102kΩ ± 1%
R2 = 71.5kΩ ± 1%
R3 = 390kΩ ± 1%
C1, C2 = 0.1µF ± 5%
X = 3.579545MHz ± 0.1%

Fig. 11 Single ended circuit for BT/CEPT Specs.



C = 30pF
X = 3.57945MHz

Fig. 10 Oscillator circuit



$t_{GTA} = R1C \ln\{V_{DD} \div V_{TSt}\}$
$t_{GTP} = R_PC \ln\{V_{DD} \div [V_{DD} - V_{TSt}]\}$
$R_P = R1R2 \div (R1 + R2)$

R1 = 368kΩ ± 1%
R2 = 2.2MΩ ± 1%
C = 0.1µF ± 5%

Fig. 12 Non-symmetric guard time circuit.

PIN DESCRIPTIONS (Note 1)

Symbol	Pin no.	Pin name and description
IN+, IN–	1 (1) 2 (2)	**In Pius and Minus (Voltage Inputs).** These are respectively the non-inverting and inverting inputs to the front-end op-amp. The DTMF input is applied to these pins in normal operation.
GS	3 (3)	**Gain Select (Voltage Output).** This pin is connected to the output of the front-end op-amp. A feedback resistor between this pin and the inverting input (IN –) controls the front-end gain.
V_{REF}	4 (5)	**Reference Voltage (Voltage Output).** This pin outputs a voltage which is half-way between the power supply voltages (V_{SS} and V_{DD}). It can be used to bias the input signal.
SEL	5 (7)	**Select Input.** This pin determines the Q4..Q1 truth table as shown in Fig. 6
PD	6 (10)	**Power Down Input.** This pin is used to power down and inhibit the oscillator. It is active high and includes an internal pull-up resistor.
FHT	- (8)	**Filter High Tones.** Sine wave output from the high group filter circuit.
FH	- (9)	**High Frequency Output.** Square wave output from the high group zero crossing detector.
OSC1	7 (12)	**Oscillator 1 (Digital Input).** This is the input to the inverter of the oscillator circuit. There is an internal biasing resistor between this pin and the inverter output (OSC2). A 3.579545MHz crystal is normally connected externally between the two pins to complete the oscillator circuit.
OSC2	8 (13)	**Oscillator 2 (Digital Output).** This is the output of the inverter of the oscillator circuit. There is an internal biasing resistor between this pin and the inverter input (OSC1). A 3.579545MHz crystal is normally connected externally between the two pins to complete the oscillator circuit.
V_{SS}	9 (14)	**Negative Supply (Power Input).** This is the negative power supply for the device. It is normally 0V.
TOE	10 (16)	**Three-State Output Enable (Digital Input with Pull-up).** If this pin is high then the decoder outputs (Q1 to Q4) are enabled. If it is low then the outputs go into their high-impedance state. There is an internal pull-up at this pin.
Q1 Q2 Q3 Q4	11 (17) 12 (18) 13 (19) 14 (20)	**Q1 to Q4 (Three-State Outputs).** When the TOE pin is high these pins output the code in the output latch which corresponds to the last valid tone-pair detected. They go into their high-impedance state when the TOE pin is low.
FL	- (21)	**Low Frequency Output.** Square wave output from the low group zero crossing detector.
FLT	- (22)	**Filter Low Tones.** Sine wave output from the low group filter circuit.
StD	15 (25)	**Delayed Steering (Digital Output).** This pin follows the ESt and St/GT pins. It goes high to indicate that a new tone-pair has been detected and the corresponding code has been loaded into the output latch. It goes low to indicate that a new tone-pair is expected.
ESt	16 (26)	**Early Steering (Digital Output).** This pin goes high when the digital detection algorithm decides that there is a valid DTMF input. It goes low as soon as the algorithm decides that there is no valid DTMF input. In normal use this pin is used to drive an external guard time circuit which in turn drives the St/GT pin.
St/GT	17 (27)	**Steering / Guard Time (Voltage Input / Digital Output).** This pin follows the ESt pin. When ESt pin changes state this pin acts as an input and monitors the voltage developed here by the ESt pin acting through the external guard time circuit. When the voltage reaches the internally generated V_{TSt} level then this pin acts as an output and pulls itself fully to the state of the ESt pin. When this pin goes fully high a new code is loaded into the output latch and the StD pin goes high. When this pin goes fully low the device prepares itself for a new tone-pair and the StD pin goes low.
V_{DD}	18 (28)	**Positive Supply (Power Input).** This is the positive power supply for the device. It is normally 5V.

Note: 1. Figures in brackets are for HP28 package.

RECOMMENDED OPERATING RANGE

Characteristic	Symbol	Value (MV8870)			Value (MV8870-1)			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
Positive supply voltage	V_{DD}	4.75	5.0	5.25	4.75	5.0	5.25	V	
Operating temperature	T_{OP}	–40	+25	+80	–40	+25	+80	°C	

ELECTRICAL CHARACTERISTICS Over Recommended Operating Range (unless otherwise specified)

Test conditions (unless otherwise stated):

Voltages measured with respect to ground (V_{SS}).

Typical figures are for design aid only; they are not guaranteed and are not subject to production testing.

Static Characteristics

Characteristic	Symbol	Value (MV8870)			Value (MV8870-1)			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
Power dissipation	P_D		15	35		15	37	mW	$f_0 = 3.579545$MHz
V_{DD} supply current	I_{DD}		3.0	7.0		3.0	7.0	mA	
Input high voltage (OSC1 & TOE)	V_{IH}	3.5		V_{DD}	3.5		V_{DD}	V	
Input low voltage (OSC1 and TOE)	V_{IL}	0		1.5	0		1.5	V	
Input leakage current (OSC1, IN+ and IN–)	I_I		100			100		nA	$0 \le V_{PIN} \le V_{DD}$
Internal pull-up current (TOE)	I_{PU}		7.5	15.0		7.5	15.0	µA	$0 \le V_{PIN} \le V_{DD}$
Steering threshold voltage (St/GT)	V_{TSt}	2.2	2.35	2.5	2.2	2.35	2.5	V	
Low level output voltage	V_{OL}		0.03			0.03		V	No Load
High level output voltage	V_{OH}		4.97			4.97		V	No Load
Output low sink current (OSC2, Q1-Q4, StD and ESt)	I_{OL}	1.0	2.5		1.0	2.5		mA	$V_{PIN} = 0.4$V
Output high source current (OSC2, Q1-Q4, StD and ESt)	I_{OH}	0.4	0.8		0.4	0.8		mA	$V_{PIN} = 4.6$V
Reference voltage	V_{REF}	2.4		2.7	2.4		2.8	V	No Load
V_{REF} output resistance	R_{REF}		10.0			10.0		kΩ	
Pin capacitance	C_P		7.0	15.0		7.0	15.0	pF	Pin to supplies

Dynamic Characteristics : Input Op Amp

Characteristic	Symbol	Value (MV8870)			Value (MV8870-1)			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
Input impedance (IN + and IN–)	R_{IN}		10			10		MΩ	1kHz
Input offset voltage (IN + and IN–)	V_{OS}		25			25		mV	
Input leakage current	I_{IN}		100			100		nA	$V_{SS} < V_{IN} < V_{DD}$
Power supply rejection	PSRR		60			60		dB	1kHz
Common mode range	V_{CM}		3.0			3.0		V	No Load
Common mode rejection	CMRR		60			60		dB	$V_{IN} = V_{REF} \pm 1.3V$
DC open loop voltage gain	A_{VOL}		65			65		dB	
Open loop unity gain bandwidth	f_C		1.5			1.5		MHz	
Output voltage swing (GS)	V_O		4.5			4.5		V_{p-p}	R_{OUT} to $V_{SS} \geq 100k\Omega$
Output capacitive load (GS)	C_{OUT}			100			100	pF	
Output resistive load (GS)	R_{OUT}	50			50			kΩ	

Dynamic Characteristics : Oscillator Circuit

Characteristic	Symbol	Value (MV8870 and MV8870-1)			Units	Conditions
		Min	Typ	Max		
Crystal/clock frequency (OSC1 and OSC2)	f_O	3.579	3.579545	3.5831	MHz	
Oscillator input rise time (OSC1) - external clock	t_{OR}			110	ns	See Fig. 13
Oscillator input high time (OSC1) - external clock	t_{OH}	110		170	ns	See Fig. 13
Oscillator input fall time (OSC1) - external clock	t_{OF}			110	ns	See Fig. 13
Oscillator Input Low Time (OSC1 Pin) - external clock	t_{OL}	110		170	ns	See Fig. 13
Oscillator Output Load (OSC2)	C_{LO}			30	pF	

Dynamic Characteristics : Detector

Characteristic	Symbol	Value (MV8870)			Value (MV8870-1)			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
Valid input level (GS)	V_{VL} P_{VL}	77.7 –29		2458 1.0	61.7 –31		2458 1.0	mV_{p-p} dBm	1, 2, 3, 5, 6, 9
Invalid input level (GS)	V_{IL} P_{IL}						30.8 –37	mV_{p-p} dBm	1, 2, 3, 5, 6, 9
Acceptable positive twist	T_{AP}		10		6.0	10		dB	2, 3, 6, 9
Acceptable negative twist	T_{AN}		10		6.0	10		dB	2, 3, 6, 9
Frequency deviation accept	Δ_{FA}	–1.5 –2.0		+1.5 +2.0	–1.5 –2.0		+1.5 +2.0	% Hz	2, 3, 5, 9
Frequency deviation rejected as too low	Δ_{FRL}		–5.0	–3.5		–5.0	–3.5	%	2, 3, 5, 9
Frequency deviation rejected as too high	Δ_{FRH}	3.5	5.0		3.5	5.0		%	2, 3, 5, 9
Third tone tolerance	P_{TTT}	–16				–18		dB	2, 3, 4, 5, 9, 12
Noise tolerance	P_{NT}		–12			–12		dB	2, 3, 4, 5, 7, 9, 10
Dial tone tolerance	P_{DTT}		+22			+22		dB	2, 3, 4, 5, 8, 9, 11
Tone present detect time	t_{DP}	5	11	14	5	11	14	ms	
Tone absent detect time	t_{DA}	0.5	4.0	8.5	0.5	4.0	8.5	ms	

NOTES
1. dBm = decibels above or below a reference power of 1mW into a 600Ω load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration = 40ms, tone pause = 40ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have equal amplitudes.
6. Tone pair is deviated by ±(1.5% + 2Hz).
7. Bandwidth limited (3kHz) Gaussian noise.
8. The precise dial tone frequencies are (350Hz and 440Hz) ±2%.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest frequency component in DTMF signal.
11. Referenced to the minimum valid input level.
12. Refer to Fig. 11. Input DTMF Tone Level at – 25dBm (– 28dBm at GS pin). Interference Frequency Range is 480 to 3400Hz.

Dynamic Characteristics : Decoder

Characteristic	Symbol	Value (MV8870/MV8870-1)			Units	Conditions
		Min	Typ	Max		
Propagation delay (St/GT to Q)	t_{PQ}		8	11	µs	TOE high. See Fig. 14
Propagation delay (St/GT to StD)	t_{PStD}		12		µs	See Fig. 14
Output data set-up time (Q to StD)	t_{QStD}		3.4		µs	TOE high. See Fig. 14
Enable propagation delay (TOE to Q)	t_{PTE}		50	60	ns	R_L = 10kΩ(pulldown) C_L = 50pF. See Fig. 15
Disable propagation delay (TOE to Q)	t_{PTD}		300		ns	R_L = 10kΩ(pulldown) C_L = 50pF. See Fig. 15

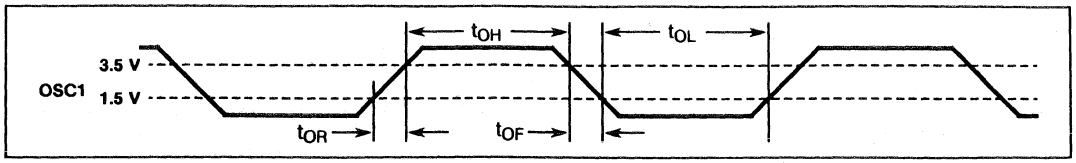


Fig. 13 Timing - external oscillator input.

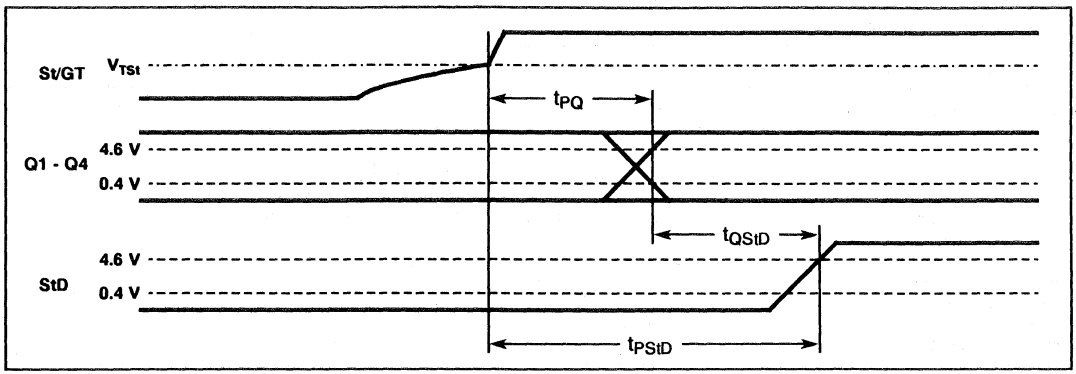


Fig. 14 Timing - decoded data.

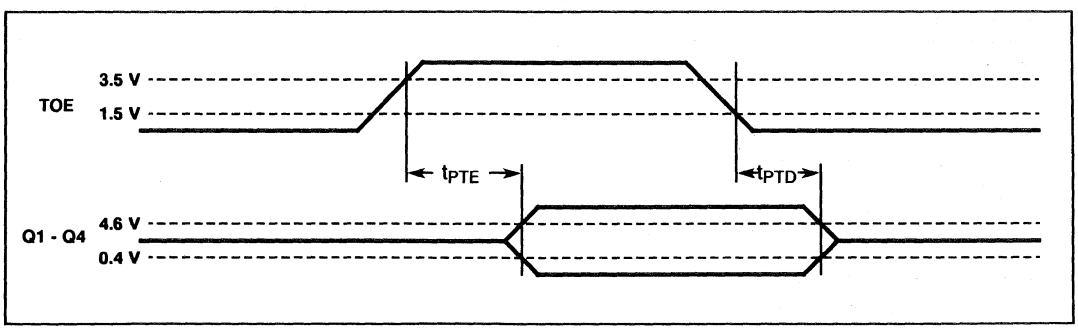


Fig. 15 Timing - Output enable and disable .

ABSOLUTE MAXIMUM RATINGS* Voltages are with respect to the negative power supply (V_{SS})

Parameter	Symbol	Value (MV8870)		Value (MV8870-1)		Units
		Min	Max	Min	Max	
Positive supply voltage (Pin 18)	V_{DD}		+6.0		+6.0	V
Voltage on any pin (other than supplies)	V_{MAX}	–0.3	V_{DD} + 0.3	–0.3	V_{DD} + 0.3	V
Current at any pin (other than supplies)	I_{MAX}		10		10	mA
Storage temperature	T_{STG}	–65	+150	–65	+150	°C
Package power dissipation	P_P		1000†		1000†	mW

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
†Derate parameter above +75°C at 16mW/°C, all leads soldered to board.

Section 4
Cryptographics

DS3114-1.3

DVS200

SPEECH/DATA ENCRYPTION PROCESSOR

The DVS200 is a digital encryption processor, with on-chip A-D and D-A converters for speech bandwidth signals, that implements a TDM (Time Division Multiplexing) encryption algorithm. The device can be used to protect virtually any vulnerable analog speech or digital data communication channel. The high security is provided by a complex on-chip key generator, and an algorithm that checks the 'randomness' of the encrypted output.

For basic speech encryption applications, the DVS200 requires the addition of only a DRAM, SRAM and a few other external components.

The device uses correlation for sync tone decoding, which gives high synchronisation performance even on relatively noisy channels.

An on-chip notch filter eliminates sync tones from the speech channel, thus enabling frequent synchronisation without significant loss of speech.

The DVS200 has a range of user selectable options: clear voice override, periodic sync, 8/16 segments per frame, message key, and sync delay.

The chip uses multiple methods of code entry: switches, keyfill gun or PROM dump and supports battery backup, enabling it to be powered down when not in use.

FEATURES

- Complete Encryption System on a chip
- Excellent Speech Quality due to On-chip High Performance A to D and D to A Converters
- Low Power CMOS Fabrication - typically 25mW
- Multiple Methods of Code Entry
- Supports Battery Backup
- High Synchronisation Performance
- On-chip Notch Filter for Eliminating Sync Tones from the Speech Channel
- A Range of User-Selectable Options
- Data Encryption Rate up to 4.8kbits/s

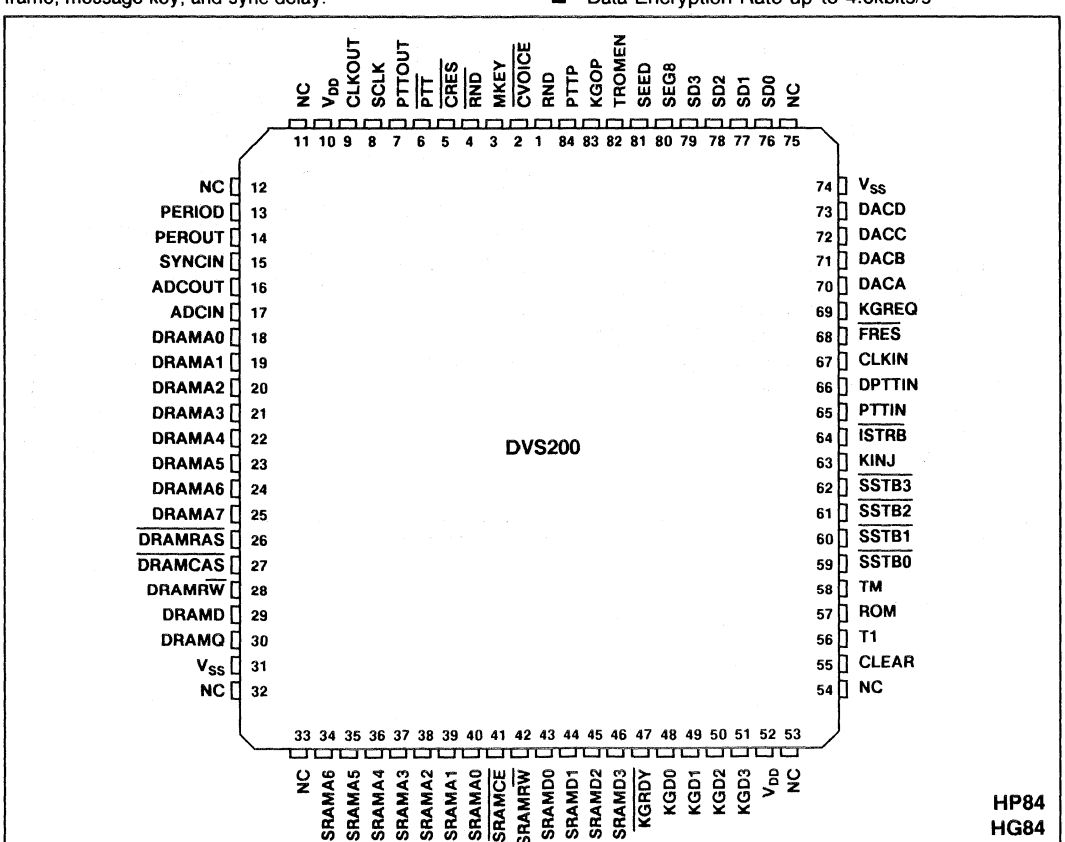


Fig. 1 Pin connections - top view

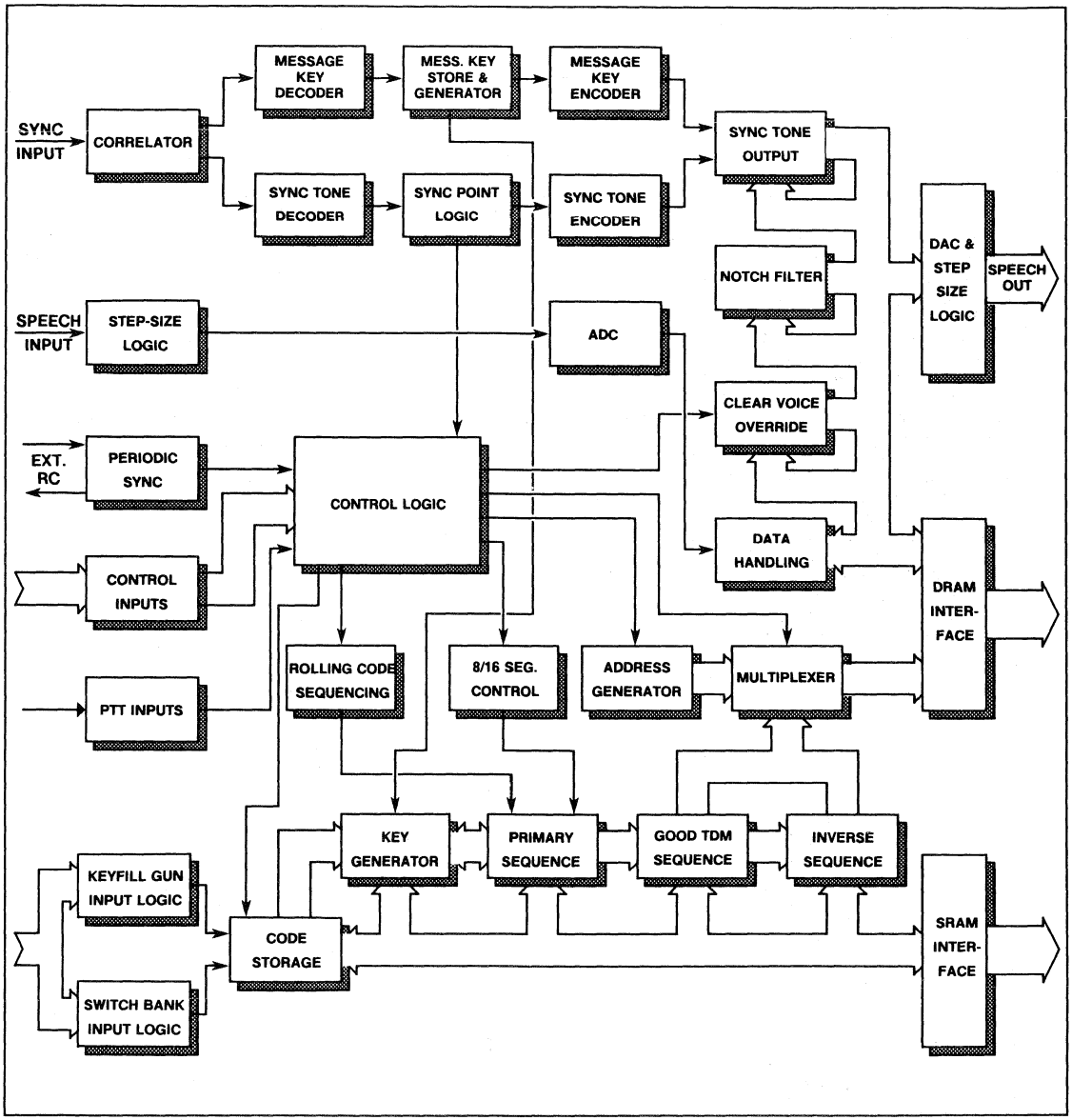


Fig. 2 DVS200 block diagram

PIN DESCRIPTIONS

Pin	Name	Type	Description
1	RND	I	Input for the source of the message key data.
2	$\overline{\text{CVOICE}}$	IP	Active low clear voice override pin. When a logic '0' is applied the device outputs unencrypted speech. When a logic '1' is applied, the device is in secure mode.
3	MKEY	IP	Used for selecting the message key option. A logic '1' enables the device.
4	$\overline{\text{RND}}$	O	This is a latched, inverted version of RND (pin 1). It can be used, together with pin 1, to provide a random data stream for the message key.
5	$\overline{\text{CRES}}$	O	Test pin - Pulses low when the device synchronises.
6	$\overline{\text{PTT}}$	O	Inverted version of PTTOUT (pin 7).
7	PTTOUT	O	This pin, when active, indicates that the device is in transmit mode. It can therefore be used to control the Tx/Rx mode of the equipment that the device is installed in.
8	SCLK	O	Buffered version of CLKOUT (pin 9). Can be used to set the clock oscillator frequency.
9	CLKOUT	O	With CLKIN (pin 67), connection for clock oscillator crystal.
10	V_{DD}	I	+5V
13	PERIOD	SI	Connections for external RC timing components for the periodic sync oscillator.
14	PEROUT	O	
15	SYNCIN	SI	Received sync tone input.
16	ADCOUT	O	The analog to digital converter is formed around these two pins
17	ADCIN	I	
18	DRAMA0	O	DRAM Address bus.
19	DRAMA1	O	
20	DRAMA2	O	
21	DRAMA3	O	
22	DRAMA4	O	
23	DRAMA5	O	
24	DRAMA6	O	
25	DRAMA7	O	
26	$\overline{\text{DRAMRAS}}$	O	DRAM Control bus.
27	$\overline{\text{DRAMCAS}}$	O	
28	DRAM$\overline{\text{RW}}$	O	
29	DRAMD	O	Connect to DRAM data input.
30	DRAMQ	I	Connect to DRAM data output.
31	V_{SS}	I	0V
34	SRAMA6	O	SRAM Address bus
35	SRAMA5	O	
36	SRAMA4	O	
37	SRAMA3	O	
38	SRAMA2	O	
39	SRAMA1	O	
40	SRAMA0	O	
41	$\overline{\text{SRAMCE}}$	O	SRAM Control bus.
42	SRAM$\overline{\text{RW}}$	O	
43	SRAMDO	BP	SRAM Data bus.
44	SRAMD1	BP	
45	SRAMD2	BP	
46	SRAMD3	BP	
47	$\overline{\text{KGRDY}}$	O	This is relevant whenever the device is used for encrypting data. It strobes low when a valid word is present on the key generator output port.

NOTES
1. Key to pin type: I = Input, IP = Input with pullup, SI = Schmitt input, O = Output, TO = Tri-state output, BP = Bidirectional output with pullup
2. Tie all unused inputs to either V_{DD} or V_{SS}.
3. Pins 11, 12, 32 and 33 are NC (No Connection).

Table 1 Pin descriptions

PIN DESCRIPTIONS (continued)

Pin	Name	Type	Description
48 49 50 51	KGD0 KGD1 KGD2 KGD3	O O O O	Key generator output port
52	V_{DD}	I	+5V
55	CLEAR	O	Indicates whether the device is operating in clear or secure mode. Logic '1' clear mode, logic '0' secure mode.
56 57 58	T1 ROM TM	O O IP	Test pins.
59 60 61 62	$\overline{SSTB0}$ $\overline{SSTB1}$ $\overline{SSTB2}$ $\overline{SSTB3}$	TO TO TO TO	These pins strobe low, in sequence, when the device is being seeded. They are only used when a bank of switches is used to provide the seed data.
63	KINJ	I	Used to select which mode of seed entry is to be used. A logic '0' selects switch entry (automatic), a logic '1' selects keyfill gun/PROM dump entry (external strobe).
64	$\overline{ISTRB}$	SI	Strobe pin (active low) for keyfill gun/PROM entry of seed data.
65	PTTIN	SI	Used to select the transmit mode of the device. The polarity of the active level (i.e. 0 or 1) is determined by PTTP (pin 84).
66	DPTTIN	SI	Used to provide an additional delay between start of transmission and sync tone transmission. Thus allowing for delays in the channel opening; due to squelch circuitry etc.
67	CLKIN	I	With CLKOUT (pin 9), connection for clock oscillator crystal.
68	$\overline{FRES}$	SI	Device reset (active low).
69	KGREQ	I	When in data encryption mode, this pin is strobed (active high) to request a key generator word.
70 71 72 73	DACA DACB DACC DACD	O O O O	Digital to analog converter outputs.
74	V_{SS}	I	0V
76 77 78 79	SDO SD1 SD2 SD3	IP IP IP IP	Seed data input port.
80	SEG8	IP	Option pin for selecting number of segments per frame. Logic '0' sixteen segments, logic '1' eight segments.
81	SEED	IP	Normally the device loads new seed data each time it is reset. Taking this pin low inhibits this function. This enables seed data already present in the SRAM, due to battery back-up for example, to be retained. The device can therefore be powered down without loss of seed data.
82	TROMEN	IP	Test pin.
83	KGOP	IP	Selects which mode of encryption the device is required to operate in. A logic '0' selects data encryption, a logic '1' selects speech encryption.
84	PTTP	IP	Used for selecting which polarity PTTIN and PTTOUT are active. A logic '0' selects active high, a logic '1' selects active low.

NOTES
1. Key to pin type: I = Input, IP = Input with pullup, SI = Schmitt input, O = Output, TO = Tri-state output, BP = Bidirectional output with pullup
2. Tie all unused inputs to either V_{DD} or V_{SS}.
3. Pins 53, 54 and 75 are NC (No Connection).

Table 1 Pin descriptions (continued)

Pin	Name	Logic '0'	Logic '1'
2	$\overline{\text{CVOICE}}$	Clear Speech mode.	Encrypted Speech mode.
3	MKEY	Message key disabled.	Message key enabled.
63	KINJ	Automatic seed data entry (switches).	Strobe controlled seed data entry using keyfill gun/PROM dump).
80	SEG8	Sixteen segments per frame.	Eight segments per frame.
81	SEED	Disable seed data loading on reset.	Enable seed data loading on reset.
83	KGOP	Data encryption mode.	Speech encryption mode.
84	PTTP	PTT active high.	PTT active low.

NOTE
All of the above pins except KINJ (pin 63) have internal pullups. So, if a logic 1 is desired, the pin should simply be left unconnected.

Table 2: Summary of Options

OVERVIEW OF OPERATION

ENCRYPTION TECHNIQUE

The DVS200 is an integrated circuit that encrypts speech using a TDM (Time Division Multiplexing) encryption technique. This process involves dividing speech, in the time domain, into sections; these sections are known as frames. The frames are then sub-divided into smaller sections or segments. The device then reverses and re-arranges (transposes) the segments of speech within each of the frames. Once this has been done, the encrypted speech is output from the DVS200. Fig. 3 demonstrates the effect that the DVS200 would have on a signal that had a ramped envelope.

Two things will be noticed from Fig. 3: first, that the signal is delayed by an equivalent of one frame, i.e. 236ms (this figure is valid for the nominal device clock frequency of 4.433619MHz). This means that there will be a system delay of 472ms (236ms for encrypt and 236ms for decrypt).

The second thing to notice, is that, in Fig. 3, there are eight segments per frame. The DVS200 has the option of increasing this to sixteen segments per frame; this is achieved by simply tying an external pin (pin 80-SEG8) to ground.

The sixteen segments per frame option offers greater security (due to the increased number of permutations available), but its use may reduce the recovered speech quality. The speech is recovered, i.e. decrypted, simply by reversing the process performed at the encryption stage.

KEY GENERATOR

The way in which the segments are transposed within the frame is determined by two functions in the DVS200. The first is the on-chip key generator. The key generator is a sub-system that outputs a set of numbers in a pseudo-random sequence. The position of each segment is determined by the output of the key generator. The key generator is complex and offers a high degree of unpredictability.

This means that it will be difficult to extract the original speech from the encrypted signal. What sequence the key generator uses, and from what point in the sequence the key generator starts, is determined by the seed data (code) that has been entered by the user. This code can be any one of approximately $3x10^{38}$ permutations (depending on the method of entry) and must be entered in both the encrypting and decrypting DVS200s for the original speech signal to be recovered correctly.

The other function that determines the transposition of the segments is the 'Good TDM Algorithm'. This algorithm ensures that the segments have been transposed in a non-linear fashion. For example, the sequence A5,A6,A7,A8,A1,A2,A3,A4 would not be suitable for encryption purposes, whereas the sequence shown in Fig. 3 (A5,A8,A2,A4,A6,A1,A7,A3) is eminently suitable.

SYNCHRONISATION - NO MESSAGE KEY

In order for the receive DVS200 (Rx) to correctly decrypt the incoming encrypted speech, it must be synchronised to the transmit DVS200 (Tx) in two ways. First, the frame and segment boundaries of the two devices must be aligned in time; secondly, the two key generators must be at the same point in the same sequence for each corresponding segment.

Both of these phases of synchronisation are achieved with a sync tone. This is a 128 period tone at a frequency of 1.082kHz (with a clock frequency of 4.433619MHz) that is transmitted across the transmission channel by the Tx DVS200. When the Rx DVS200 receives the sync tone it is recognised (using a form of correlation) and a sync point is extracted.

At this point the frames are aligned and the key generator is loaded with the code previously entered by the user. The two devices then have an equal time reference from which to start operation (this reference point is shown in Fig. 6a).

A sync tone is transmitted each time a transmission is initiated. Sync tones can also be transmitted at regular intervals (periodic sync); the period between each sync tone transmission is determined by the user. Note that in Fig. 6a, the DAC output is shown with only sync tones present. Normally encrypted speech is also present, but this has been omitted for clarity.

SYNCHRONISATION - MESSAGE KEY

The message key facility is an option, selected by MKEY (pin 3), that significantly increases the operational security of the DVS200. The main function of the message key is connected with synchronisation. Normally, as mentioned above, the key generator is set to a particular point (determined by the user code) each time the devices synchronise. The net result of this is that the DVS200 repeats a sequence of segment transpositions each time a sync tone is received.

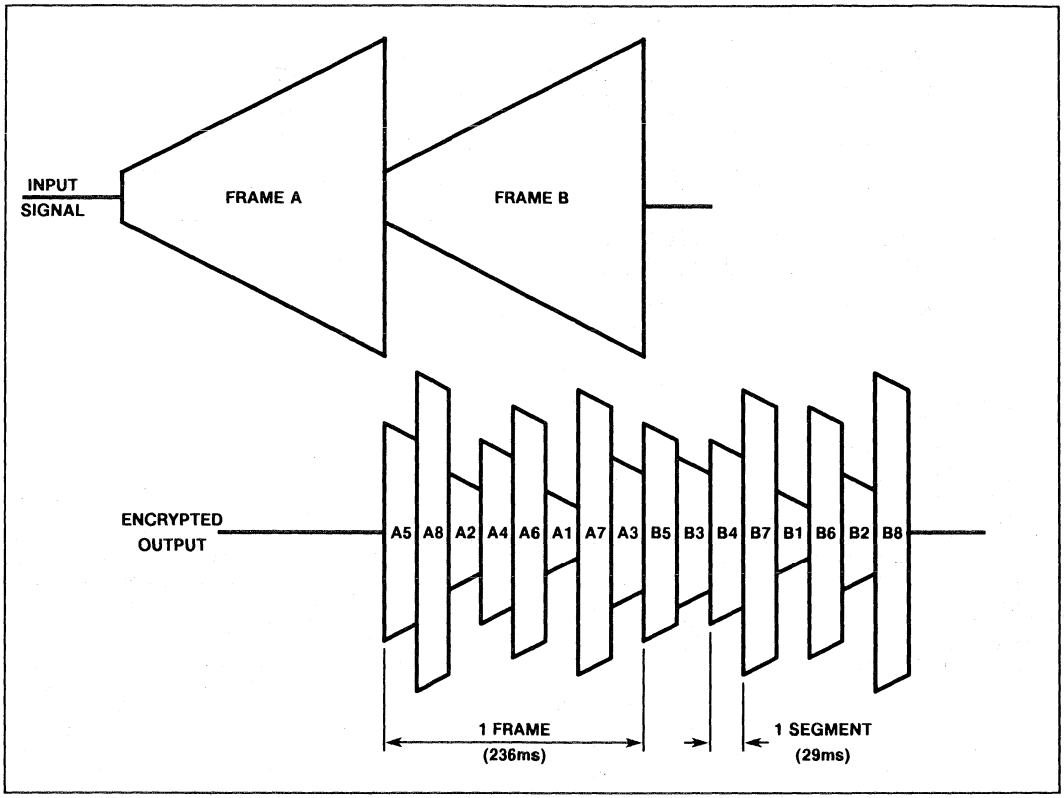


Fig. 3 Segmentation

When the message key option is selected, the key generator is set to a different point each time the device synchronises. The point to which the key generator is set is determined by the user code and a new set of data. This new data is the message key.

The message key data is derived by the Tx DVS200 and then transmitted to the Rx DVS200 (using phase modulation) each time a sync tone is transmitted (for derivation of message key data see page 4-10). The fact that the key generator is reset to a different point each time devices synchronise means that the period between the transmission of sync tones can be very short (as little as a second) without diminishing the security of the DVS200, thus allowing the late-entry-into-net facility that many communication systems require.

There are 32 bits of data exchanged between the two devices each time they synchronise. Each bit is represented by 32 periods of a 1.082kHz tone (the same frequency as the sync tone). It would therefore take approximately one second to complete the synchronisation process. To avoid this excessive delay, and to initialise the message key exchange, a message key precursor is transmitted before the message key itself (see Fig. 6b). This precursor is of the same length and frequency as that of the sync tone discussed on page 4-7.

The DVS200 temporarily synchronises to the precursor, loading only user code into the key generator. So, between the precursor sync point and the final sync point the DVS200 is operating with the user code exclusively (as in non-message key mode). It is only once all of the message key has been received that it can be utilised by the encryption facilities.

As mentioned above, the data is encoded using phase modulation. Each set of 32 periods (one data bit) is either in phase or anti-phase with the precursor; if it is in phase it represents a logic '0', anti-phase a logic '1'. The first bit, D1 in Fig. 6b, is always a logic '1'; i.e. in anti-phase to the precursor. The DVS200 detects this phase change and switches over to message key decode mode.

The example shown in Fig. 6b has the second data bit (D2) as a logic '0', and it can be seen that at the junction of D1 and D2 the tone reverts to being in phase with the message key precursor.

The final sync point always occurs at the final edge of the message key tone. In the case of Fig. 6b, the last bit, D32 is a logic '0' (in-phase), so the final edge is negative-going. If D32 were a logic '1', the final edge would be positive-going.

CLEAR VOICE OVERRIDE

The DVS200 outputs unprocessed speech when either one of two things happen. The first possibility is that clear speech mode is selected manually by the user. This is done by applying a logic '0' to the $\overline{\text{CVOICE}}$ input (pin 2).

The second possibility is that the DVS200 has automatically invoked the clear speech mode because the encryption facility is not being used.

This facility allows a piece of equipment incorporating the DVS200 to be used on channels that are not exclusively encrypted, without the user manually switching the equipment between clear and secure mode.

There are three different events that can trigger the automatic switch to clear mode. They are as follows:

(a) Device Reset - Each time the device is reset, the DVS200 switches to clear speech mode.

(b) Post PTT - At the point that PTTOUT (pin 7) goes inactive (i.e. the transmission has been completed) the DVS200 switches to clear speech mode.

(c) Non-receipt of Sync Tone - If, when using periodic sync, a sync tone has not been received within twice the normal interval between sync tones, the DVS200 switches to clear speech mode.

When the DVS200 has been switched to clear speech mode by one of the above events (a, b or c) it remains in that state until it either receives a sync from another DVS200, or the transmit mode is selected (i.e. PTT goes active). It then switches back to secure speech mode.

From the above, it will be noticed that the speech is always transmitted encrypted unless $\overline{\text{CVOICE}}$ is active (logic '0'). A logic '1' on the CLEAR output (pin 55) indicates that the DVS200 is in clear speech mode.

APPLICATION NOTES

DRAM AND SRAM SPECIFICATIONS

For basic operation the DVS200 needs two external ICs: a dynamic RAM (DRAM), and a static RAM (SRAM). The DRAM is used by the DVS200 to store sections of speech. The DRAM should have an organisation of 64K×1 and an access time of no greater than 150ns. The minimum timing requirements are shown in Fig. 8a; the TMS4164-15 is recommended, though any DRAM may be used as long as it has similar (or better) operational characteristics to those shown. Similarly, a larger bit-wide DRAM (the TMS4256-15, for example) may be used as long as the unused address inputs are tied.

The SRAM is used for code storage and as a scratch pad for general DVS200 operation. The SRAM requirements for the DVS200 are that it should have an organisation of at least 128×4, and a maximum access time of 200ns. The minimum timing requirements are shown in Fig. 8b; the PCD5114 satisfies this specification, though again, any SRAM whose performance is within the specification shown in Fig. 8b may be used.

Larger SRAMs can be used with the extra addresses either tied, or alternatively, be used as part of a paging system; this would allow the user to switch between sets of codes (by means of a switch on the equipment, for example) without having to continually re-seed the system. See Seed Data Paging (page 4-12).

DEVICE RESET

Each time the DVS200 is powered up, it must be reset so that the internal logic is set to a known state. This is achieved by taking the $\overline{\text{FRES}}$ input (pin 68) low for a period of time not less than 2 microseconds. A simple circuit for achieving this is shown in Fig. 11.

CLOCK OSCILLATOR

The DVS200 has a nominal clock frequency of 4.433619MHz, though it can run at clock frequencies of up to 8MHz (note that if the frequency is increased from the nominal, the access times of the DRAM and SRAM will have to be reduced by a similar factor). As well as the two oscillator pins, the DVS200 has an extra pin (SCLK-pin 8) that is a buffered version of the oscillator output, CLKOUT (pin 9). The SLCK output can, therefore, be used to set the oscillator frequency without loading the oscillator circuitry. The SCLK output can also be used to clock any external logic being used. The basic circuitry required to implement the oscillator is shown in Fig. 12.

ANALOG TO DIGITAL CONVERTER

The DVS200's analog to digital converter (ADC) is a serial adaptive delta modulator (ADM) that runs at a sample rate of 139kbit/s. The average input signal level should be approximately 1.7Vp-p; the ADC input should be driven by an impedance of less than 1kΩ. The external circuitry required, together with the recommended component values, are shown in Fig. 13.

DIGITAL TO ANALOG CONVERTER

The DVS200 has four outputs which, together with a few external passive components, form the digital to analog converter (DAC); these outputs are DACA (pin 70), DACB (pin 71), DACC (pin 72) and DACD (pin 73). Fig. 14 shows the connection details. It is recommended that the values shown in Fig. 14 are used as any modification may adversely affect the performance of the DAC. It is important to not to load the output of the resistor/capacitor network with an impedance or less than 100kΩ. If the input impedance of the interface circuitry is less than 100kΩ then the network should be buffered.

Any one of five different signals can be present on each of the outputs; the signals are: clear speech data, encrypted speech data, notch filter data, transmit sync tones and device clock. The mode in which the device is operating determines which of these signals are present on each output. The DVS200's DAC has six different modes of operation, each of which is selected by the control logic of the DVS200. A description of each mode, together with the signals present on each of the DAC outputs is given below:

(a) Tx Encrypted - The DVS200's normal transmit operation. Encrypted speech outputs from the DAC at the same amplitude as the signal input to the ADC. Encrypted speech data is present on all four of the DAC outputs.

(b) Tx Clear - In this mode the DVS200 outputs clear speech, again at the same amplitude as the signal input to the ADC. Clear speech data is present on all four of the DAC outputs.

(c) Tx Sync - This mode is invoked whenever transmission of a sync tone is requested, either by an activation of the DPTTIN input (pin 66; see Push-to-Talk Circuitry, page 4-10), or the periodic sync circuitry. The operation consists of two phases. The main phase involves the transmission of the sync tones. During this phase encrypted speech data is output from the DADC and DACB outputs, and sync tones are output from the DACC and DACD outputs. This has the effect of attenuating the speech by the factor of two (this will be compensated for by the Rx DVS200). This phase lasts for either 1.06s or 118ms (depending on whether the message key mode has been selected).

The other phase of this mode, which occurs immediately before the sync tone transmission phase, attenuates the speech output from the DAC (again, by a factor of two) for a period of 118ms. This has the effect of maintaining the speech at a constant level for the duration of a whole frame (or an exact multiple with the message key option selected). The attenuation is achieved by replacing the sync tone on DACC and DACD with the device clock.

(d) Rx Encrypted - The DVS200's normal receive operation. Note about that the output is attenuated (again, by a half) with respect to the ADC input. As with the first phase in (c) above, this is achieved by outputting encrypted speech data on DACA and DACB, and device clock on DACC and DACD.

(e) Rx Clear - In this mode the DAC outputs undecrypted speech (see Clear Voice Override, page 4-8): so if there is clear speech on the ADC, there will be clear speech on the DAC output. The situation is the same as that in (d) above, except for the fact that clear speech data outputs from DACA and DACB instead of encrypted speech data.

(f) Rx Notch Filter - The notch filter function is used to remove sync tones from the receive channel, and is therefore centred at the sync tone frequency of 1.082kHz.

As the notch filter attenuates other adjacent frequencies as well as the sync tone frequency, it is only selected whenever a sync tone has been received. When the DAC is in this mode, the speech is output from the DAC at the same level as it was presented to the input of the ADC. As the speech was transmitted at half its normal level during Tx sync (see (c), previous page) the level will be consistent throughout the receive mode of operation.

Table 3 summarises the various modes of operation of the DAC outputs, as well as the signal combinations that appear at the outputs during the various phases.

MESSAGE KEY

Basic Circuitry

The message key option is is selected by leaving the MKEY pin (pin 3) unconnected as an internal pullup holds the input at logic '1'. There is a small amount of external circuitry required for the message key operation which is shown in Fig. 16. This external circuitry is inserted between the DVS200 and SRAM on the D0 connection. Note that the circuit in Fig. 16 is for PTT active low - if PTT is active high, the $\overline{\text{PTT}}$ output should be used instead of PTTOUT). It is only functional in Tx mode, so if a DVS200 is being used exclusively in the Rx mode (in a duplex system for example) this circuitry is not required.

Message Key Derivation

While the DVS200 is in message key mode, 32 bits of data (the message key) are required each time a sync tone is transmitted. Each time the Tx sync circuitry requires a data bit for the message key, it samples the input RND (pin 1); there is a free-running latch on this input, clocked at a frequency of 138kbits/s. The signal presented to this input can be derived from any source, but it should be random in nature. There are many ways of deriving this signal; one way is to connect the RND input to the ADCIN input. Another method of deriving this signal is to connect a noisy diode to the RND input.

There is in addition to the RND input, an output called $\overline{\text{RND}}$ (pin 4). This is the inverted output of the latch on the RND input and can be used to help derive the message key data. For example, it could be used, with RND, to form an oscillator circuit; or it could be used to form another ADC circuit (like that shown in Fig. 13). Any of these methods, or indeed any other, can be used to derive the message key.

Message Key Mute

When the Rx DVS200 receives a sync tone (with or without message key) the notch filter at the DAC is activated; this notch filter is centred at the sync tone frequency. With a message key transmission the sync tone may be changing phase every 32 periods, depending on whether the message key data is changing.

At these data boundaries the sync tone will not be a 50% duty cycle square wave (see Fig. 6b). The notch filter will not be able to eliminate this from the channel. This will result in a glitch on the final speech waveform which may be large enough to be heard over the speech present on the channel.

One way to eliminate this glitch is to mute the channel (post-DVS200) each time a glitch is expected. A circuit providing a 1ms pulse each time a glitch is present is shown in Fig. 17. This logic output (Mute Out) can then be connected to an FET, or analog switch, that will shunt the channel each time a glitch is present.

The channel should be shunted to a voltage equal to the bias level, otherwise a glitch may be introduced that is larger than the one the circuit is designed to eliminate!

SYNC INPUT

The receive analog channel of the equipment should be fed into the SYNCIN Input (pin 15) before it has been processed by the Rx DVS200. SYNCIN is a digital input, so the signal present on this input must be a squarewave with a 50% duty cycle.

You will have noticed in Fig. 6a that the sync tone present on the Rx SYNCIN input is inverted with respect to the sync tone at the Tx DAC output. This relationship should be maintained wherever possible. A simple sync tone inverter-cum-conditioner is shown in Fig. 15.

PUSH-TO-TALK (PTT) CIRCUITRY

The PTT circuitry usually indicates that a piece of simplex equipment (a mobile radio, for example) is in transmit mode. It is usually derived by the user by means of an external switch. As the DVS200 is also a single channel device it has receive and transmit modes; the simplex equipment's PTT signal can therefore be used to select the operational mode of the DVS200 (i.e. receive or transmit).

Mode of operation	DACA (Pin 70)	DACB (Pin 71)	DACC (Pin 72)	DACD (Pin 73)
Tx Encrypted	Encrypted Data	Encrypted Data	Encrypted Data	Encrypted Data
Tx Clear	Clear Data	Clear Data	Clear Data	Clear Data
Tx Sync	Encrypted Data	Encrypted Data	Clock/Sync Tone	Clock/Sync Tone
Rx Encrypted	Decrypted Data	Decrypted Data	Clock	Clock
Rx Clear	Clear Data	Clear Data	Clock	Clock
Rx Notch Filter	Notch Filter Data	Decrypted Data	Decrypted Data	Notch Filter Data

Table 3 Summary of Digital-to-Analog Converter operation

The DVS200 has two PTT inputs and two PTT outputs. The polarity of these pins, i.e. whether the transmit mode is active on a high PTT or low PTT, is determined by the option pin PTTP (pin 84). In the following paragraphs it is assumed, for simplicity, that the PTT signal is active low.

As mentioned above, there are two PTT inputs; they are PTTIN (pin 65) and DPTTIN (pin 66). The PTTN input should be connected directly to the PTT signal. On some pieces of equipment, there is a delay between the PTT signal going active and the channel opening on the receive equipment. This can be due to any number of factors; squelch circuitry and voting systems are just two examples of channel opening delays. On PTT activation, the DVS200 transmits sync tones. It is imperative that the DVS200 in the receive equipment receives all of the sync tones, otherwise it may not synchronise correctly (the DVS200 must receive a minimum of 96 out of 128 periods of the sync tone transmitted by the Tx DVS200). It is therefore necessary to delay the transmission of the sync tones until the channel is open on the receiver. The input DPTTIN is used for this purpose. The sync tone is transmitted 118ms after DPTTIN goes active. If this is long enough for the receive channel to open, then DPTTIN should be connected directly to PTTIN. If this is not a long enough delay, a delay stage should be inserted between PTTIN and DPTTIN. Alternatively, if there is a signal available on the transmitting equipment that indicates that the channel is open, then this may be connected to the DPTTIN input (assuming it is the same polarity as the PTT signal).

Note that this delay should be on the active edge of the PTT signal only, otherwise the transmit channel will be held open for a time equal to that of the DPTTIN delay. A simple circuit for introducing a delay is shown in Fig. 18. The resultant timing is shown in Fig. 4.

Because of the nature of the encryption technique, there is a time delay, of approximately 236ms, between the speech input and the encrypted output. A consequence of this is, that when the user releases the PTT switch, there will still be speech stored in the DRAM waiting to be output. For this reason the DVS200 delays de-selecting the transmit mode of the transmitting equipment. This delay, PTT_{DEL} in Fig. 4, ranges from 236ms (one frame length) to 450ms, depending on the point in the frame at which the PTT switch is released.

The result of this is that there is a difference between the PTT input and the PTT output. So, the PTT signal that was previously connected to the transmitter cannot now be used; it must be disconnected and the DVS200's PTTOUT (pin 7) signal should be re-connected in its place.

The $\overline{PTT}$ output (pin 6) is an inverted version of PTTOUT, and can be used to control any analog switches that are needed to switch between the Rx and Tx speech channels.

PERIODIC SYNC

In transmit mode, the periodic sync circuitry automatically initiates the transmission of a sync tone at regular intervals. There are several problems that can be solved by utilising the periodic sync option. One is the problem of late entry into net. This phenomenon occurs when a receiver is turned on during a transmission. Normally, the user in this situation will be unable to recover encrypted speech correctly until another transmission has been initiated, i.e., another sync tone has been transmitted. With periodic sync, the maximum duration the late entry user will be out of synchronisation will be equal to just over the periodic sync interval.

Another problem that can be cured with periodic sync is that of multiple path reception. This occurs when the transmitter and/or receiver are mobile and results in varying time reference between the Tx and Rx DVS200s; thus causing synchronisation error. With periodic sync, this error will only persist until the next sync tone is received, so the periodic sync option is again beneficial.

The periodic sync option is implemented by connecting a resistor/capacitor time constant between the pins PERIOD (pin 13) and PEROUT (pin 14) as shown in Fig. 19. The periodic sync interval is then 190 times the RC time constant. If the periodic sync option is not required, then the PERIOD input should be tied to either V_{DD} or V_{SS}.

Note that the sync tones are transmitted at a particular point in a frame, so the intervals between each sync tone will not correspond exactly to the interval determined by the periodic sync RC; there may be an additional time of anything between 0 and 460ms, depending upon where in a frame the periodic sync operation is completed.

As mentioned earlier, the periodic sync also affects the device in receive mode. The periodic sync circuitry is used to detect whether the device is being used in encrypted mode during receive operation. If the Rx does not receive a sync tone within a period equal to that of twice the periodic sync interval, the device switches to clear speech mode. It remains in this state until it either receives a sync tone, or PTT goes active (assuming the $\overline{CVOICE}$ pin is not active, i.e. high).

If this automatic override is not required, then the periodic sync option should not be selected in receive mode.

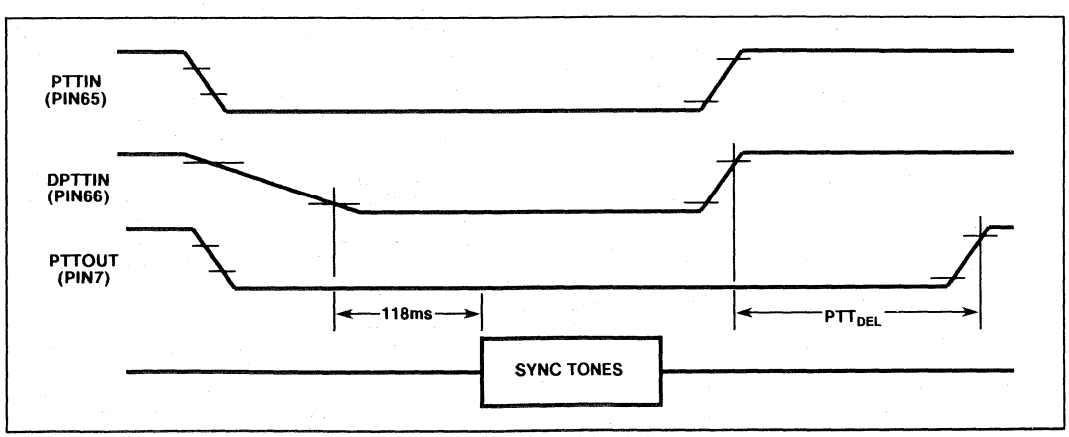


Fig. 4 PTT to Sync delay timing

SEED DATA ENTRY

Before the DVS200 can perform any encryption function seed data has to be loaded into the code storage registers in the SRAM. With this seed data the key generator can be used to derive a sequence of segment transpositions. This seed data then is the code that must be inserted into the DVS200, of both the Tx and Rx user, before the encrypted speech can be correctly recovered. There are several different ways of entering the code. These can be divided into two categories; automatic strobe, and external strobe. Both of these should be performed immediately after the device has been reset ($\overline{FRES}$ active).

Seed Data Entry - Automatic Strobe

With this method the seed data is loaded automatically from an external bank of switches. It is selected by tying the KINJ input (pin 63) to V_{SS}. It has the advantage of removing the necessity for battery back-up facilities, as the switches are always present on the seed data input port. So, whenever the device is reset, the switches are simply read into the code storage registers.

The switches must be arranged in banks of four, and can be any multiple from four to sixteen. The four switch option gives low security (16 possible codes) but uses a smaller amount of board space (see Fig. 20). The inverse is true of the sixteen switch configuration; it offers greater security (65336 possible codes), but this occupies greater board area. The decision about the number of switches to be used for code entry is, therefore, mainly governed by the amount of board space available, and the degree of security required.

One of the terminals of each switch in each bank is connected to one of the inputs on the seed data input port, SD0-SD3 (pins 76, 77, 78, 79). This connection should be made via a diode if the number of switches is greater than four (see Fig. 21). The other terminals are then grouped together in their respective banks. If there is more than one bank of four switches each bank should be connected to one of the seed strobe outputs. $\overline{SSTB0}$-$\overline{SSTB3}$ (pins 59, 60, 61, 62); otherwise these terminals should be connected to V_{SS} (see Fig. 20). Each one of these four strobe outputs must be connected to a bank of switches (if more than four switches are used). If an eight or twelve switch configuration is used some of the $\overline{SSTB}$ outputs should be connected together, ensuring that the number of strobe nodes is equal to the number of switch banks (see Fig. 21). The timing diagram for automatic seed data entry is shown in Fig. 9.

Seed Data Entry - External Strobe

This method of seed data entry is selected by tying the KINJ input (pin 63) to V_{DD}. The main advantage of this method of seed data entry is that there is a total of 128 bits (entered as 32 nibbles) of seed data. This gives approximately 3.4×10^{38} possible permutations. To enter the code in this method a nibble is placed on the seed data entry port, and then strobed into the DVS200 using the $\overline{ISTRB}$ input (pin 64 - active on the negative edge). This is repeated for each of the 32 nibbles. With this method of seed data entry the contents of the SRAM must be retained (using battery back-up) each time the DVS200 is powered down, otherwise the codes will be lost (see Seed Data Override below).

There are two ways to implement this. The first is to use a key fill gun; this supplies the necessary data and strobe signals via an external connector. The other way to do this is to use external logic to access a PROM (32×4 minimum) each time the DVS200 is reset. The necessary timings for strobe controlled seed data entry are shown in Fig. 10.

Seed Data Paging

When an SRAM with excess capacity is used (i.e. greater than 128×4), it is possible to utilise the remaining space to supply the user with a choice of codes. This is achieved by connecting a set of switches to the extra address pins available on the SRAM. Each one of the different switch settings will address a different page of 128×4 (the normal block used by the DVS200). Each one of these pages can be used to hold a different set of codes that can be selected by altering the switch settings.

This means, of course, that each page has to have a code loaded into it. This is done by resetting the DVS200 several times (thus loading seed data), changing the page address and seed data each time the device is reset. The sequence of events for paged data loading is shown in Fig. 5.

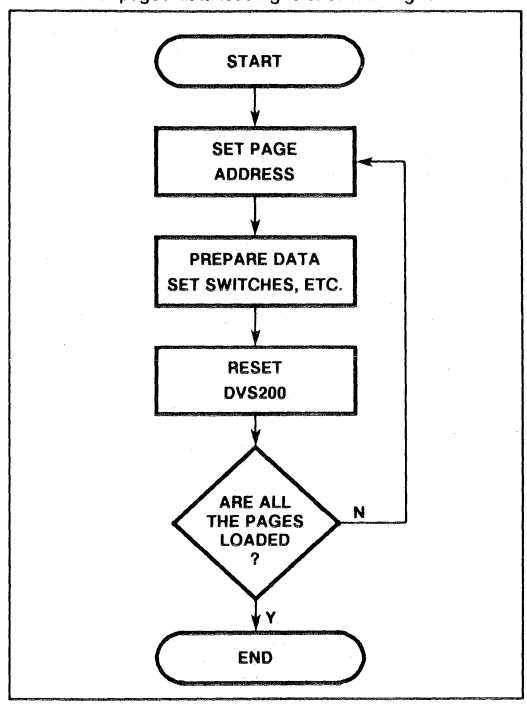


Fig.5 Loading Paged Seed Data

If the seeding is being done using the external strobe option, the $\overline{FRES}$ pulse can be supplied by either the keyfill gun, or the external logic, depending on which is being used. If automatic seeding is selected, the $\overline{FRES}$ pulse can be supplied by an external push-button switch. This is then pressed each time the switches have been correctly set to their new settings (both the seed data and page addresses).

When the paging option is used, the automatic seeding option (described under Automatic Strobe, above) will also have to have battery back-up on the SRAM. If this is not done, each page will have to be re-loaded each time the DVS200 is powered down.

Seed Data Override

In some applications it may not be desirable to load seed data each time the DVS200 is reset (when the device is powered-up). The code may be loaded into the device by a master keyfill gun at the beginning of the day and then retained, during power down phases, by battery back-up on the SRAM (this also applies to paged data).

Each time seed data entry is required, the SEED input pin (pin 81) must be taken high either before or during device reset (see under PTT Circuitry on page 4-10 and External Strobe, above). Once the code entry has been completed the seed input can then be taken low. This will then inhibit the device from overwriting the stored codes on each subsequent device reset.

TIMING DIAGRAMS

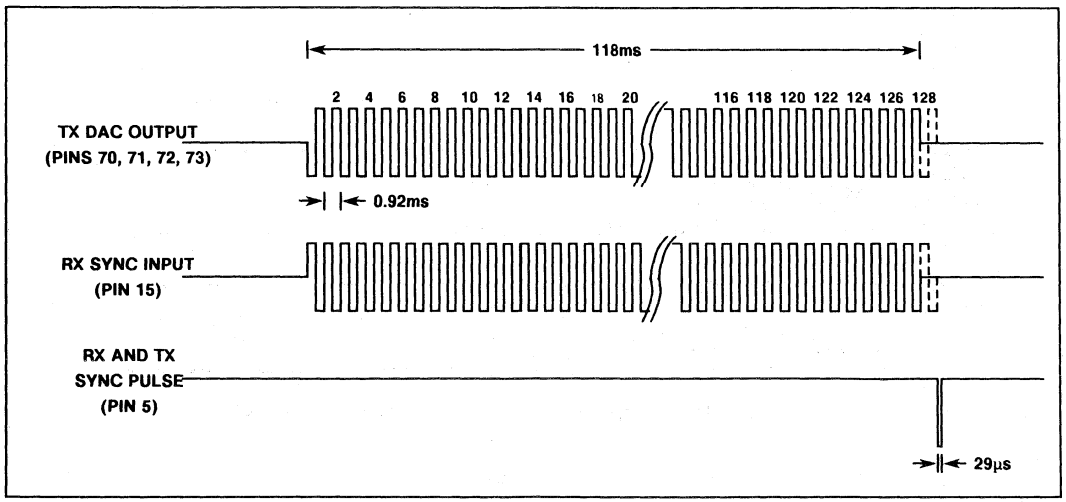


Fig.6a Synchronisation (no Message Key)

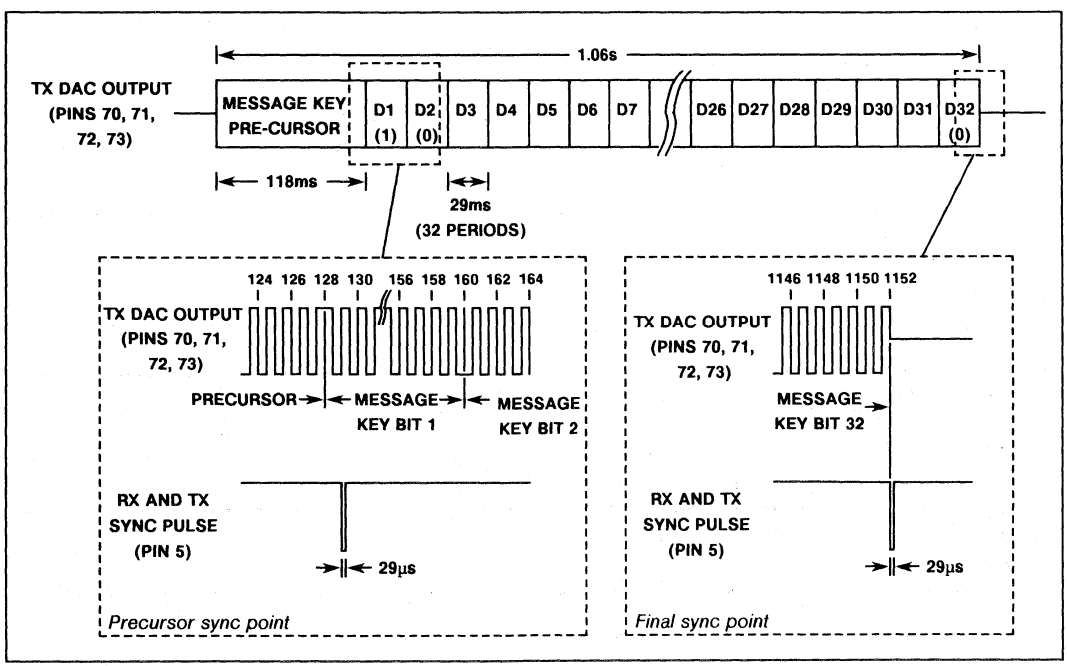


Fig.6b Synchronisation (with Message Key)

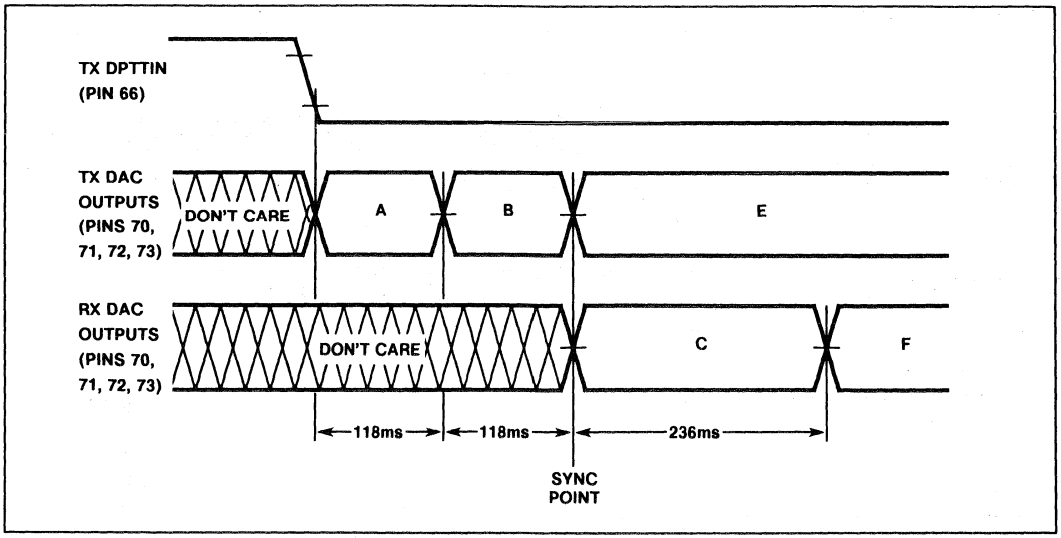


Fig.7a DAC operation (no Message Key)

Figs. 7a and 7b Key

A - Attenuated speech
B - Sync Tones with attenuated speech
C - Notch Filter
D - Message Key with attenuated speech
E - Normal Tx operation
F - Normal Rx operation (Attenuated)

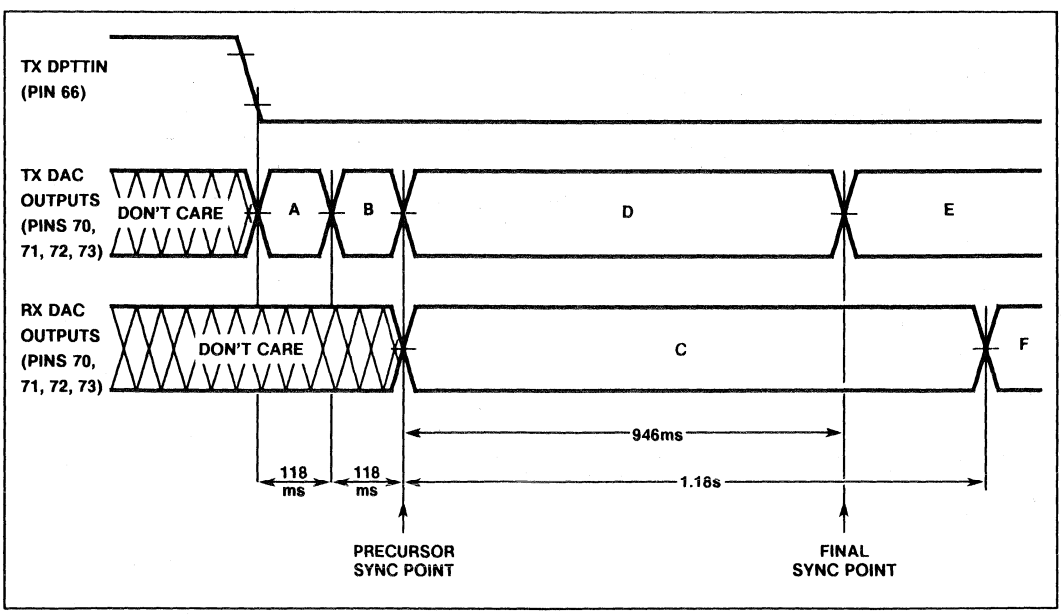


Fig.7b DAC operation (with Message Key)

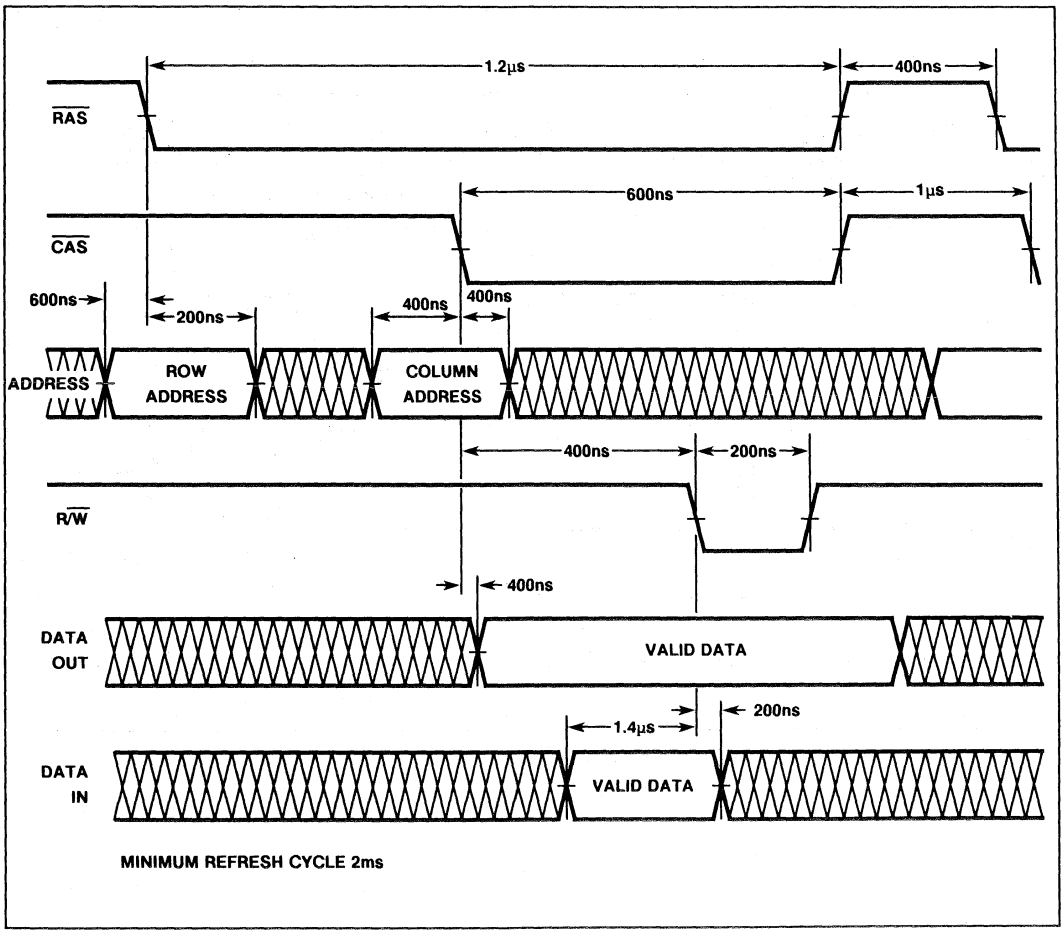


Fig.8a DRAM Read/Write cycle

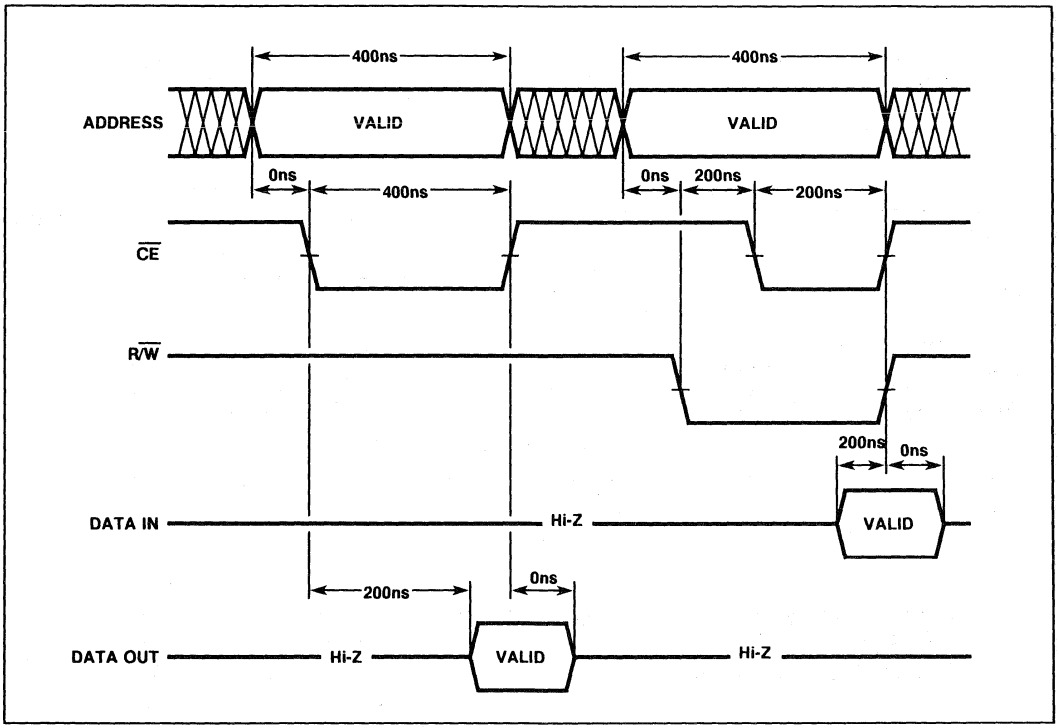


Fig.8b SRAM read/write cycle

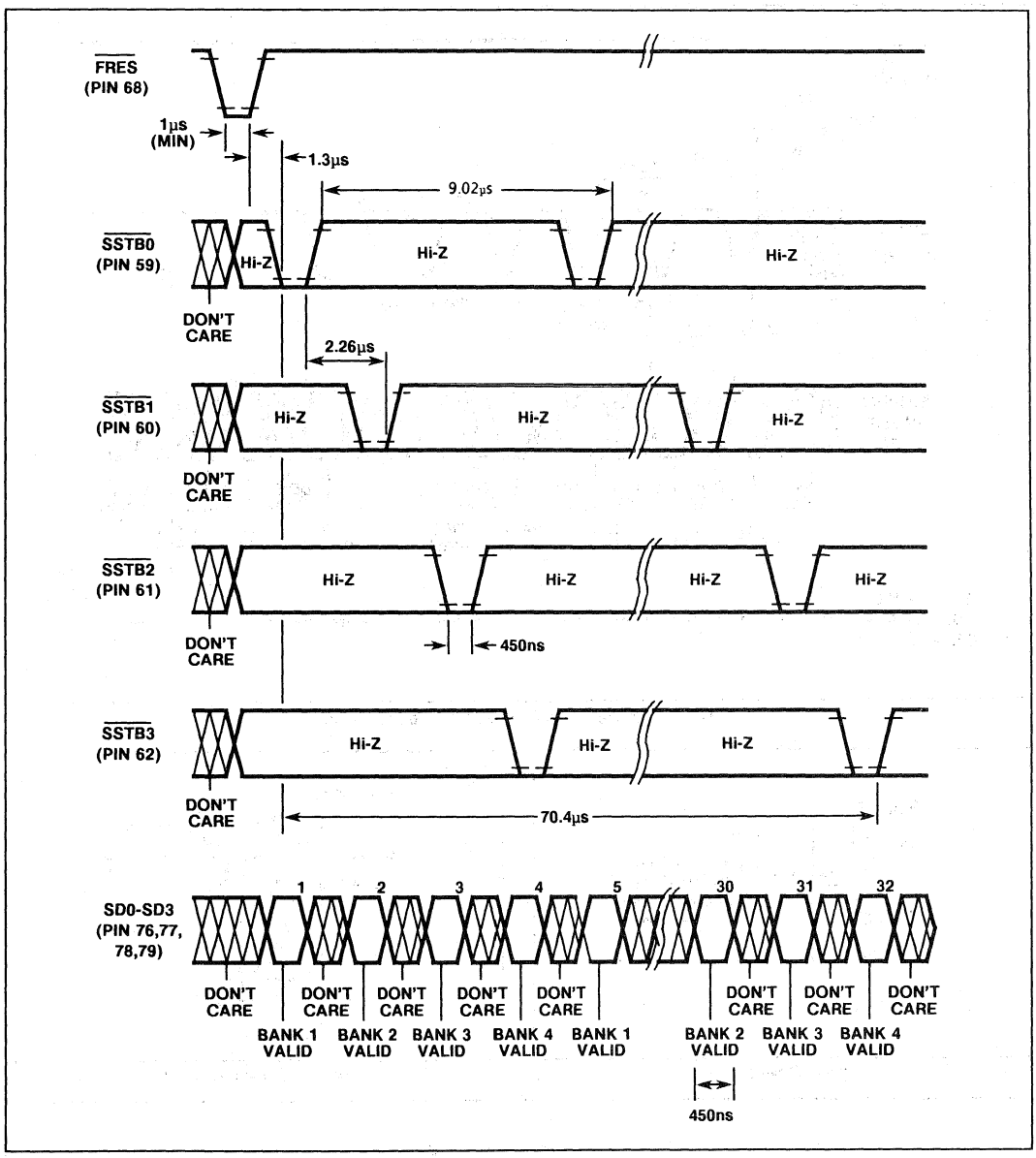


Fig.9 Automatic seed data entry timing

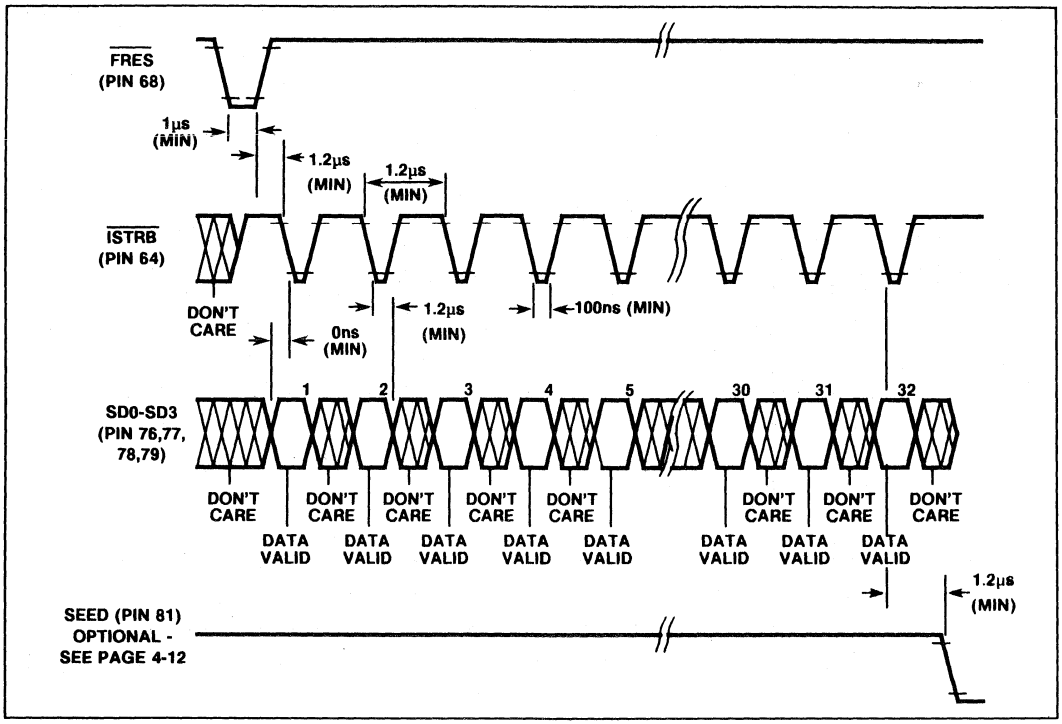


Fig.10 Strobe-controlled seed data entry timing

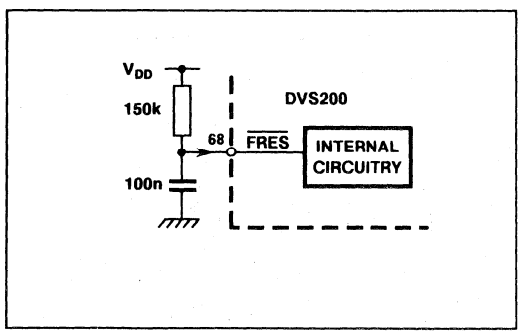


Fig.11 Device reset

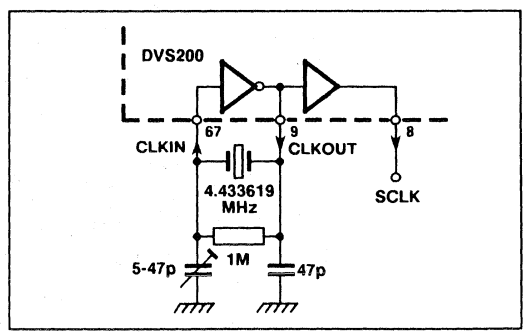


Fig.12 Clock oscillator

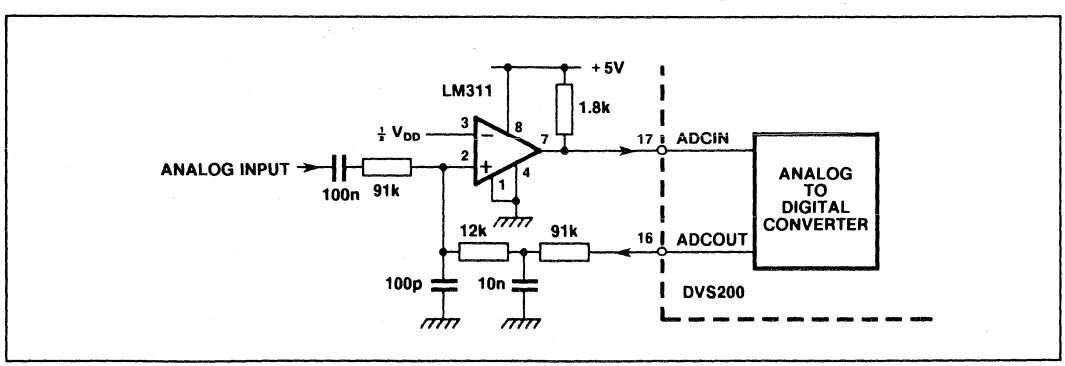


Fig.13 ADC external circuitry

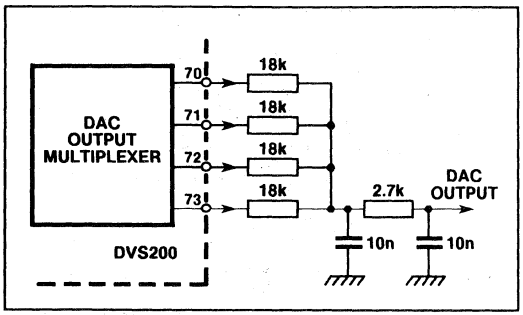


Fig.14 Digital to analog converter

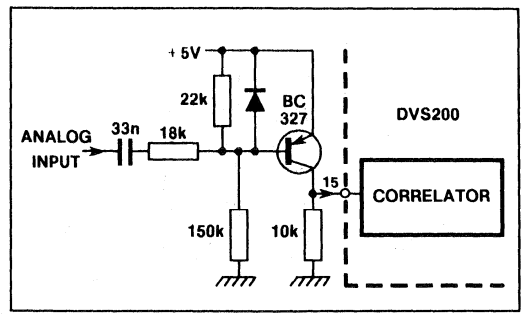


Fig.15 Sync tone inverter

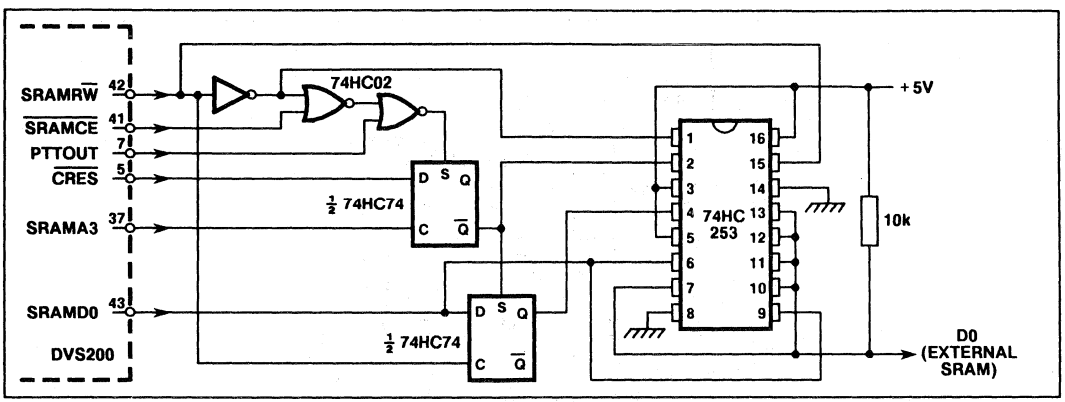


Fig.16 Tx message key circuitry

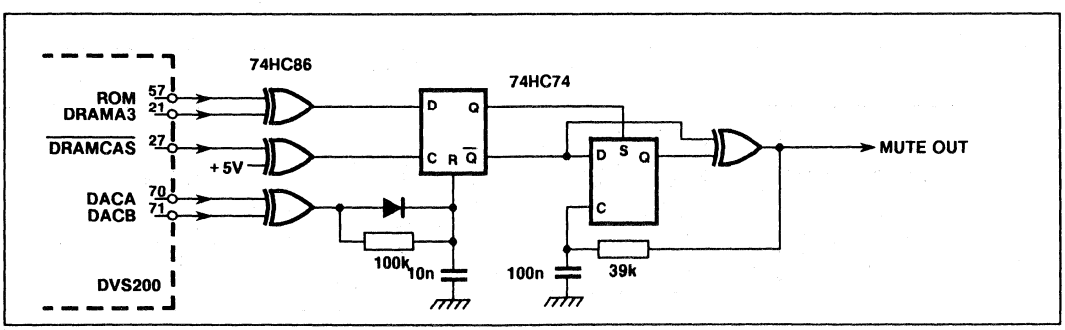


Fig.17 Rx message key circuitry

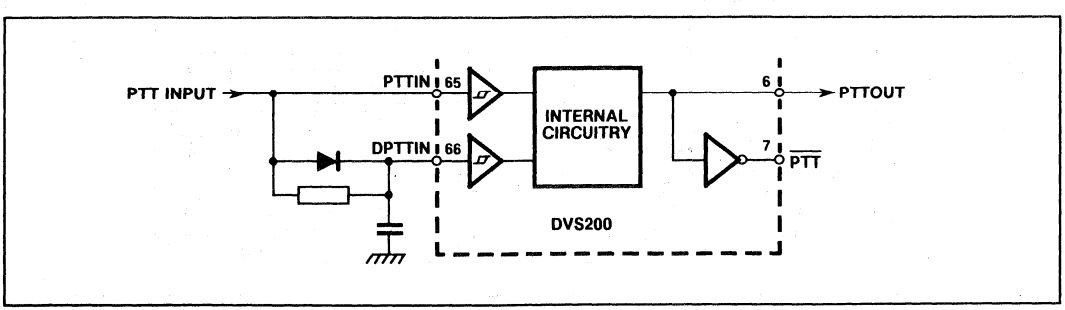


Fig.18 PTT to sync delay circuit

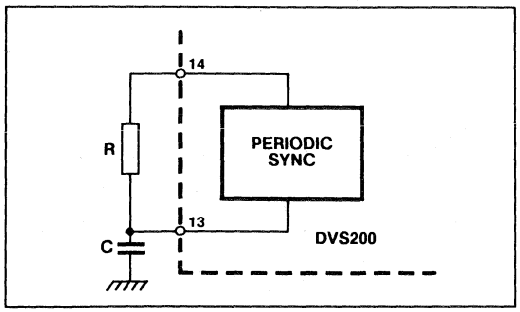


Fig.19 Periodic sync circuit

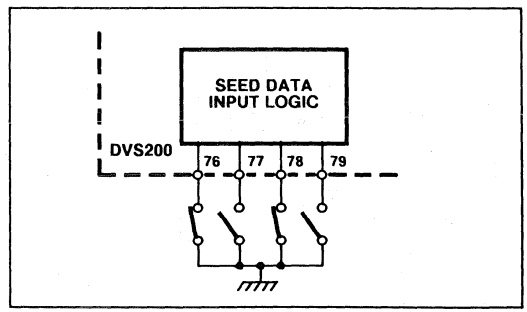


Fig.20 Seed data entry - four switches

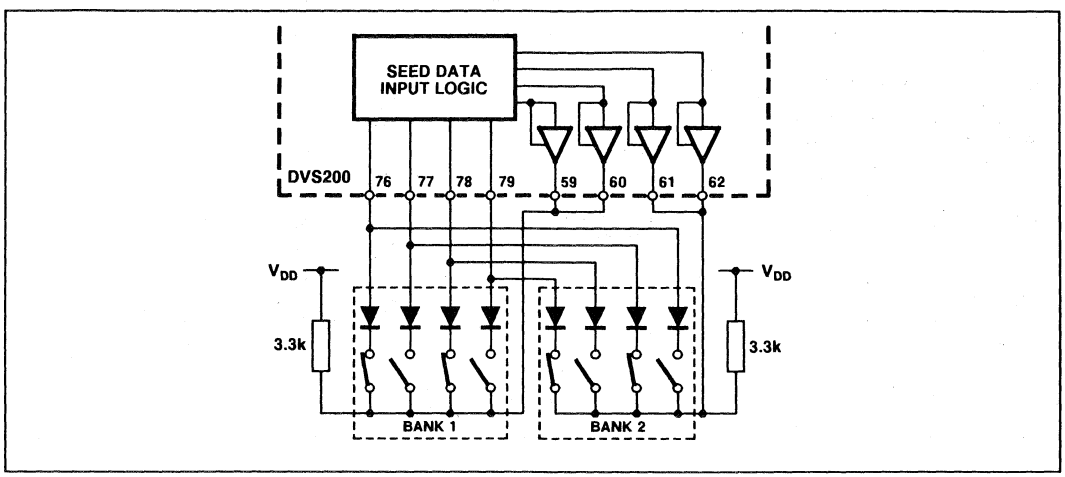


Fig.21 Seed data entry - eight switches

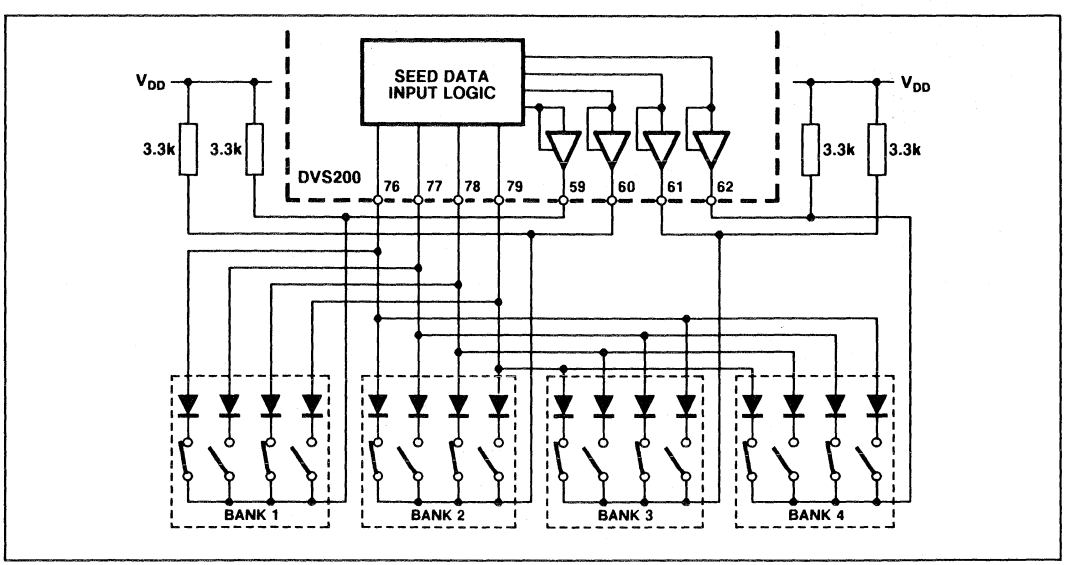


Fig.22 Seed data entry - sixteen switches

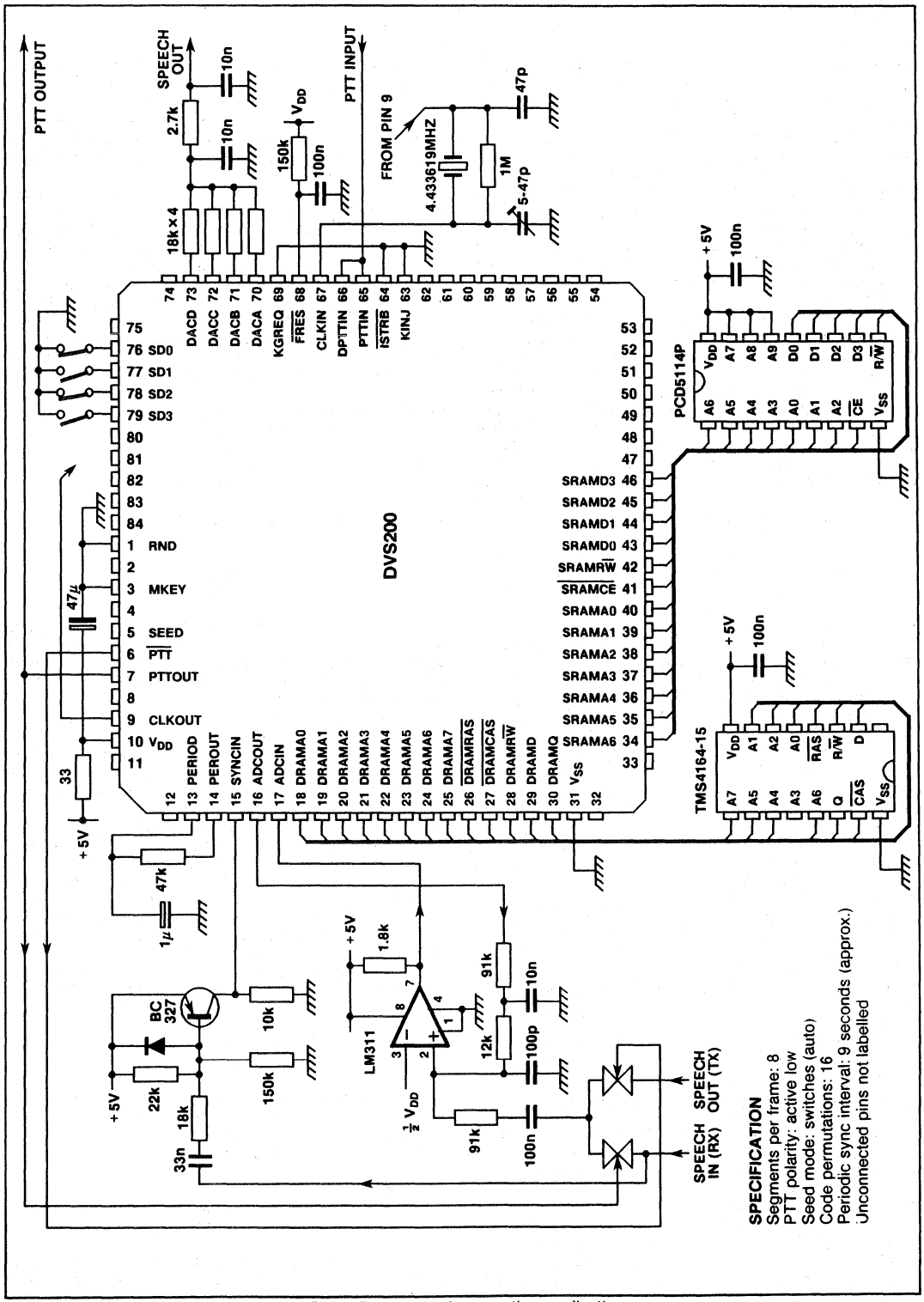


Fig.23 Basic speech encryption application

DATA ENCRYPTION

OVERVIEW

The DVS200 has a data encryption mode which can be selected by connecting the option pin KGOP (pin 83) to V_{SS}. When in this mode, the output of the DVS200's on-chip key generator can be used to encrypt a low-bandwidth data stream.

The data stream is encrypted by modifying each bit of data before it is transmitted. The modification of the bit is determined by the pseudo-random output of the DVS200's key generator, and is usually achieved with the modulo-2 addition of the data stream to the key generator output, using an EXOR gate. The output of this gate is the encrypted data stream and can, therefore, be transmitted over the vulnerable network or link. The data is recovered by simply repeating the procedure at the receive end.

BASIC OPERATION

Before data encryption can begin, there are three operations that need to be performed. The first requirement is that the DVS200's is reset by activating the $\overline{FRES}$ pin (see page 4-9). The second phase is that the code storage registers are loaded with the seed data; this happens automatically whenever the DVS200 is reset. The details of this operation are described on page 4-12. Once this has been done the seed data in the code storage registers needs to be transferred to the key generator. In the speech encryption mode this is usually done when synchronisation occurs. In data encryption mode this can be simulated by taking the PTTIN and DPTTIN pins low (see pages 4-10 and 4-11) for at least 240ms. Each time the DVS200's key generator is reseeded (i.e., the key generator is reset) it is essential that the first and third phases of the initialisation process (device reset and synchronisation) are performed. If the seed data has already been entered, the second phase can be omitted by activating the SEED option pin (see Seed Data Override, page 4-12). The flow diagram of Fig. 24 shows the key generator initialisation sequence.

Just before a data bit is ready to be transmitted, a word should be requested from the DVS200's key generator. This is achieved by strobing KGREQ (pin 69). A number of clock cycles after the falling edge of KGREQ, the key generator will indicate the presence of a valid four bit word on the key generator output port (KGD0-KGD3) with a logic '0' on the $\overline{KGRDY}$ output. The timing for the signals involved with a request for a word from the key generator is summarised in Fig. 25.

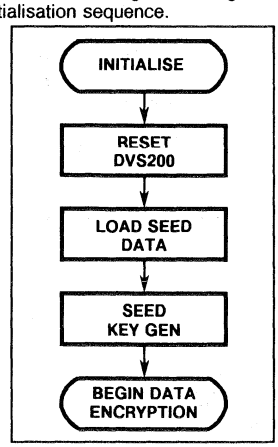


Fig.24 Key generator initialisation sequence

The key generator output is in the form of a four bit word; usually, the data to be encrypted is in serial form. If this is the case, the output of the DVS200's key generator should be loaded into a four-bit shift register; the shift register should then be clocked each time one of the bits from the nibble is required. It is, therefore, only necessary to request a word from the key generator every fourth bit in the data stream. A circuit diagram illustrating the implementation of this basic data encryption application is shown in Fig. 26. A timing diagram showing the relevant signals for this application is shown in Fig. 27. Note that in this application, the external DRAM is omitted as it is only required for storing sections of speech in the speech encryption mode. The DRAMQ input (pin 30) is therefore connected to V_{SS}.

DATA RATES

Unbuffered Key Generation

Because of the nature of the DVS200's key generator, the time that elapses between a KGREQ strobe and a valid output appearing on the key generator output port is variable. It is the time that elapses between these two events that determines the maximum rate at which the key generator can be accessed, and hence the maximum data rate that can be encrypted.

If a clock of fixed period is used to strobe the KGREQ pin, and no form of storage buffer is used (other than the four bit shift register), the minimum period of this clock must be equal to the maximum possible time taken to complete a key generator operation. If the four-bit shift register is loaded before $\overline{KGRDY}$ strobes low (key generator operation complete), erroneous data will be read from the key generator output port.

The maximum time taken to complete a key generator operation is equivalent to 9100 times the period of the device clock. So for a clock of 4.433619MHz:

Maximum time for Key Generator Operation
$= 9100 \times 225.5\text{ns}$
$= 2.05\text{ms}$
$\therefore$ Max number of Key Generator operations per second
$= (1/2.05) \times 10^3$
$= 487$
As the key generator outputs four bits:

Equivalent Data Rate
$= 4 \times 487\text{bits/s}$
$\approx 1.9\text{kbits/s}$

This means in this system the DVS200 can encrypt data streams operating at data rates of up to 1.948kbits/s. If the device clock were to be increased to 6MHz, the DVS200 could encrypt data streams at rates of up to 2.637kbits/sec.

Buffered Key Generation

Buffered key generation is a method of increasing the data encryption rate possible with the DVS200.

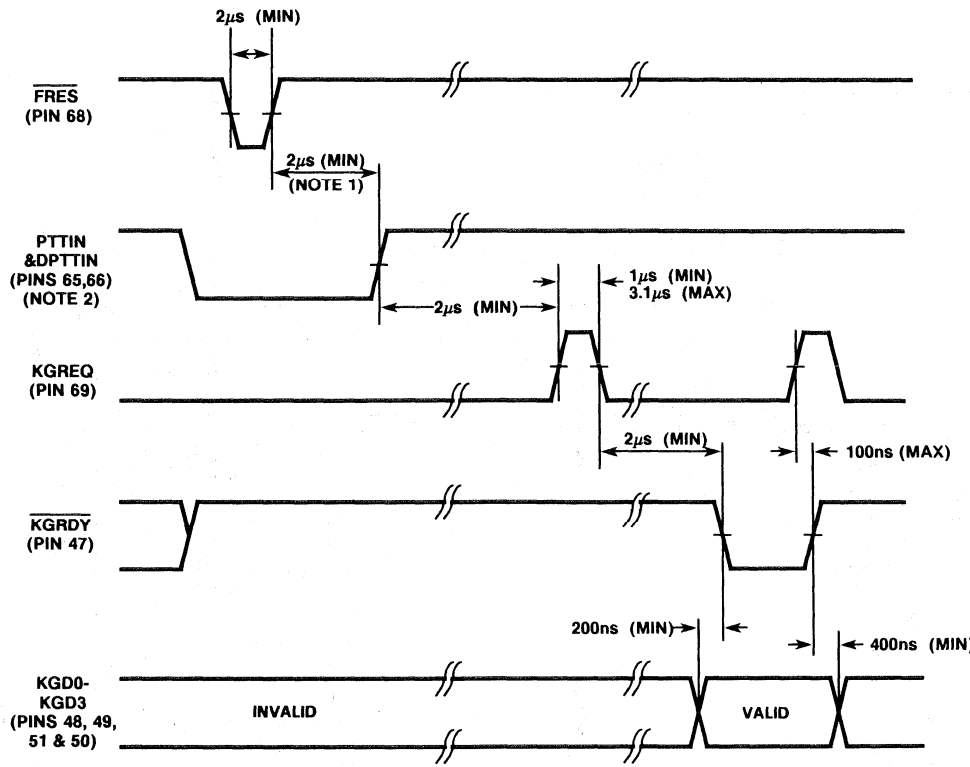
In this mode, the key generator is allowed to 'free-run' This is achieved by connecting the KGREQ input to the $\overline{KGRDY}$ output via an inverting gate. The 'free-running' mode is controlled by an externally supplied logic signal which is gated with $\overline{KGRDY}$. Once 'free-running', words will appear on the key generator outputs at variable intervals. These words can then be buffered externally and clocked out of the buffer at a fixed rate equal to the *average* time taken to complete the key generation cycle. This method gives an 86% increase in the equivalent data rate over the method described above for only a small increase in the amount of external logic required.

The average key generation cycle time is equivalent to 4900 times the period of the device clock. For a clock of 4.433619MHz:

Average time for Key Generator operation
$= 4900 \times 225.5\text{ns}$
$= 1.1\text{ms}$
$\therefore$ Possible number of Key Generator operations per second
$= (1/1.1) \times 10^3$
$= 909$
As the key generator outputs four bits:

Equivalent Data Rate
$= 4 \times 909\text{bits/s}$
$\approx 3.6\text{kbits/s}$

Hence, with a storage buffer, the DVS200 can encrypt data streams at rates of up to 3.6kbits/s, (or up to 4.8kbits/s with a device clock of 6MHz).



NOTES
1. The figure quoted applies when no seed data is to be entered (battery back-up). If seed data is to be entered, this time should be equal to the time taken to enter the seed data (see Seed Data Entry, page 4-12).
2. PTT is selected to be active high (PTTP tied low).

Fig.25 Key generator timing diagram.

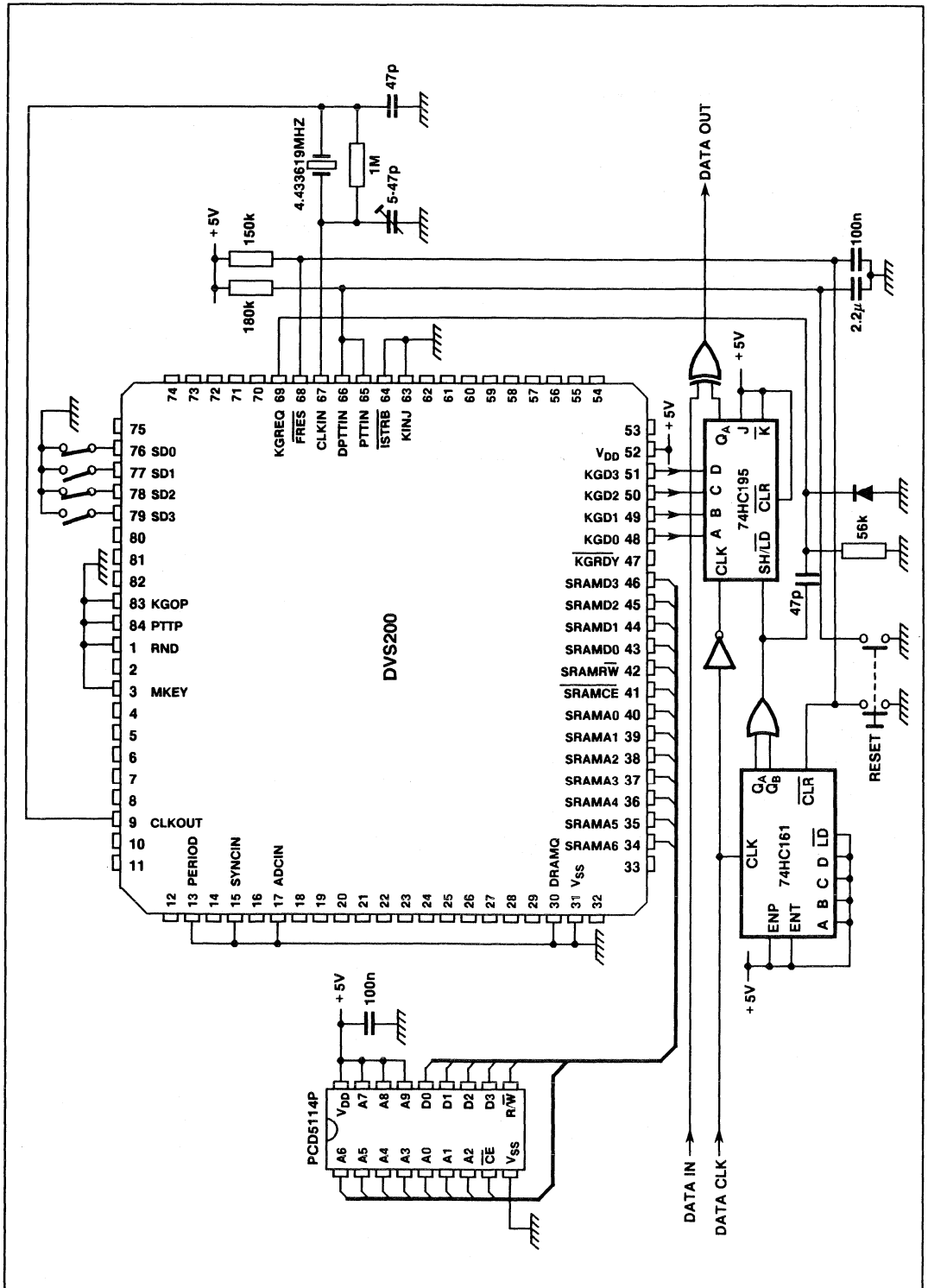
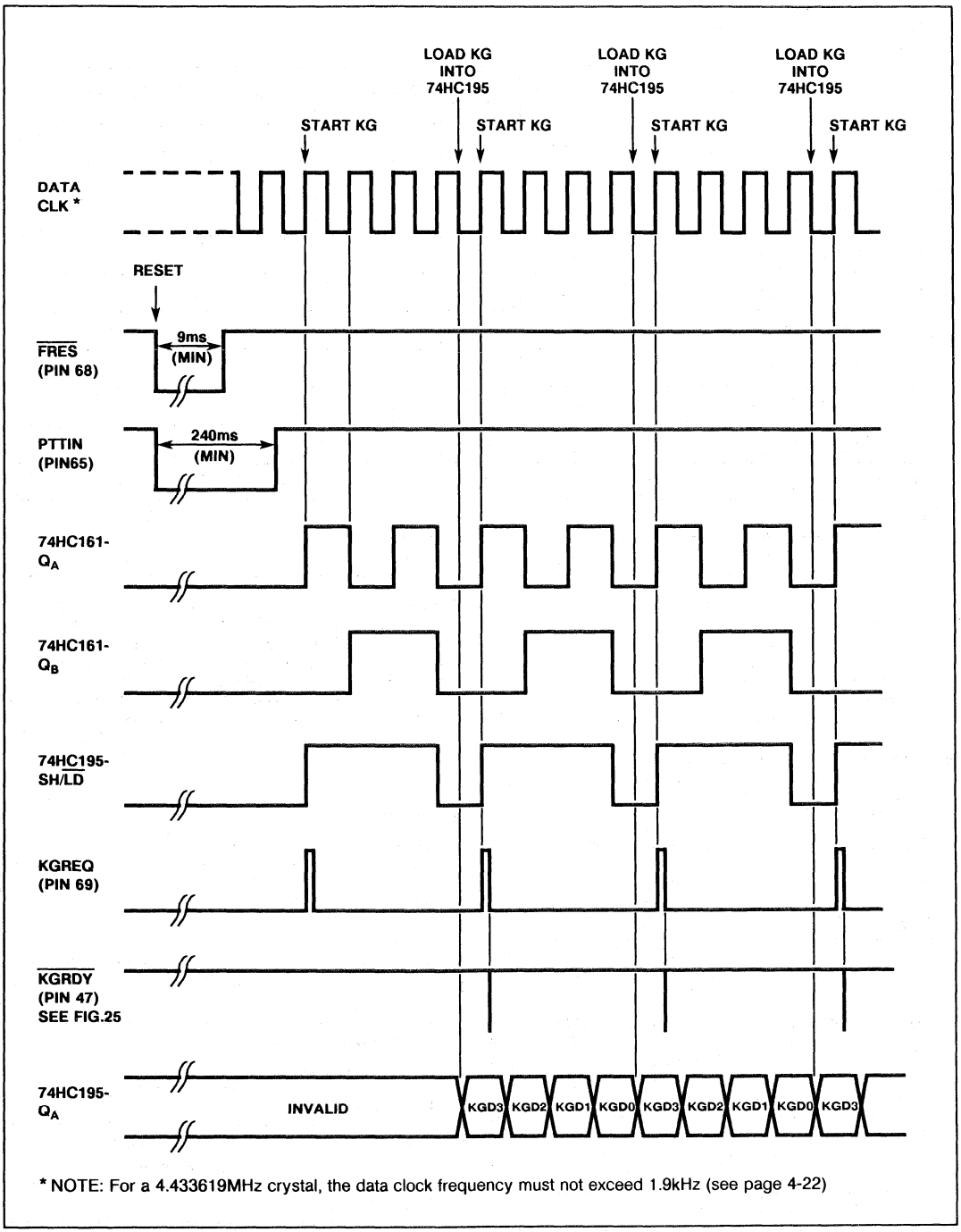


Fig.26 Basic data encryption application (unbuffered key generation - see text, page 4-22)



* NOTE: For a 4.433619MHz crystal, the data clock frequency must not exceed 1.9kHz (see page 4-22)

Fig.27 Timing diagram for data encryption application, Fig. 26

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{DD} = 5V \pm 10\%$, $T_{AMB} = -40°C$ to $+85°C$

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	3	-	7	V	
Power supply current	I_{DD}	-	5	-	mA	$V_{DD} = 5V$
TTL input high voltage	V_{IH1}	2	-	-	V	
TTL input low voltage	V_{IL1}	-	-	0.8	V	
TTL Input leakage current	I_{IL1}	-	-	10	μA	$V_{IN} = V_{SS}$ or V_{DD}
TTL Tri-state leakage current	I_{OZ}	-	-	10	μA	$V_{IN} = V_{SS}$ or V_{DD}
Schmitt input high voltage	V_{IH2}	-	3.2	-	V	
Schmitt input low voltage	V_{IL2}	-	1.8	-	V	
Schmitt input leakage current	I_{IL2}	-	-	10	μA	
Output high voltage	V_{OH}	2.4	-	-	V	$I_{OH} = -2mA$
Output low voltage	V_{OL}	-	-	0.4	V	$I_{OL} = 4mA$
Input pullup resistance	-	-	10	-	kΩ	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	10V
Voltage on any pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Short circuit output current	10mA
Power dissipation	1W
Storage temperature	$-65°C$ to $+150°C$
Operating temperature range	$-40°C$ to $+85°C$

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

FUNCTIONAL SPECIFICATION

All figures quoted at $V_{DD} = 5V \pm 10\%$, $f_{CLK} = 4.433619MHz$

Encryption	
Technique	TDM and time inversion
Frame length	236ms
Segments per frame	8/16 (option)
System delay	236ms per end
A to D Conversion	
Conversion method	Adaptive Delta modulation
Sample rate	139kbits/s
Average input signal level	1.7Vp-p
Dynamic range	40dB
Idling noise	10mV
SNR (1kHz at 1.7Vp-p)	45dB
Psophometric noise	Better than – 45dBm

Key Generator	
Sequence length	1.329 × 1036
Sequence number	260
Key variable entry (switches)	16 bits
Key variable entry (keyfill; gun)	1228 bits
Synchronisation	
Sync tone frequency	1.082 kHz
Sync tone decoding	Correlation
Periodic sync	Period variable (external RC)
No. of message key bits	32
Message key modulation	Phase

Section 5
Fibre Optic Links/LANs

SL9901

50MHz TRANSIMPEDANCE AMPLIFIER

The SL9901 is a monolithic silicon integrated circuit designed to interface between a detector diode and a decoder in a Fibre Optic Receiver System.

The device is also available as the SL9901AC, which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

FEATURES

- High Sensitivity
- 50MHz Bandwidth (100 Mbit/s NRZ Data Rate)
- Wide Dynamic Range
- -40°C to +85°C Operating Range
- Usable in System with 10^{-9} BER at -36dBm Average Power

APPLICATIONS

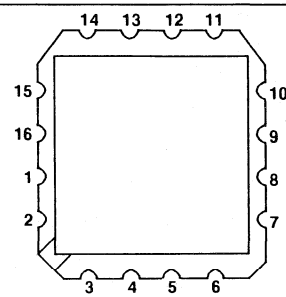
- Fibre Optic Data Links
- Nucleonics
- Instrumentation
- Current/Voltage Conversion

ORDERING INFORMATION

SL9901 B MP (Industrial - miniature plastic surface mount package)
SL9901 B LC (Industrial - leadless chip carrier)
SL9901 AC LC (Military - leadless chip carrier, screened to MIL-STD-883C CLASS B)

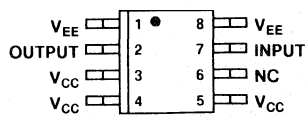
ASSOCIATED PRODUCTS

SP9960 50M-Bit Manchester Biphase Encoder
SP9921 50M-Bit Manchester Biphase Decoder



LC16

Pin	Function	Pin	Function
1	NC	9	OUTPUT
2	NC	10	NC
3	V_{EE}	11	NC
4	V_{EE}	12	V_{CC}
5	V_{EE}	13	V_{CC}
6	V_{EE}	14	V_{CC}
7	NC	15	NC
8	NC	16	INPUT



MP8

Fig.1 Pin connections - top view

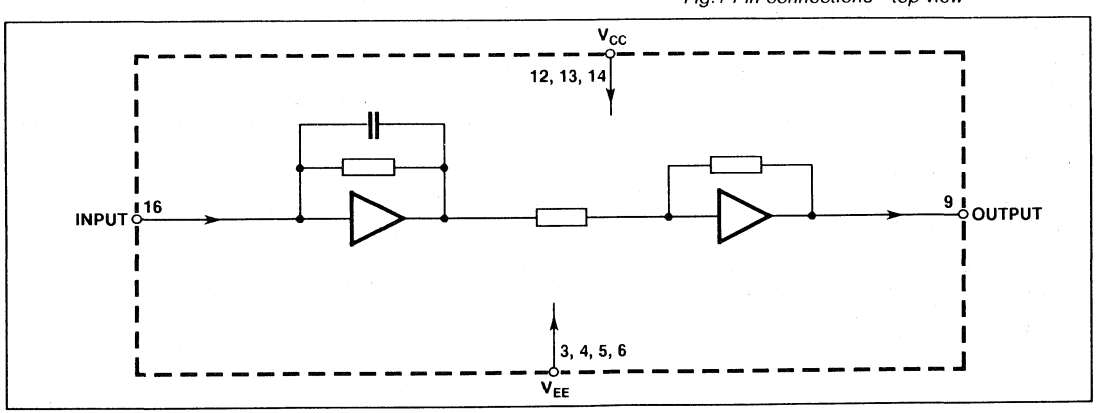


Fig.2 Functional block diagram SL9901 (LC pinout)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply voltage V_{CC} = +4.50V to +5.50V. T_{AMB} = -40°C to +85°C. Input current I_I = 0.3μA to 30μA peak (see note 1). Output load R_o = 200Ω minimum. Characteristic voltages are with respect to V_{EE}

Characteristic	Symbol	Value		Units	Conditions
		Min	Max		
Supply current	I_{CC}	12	20	mA	Outputs disabled
Input bias voltage	V_{IB}		1.65	V	T_{AMB} = 25°C
Output bias voltage	V_{OB}	0.55	1.05	V	T_{AMB} = 25°C
Transimpedance gain	G_T	20	40	kΩ	
Gain roll-off	G_R	6		dB/Oct	
3dB bandwidth	f_{3dB}	50		MHz	2.2pF on input See Fig. 3.

NOTE 1. The device is guaranteed to operate at up to 84μA (peak), but above 30μA (peak) the output may be be clipped

GUARANTEED CHARACTERISTICS

The following characteristics are guaranteed, but not tested, for the SL9901B at 25°C and over the full supply voltage range (+4.50V to +5.50V)

Characteristic	Symbol	Value		Units	Conditions
		Min	Max		
Input noise current (RMS)	I_N		4.0	pA/√Hz	C_{IN} = 2.2pF, f = 10MHz
			6.0	pA/√Hz	C_{IN} = 2.2pF, f = 50MHz
Input bias variation	dV_{IB}/dT		4.0	mV/°C	
Input current at clipping	I_{IC}	30		μA	Peak current
Output impedance	Z_O		100	Ω	
3dB Bandwidth	f_{3dB}	30		MHz	10pF on input See Fig. 3.

ADDITIONAL INFORMATION

The following characteristics are typical for the SL9901 at +25°C, but not tested.

Characteristic	Symbol	Value	Units	Conditions
Thermal resistance, chip-to-case	θ_{CC}	40	°C/W	
Thermal resistance, chip-to-ambient	θ_{CA}	120	°C/W	
Input impedance	Z_I	200	Ω	
Pin capacitance	C_P	1-5	pF	Pin to supplies

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+7V
Input voltage (device sourcing current)	0V
Input current (device sinking current)	1mA
Output voltage (device sinking current)	0V to V_{CC} - 2V
Output current (device sourcing current)	10mA
Storage temperature range	- 65°C to +150°C
Maximum junction temperature	+175°C

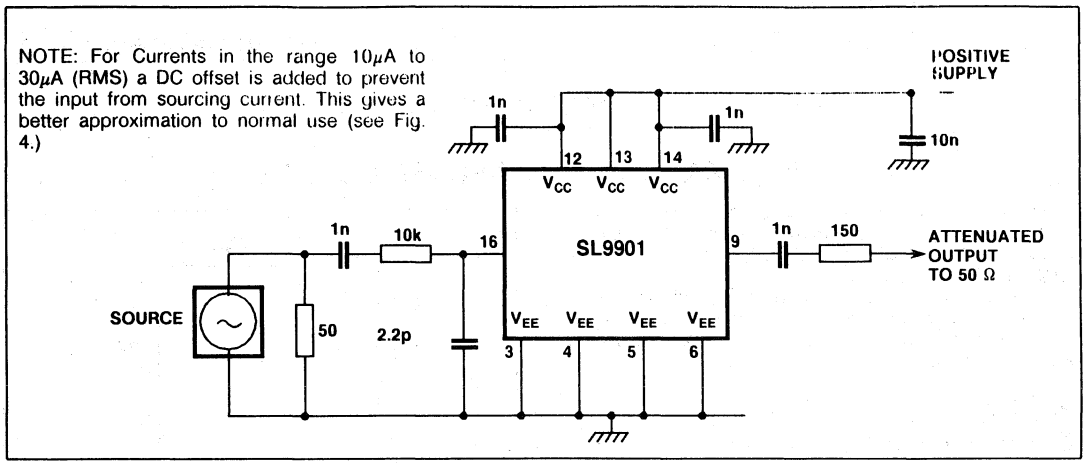


Fig. 3 Test circuit (LC package)

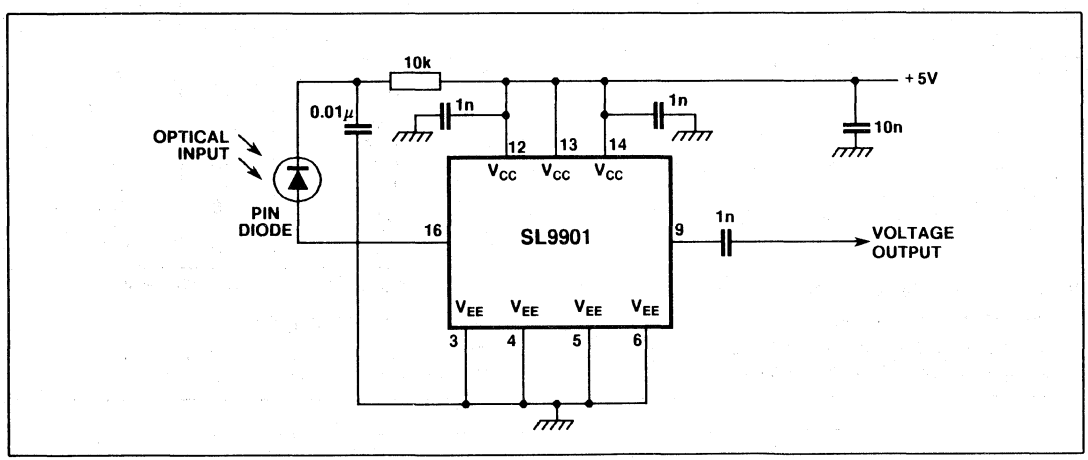


Fig. 4 Typical application circuit (LC package)

SP9921

50 MBIT MANCHESTER BIPHASE DECODER

The SP9921 is a bipolar monolithic silicon integrated circuit for clock and data recovery from a Manchester biphase-mark encoded signal. It operates from a single 5V supply and has ECL outputs.

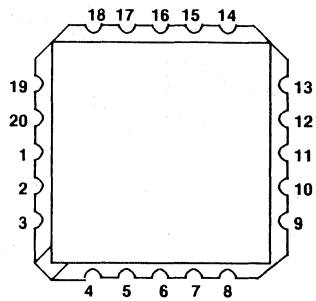
The device is also available as the SP9921AC, which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

FEATURES

- -40°C to +85°C Operating Temperature Range
- 50Mbit/s Clock and Data Rates.
- Single Supply Voltage
- Sensitive Differential Input
- ECL Outputs
- Input Signal Detection from Lock Detect Output
- No False Frequency Lock
- Correct Phase Lock on Random Data

APPLICATIONS

- High Speed Serial Data Communications
- Fibre Optic Data Links
- Local Area Network (LAN) Interface



Pin	Description	Pin	Description
1	RX –	11	RXD
2	NC	12	RXC
3	V_{EE}	13	RXO
4	V_{EE}	14	V_{CC}
5	RECF	15	V_{CC}
6	BD	16	NC
7	REFF	17	RCI
8	V_{EE}	18	V_{CC}
9	RCO	19	V_{CC}
10	PLO	20	RX+

Fig.1 Pin connections - top view

ORDERING INFORMATION

SP9921 B LC (Industrial - leadless chip carrier)
SP9921 AC LC (Military - leadless chip carrier, screened to MIL-STD-883C CLASS B)

ASSOCIATED PRODUCTS

SL9901 50MHz Transimpedance Amplifier
SP9960 50M-Bit Manchester Biphase Encoder

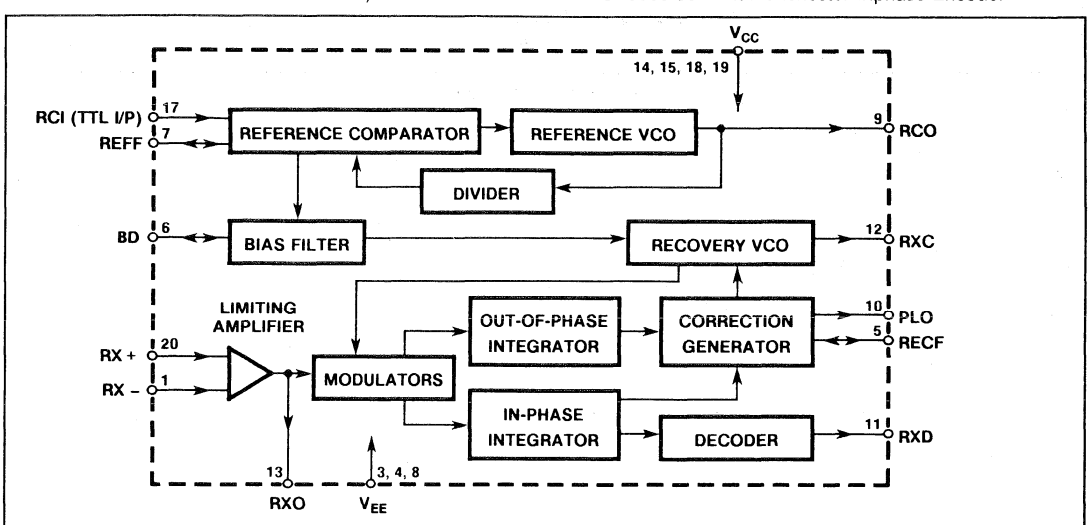


Fig.2 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Supply voltage V_{CC} = +4.50V to +5.50V, T_{AMB} = -40°C to +85°C
Programming input low voltage V_{ILP} = 0V to 0.4V. TTL input low voltage V_{ILT} = 0.8V max, TTL input high voltage V_{IHT} = 2.0V min. Differential receiver voltage V_{RD} = 10mV to 2.00V peak to peak. Bit Error Rate BER = 10^{-9} max.

Characteristic	Symbol	Value		Units	Conditions
		Min	Max		
Supply current	I_{CC}		200	mA	Output Unloaded
TTL input sink current	I_T		10	µA	T_{AMB} = +25°C
			30	µA	T_{AMB} = +25°C.
ECL output high voltage	V_{OH}	V_{CC}-0.96	V_{CC}-0.81	V	T_{AMB} = +25°C See note 1
		V_{CC}-0.89	V_{CC}-0.70	V	T_{AMB} = +85°C See note 1
		V_{CC}-1.06	V_{CC}-0.89	V	T_{AMB} = -40°C See note 1
ECL output low voltage	V_{OL}	V_{CC}-1.85	V_{CC}-1.62	V	T_{AMB} = +25°C See note 1
		V_{CC}-1.82	V_{CC}-1.61	V	T_{AMB} = +85°C See note 1
		V_{CC}-1.89	V_{CC}-1.67	V	T_{AMB} = -40°C See note 1
Receive offset voltage	V_{RO}		5.0	mV	
Minimum VCO frequency	fL		20	MHz	
Maximum VCO frequency	fH	50		MHz	

NOTE 1. $[V_{RX}+] - [V_{RX}-] > 100mV$ to ensure a good ECL output on RXO output load as per Fig. 4b.

GUARANTEED CHARACTERISTICS

The following characteristics are guaranteed, but not tested, for the SP9921 at +25°C and over the full supply voltage range (+4.50V to +5.50V). Voltages are with respect to the negative power supply (V_{EE})

Characteristic	Symbol	Value		Units	Conditions
		Min	Max		
ECL output source current	I_{SOURCE}	1.2		mA	See Fig. 5.
RCI frequency	f_R	3.9	10.1	MHz	
PCM clock high period	t_{RH}	20		ns	
PCM clock low period	t_{RL}	20		ns	
RCO rise or fall time	t_{RRF}		4	ns	R_L = 1kΩ, Fig. 4a.
REFF source current pulse	I_{RF+}	100	350	µA	
REFF sink current pulse	I_{RF-}	100	350	µA	
Minimum half period	t_{MIN}	$0.3t_B$		ns	See note 2
Minimum half period	t_{MAX}		$0.7t_B$	ns	See note 2
Operating voltage (REFC)	V_{OP}	V_R-0.33	V_R+0.33	V	See note 3
Free-running voltage (REFC)	V_{FR}	V_R-0.33	V_R+0.33	V	See note 3
Free-running frequency offset (wrt f_{RCO})	Δ_{FR}	-2.0	+2.0	%	Input grounded
Lock on range (wrt f_{RCC})	Δ_L	-2.0	+2.0	%	Circuit as Fig.11 With C5 = 0

GUARANTEED CHARACTERISTICS (continued)

Characteristic	Symbol	Value		Units	Conditions
		Min	Max		
RXC fall time	t_{RXF}		4	ns	R_L = 1kΩ, Fig. 4a.
RXC rise time	t_{RXR}		4	ns	R_L = 1kΩ, Fig. 4a.
Output delay	t_{OD}		5	ns	R_L = 1kΩ, Fig. 4a.

NOTES
2. t_B typically = $1/f_{RCO}$ secs
3. V_R typically = V_{CC}-1 volts

ADDITIONAL INFORMATION

The following characteristics are typical for the SP9921B at +25°C, but not tested.

Characteristic	Symbol	Value	Units	Conditions
Thermal resistance chip-to-case	θ_{CC}	28	°C/W	
Thermal resistance chip-to-ambient	θ_{CA}	73	°C/W	
Pin capacitance	C_P	3	pF	Pin to supplies
ECL output sink current	I_{SINK}	2	mA	See Fig. 5
Receive bias voltage	V_{RB}	$V_{CC}/2$	V	
Receive input impedance	Z_{RI}	1000	Ω	Differential input
RCI rise time	t_{RR}	20	ns	
RCI fall time	t_{RF}	20	ns	
fH temperature coefficient	ΔfH	-0.2	MHz/°C	
RCO frequency	f_{RCO}	18	MHz	V_{REFF} = 2.5V
		46	MHz	V_{REFF} = 3.0V
		54	MHz	V_{REFF} = 3.5V
Reference loop gain	G_{REF}	40	MHz/V	f_{RCO} = 20MHz
		100	MHz/V	f_{RCO} = 30MHz
		55	MHz/V	f_{RCO} = 40MHz
		20	MHz/V	f_{RCO} = 50MHz
Frequency - voltage ratio	OCF/V	8.5	MHz/V	f_{RCO} = 50MHz
		9.5	MHz/V	f_{RCO} = 40MHz
		11.0	MHz/V	f_{RCO} = 30MHz
		6.5	MHz/V	f_{RCO} = 20MHz

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V
Input voltage	- 0.3V to V_{CC} + 0.3V
Output voltage	0V to V_{CC}
Storage temperature range	- 55°C to + 150°C
Maximum junction temperature	+ 175°C

PIN DESCRIPTIONS		
Symbol	**Pin no**	**Description**
REFF	7	**Reference Filter (Current Output/Voltage Input)**. A series RC network should be connected between this pin and ground to provide the filtering for the control of the reference VCO.
V_{EE}	8	**Negative Power Supply**
RCO	9	**Reference Clock Out (ECL Output)**. This pin should output a clock which is frequency-locked to the reference clock input (RCI pin) but which is 5 times its frequency.
PLO	10	**Phase Lock Out (ECL Output)**. This pin goes low for any bits where the output of the in-phase integrator (data) fails to exceed the output of the out-of-phase integrator (error) by a set margin.
RXD	11	**Received Data** (ecl output). This pin outputs the decode received data.
RXC	12	**Received Clock (ECL Output)**. This pin outputs the recovered clock.
RXO	13	**Receive Out (ECL Output)**. This pin outputs the undecoded received data.
V_{CC}	14, 15	**Positive Power Supply**
NC	16, 2	**No Connection** This pin should be left unconnected for normal operation.
RCI	17	**Receive Clock In (TTL Input)**. This is the input for the reference clock which sets the free-running frequency for the recovery VCO. Its frequency should be close to one fifth of the received data rate.
V_{CC}	18, 19	**Positive Power Supply**
RX+ **RX–**	20 1	**Receive Plus and Minus (Analog Voltage Inputs)**. These are the differential inputs to the limiting receive amplifier. They are self-biasing and would normally be capacitively coupled. For a single-ended input the unused pin should be capacitively coupled to ground.
V_{EE}	3, 4	**Negative Power Supply**
RECF	5	**Recovery Filter (Current Output/Voltage Input)**. A series RC network should be connected between this pin and ground to provide the filtering for the control of he recovery VCO.
BD	6	**Bias Decoupling (Decoupling Node)**. A capacitor should be connected between this pin and ground to eliminate noise on the bias voltage generated by the reference PLL and which sets the free-running frequency of the recovery VCO.

FUNCTIONAL DESCRIPTION

Fig. 2 shows the simplified block diagram of the device. It locks onto incoming data, recovers the clock and decodes the data making use of a reference clock input at one fifth of the data rate.

Receive Path

Data is received at the differential input pins (RX+/-) of the limiting amplifier which outputs the digital received signal for monitoring at the amplifier output pin (RXO). This signal is fed into a modified Costas loop which outputs the recovered clock (RXC pin) and the decoded data (RXD pin).

Fig. 3 shows how the input signal is decoded. The Manchester biphase-mark code uses a transition at the centre of the bit to indicate a one and the absence of a transition to indicate a zero. In addition there is always a transition at the end of the bit.

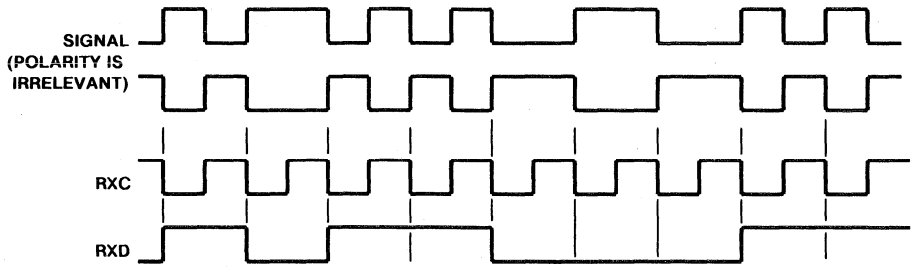
Phase-Locking and Signal Recovery

The SP9921 can be used in systems operating over a wide range of data rates without false frequency lock. This is achieved using a reference VCO and a recovery VCO.

The reference VCO is phase-locked to the reference clock input (RCI pin). This generates an internal clock at 5 times the frequency of the reference clock input. The output of this VCO is output for monitoring on the reference clock output (RCO pin). Filtering of the bias control signal to the VCO is performed at the reference filter pin (REFF).

The bias control signal for the reference VCO is filtered at the bias decoupling pin (BD) and used to set the free-running frequency of the recovery VCO. The recovery VCO drivers the receive clock (RXC pin) and the modulators which in turn drive the integrators. The integrators analyse the components of the signal which are in phase and 90° out of phase and so obtain the recovered data and the correction signal for the modified Costas loop. The correction signal is filtered at the recovery filter pin (RECF).

The modified Costas loop also pulls the phase-lock output pin (PLO) low for any bits when the output of the in-phase integrator (data) does not exceed the output of the out-of-phase integrator (error) by a set margin. This can occur when there is a loss of data, if there is too much noise on the link (even if no data is corrupted) or if the Costas loop has difficulty locking.



NOTE: There is a delay of 3 clock cycles between the input signal and the decoded data output.

Fig. 3 Biphase-Mark Decoding

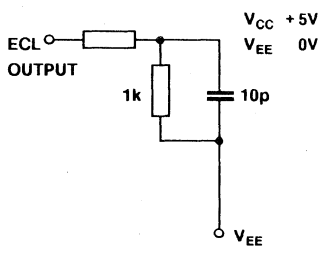


Fig. 4a

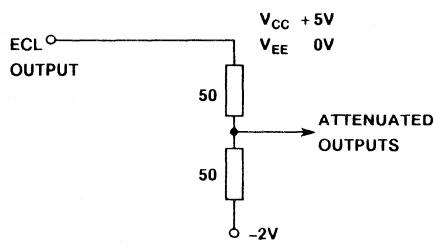


Fig. 4b

Fig. 4 ECL Output test loading

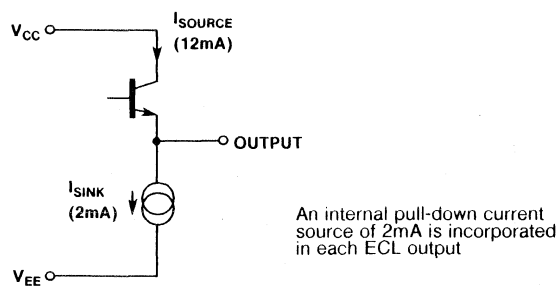


Fig. 5 ECL output circuitry

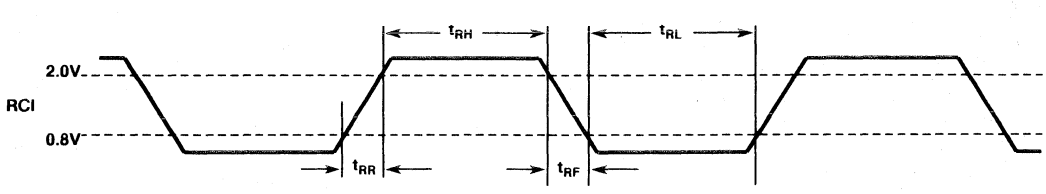


Fig. 6 Timing - reference clock in

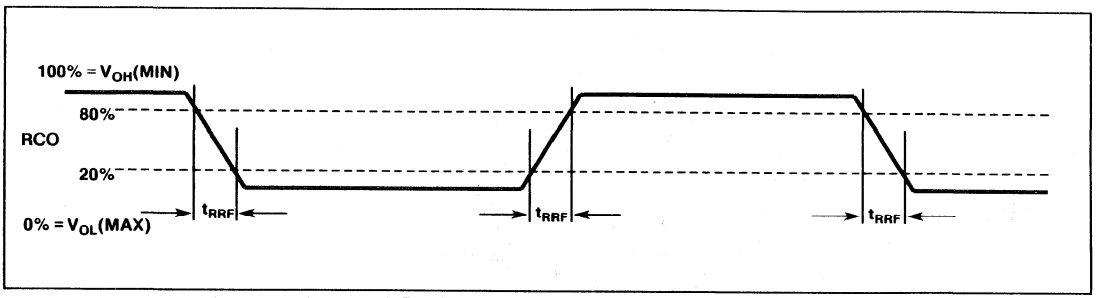


Fig. 7 Timing - reference clock out

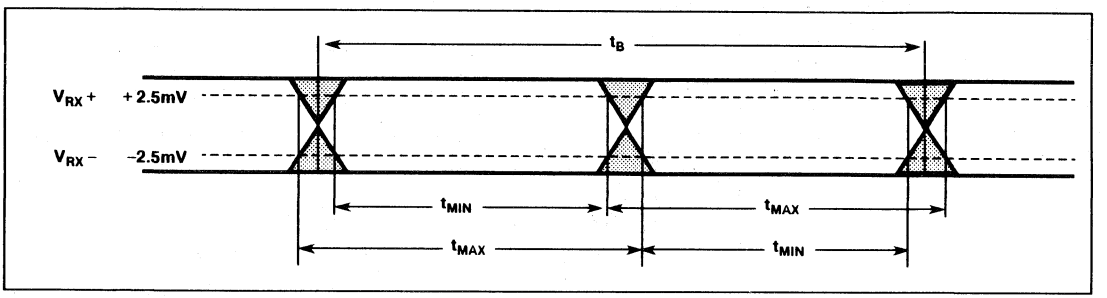


Fig. 8 Timing - receive data

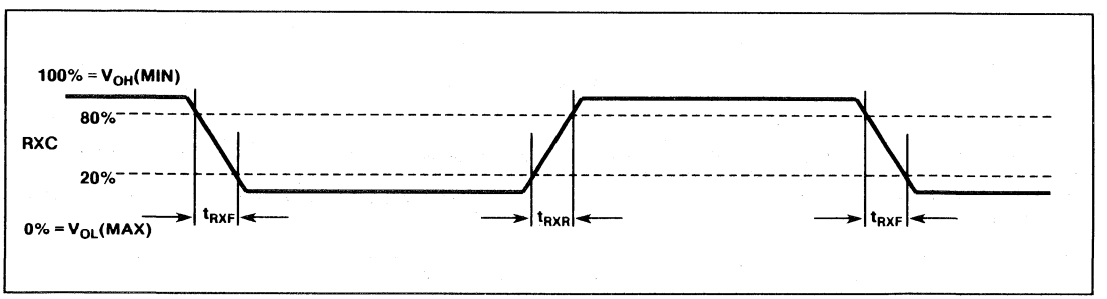


Fig. 9 Timing receive clock

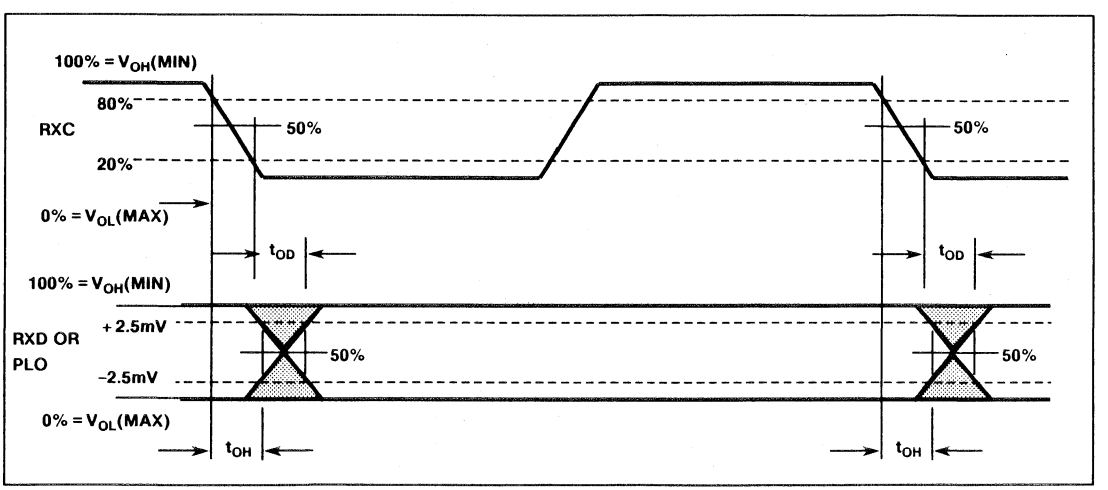
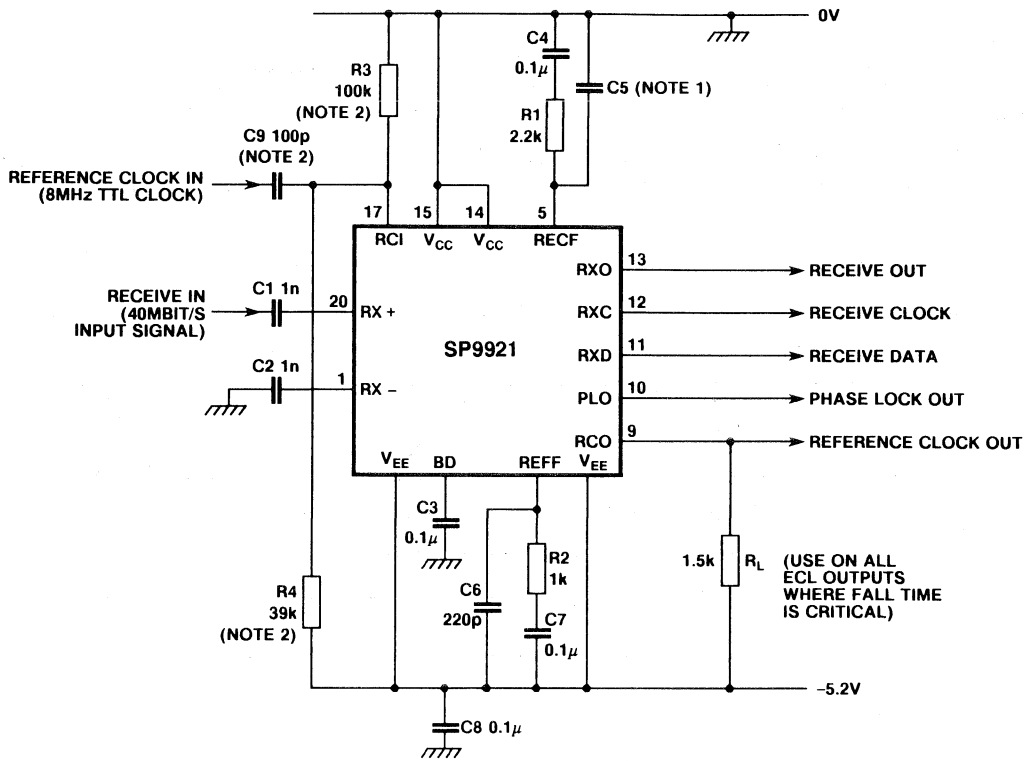


Fig. 10 Timing - receive data and phase lock out



1. C5 should be zero for most applications to maximise capture range, in applications where jitter is of paramount importance then a small value up to 47pF maybe used.
2. C9, R3 and R4 may be removed and the TTL reference clock connected directly to pin 17, provided that the TTL signal is referenced to V_{EE}

Fig.11. Typical application circuit

GEC PLESSEY
SEMICONDUCTORS

PRELIMINARY INFORMATION
DS2122-1.0

SP9960

50M-BIT MANCHESTER BIPHASE-MARK ENCODER AND LED DRIVER

The SP9960 is a Manchester biphase-mark encoder and LED driver, designed for use in fibre-optic links at up to 50Mbits/s. It encodes TTL or ECL data and outputs the result as a current at either the large or small LED driver output. The LED driver and the current output are selected.

The device is also available as the SP9960AC, which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883 Class B. Data is available separately.

FEATURES

- -40°C to +85°C Operating Temperature Range
- 50Mbit/s Operation Clock and Data Rates
- TTL or ECL Inputs
- Choice of LED drivers - Large or Small
- Choice of LED Drive Currents
- LED Driver Enable Voltage
- Single Supply Voltage

APPLICATIONS

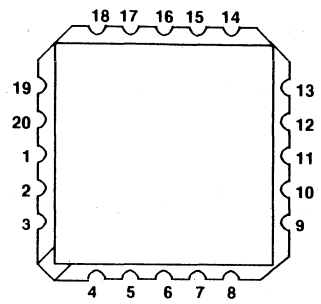
- Fibre Optic Data Link
- Local area Network (LAN) Interface
- Coaxial/Twisted Pair Devices

ORDERING INFORMATION

SP9960 B LC (Industrial - leadless chip carrier)
SP9960 AC LC (Military - leadless chip carrier, screened to MIL-STD-883C CLASS B)

ASSOCIATED PRODUCTS

SL9901 50MHz Transimpedance Amplifier
SP9921 50M-Bit Manchester Biphase Decoder



LC20

Pin	Function	Pin	Function	Pin	Function
1	NC	8	EDI	15	LD
2	V_{EE}	9	NC	16	NC
3	V_{EE}:10	10	V_{CC}	17	V_{EE}:80
4	TDI	11	DL	18	V_{EE}:45
5	TCI	12	DL	19	V_{EE}:LD
6	NC	13	SD	20	ODE
7	ECI	14	NC		

Fig.1 Pin connections - Top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+7V
Input voltage	-3.0V to +0.3V
Storage temperature range	-65°C to +175°C
Maximum junction temperature	+175°C

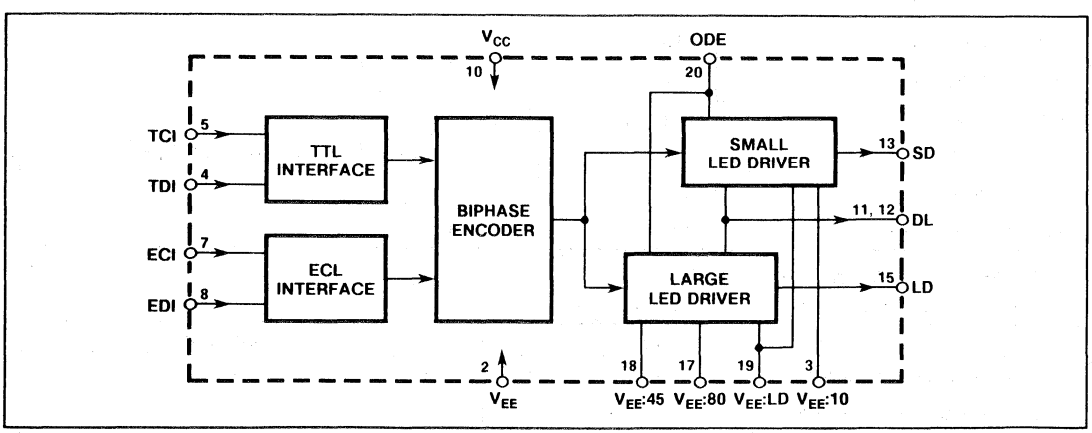


Fig.2 Functional block diagram

ELECTRICAL CHARACTERISTICS (Voltages are with respect to the negative power supply (V_{EE})

Test conditions (unless otherwise stated)

Supply voltage V_{CC} = +4.5V to +5.50V, T_{AMB} = -40°C to +85°C (see note 1),
Programming input low voltage V_{ODEL} = 0V to 0.4V; Programming input high voltage V_{ODEH} = 2V to V_{CC}; TTL input low voltage V_{ILT} = 0.84V Max; TTL input high voltage V_{ILT} = 2.0V min; ECL input low voltage $V_{ILE} = V_{CC}$ -1.65V max; ECL input high voltage $V_{IHE} = V_{CC}$ -0.96V min. (see note 2).

Parameter	Symbol	Value		Units	Conditions
		Min	Max		
Supply current	I_{CC}		70	mA	Output disabled
TTL input current	I_T		130	µA	$V_{IHT} = V_{CC}$
ECL input current	I_E		300	µA	$V_{IHE} = V_{CC}$
Small driver ON current (sink) (note 3)	I_{SD}	12 20	18 30	mA mA	$1V < (V_{EE}:10) < V_{CC}$, default. $V_{EE}:10 = V_{EE}$
Large driver ON current (sink) (note 3)	I_{LD}	35 72 102 140	55 108 148 200	mA mA mA mA	$1V < (V_{EE}:45/80) < V_{CC}$, default. $V_{EE}:45 = V_{EE}$ $V_{EE}:80 = V_{EE}$ $V_{EE}:45 = V_{EE}$, $V_{EE}:80 = V_{EE}$
Operating clock frequency	f_C	50		MHz	

NOTES

1 The maximum temperature depends on the selected LED drive current. The limits are found by derating the limit of the chip temperature (given in Absolute Maximum Ratings) by the temperature difference due to the power dissipation and the thermal resistance to case or ambient (given in the Additional Information table).

2. T_{AMB} = +25C.

3. The maximum power dissipation depends on the selected output drive current. It is always less than the product of the supply voltage and the sum of maximum drive current (either I_{SD} or I_{LD}) and the maximum current with driver disabled (I_{CC})

GUARANTEED CHARACTERISTICS

The following characteristics are guaranteed, but not tested, for the SP9960B at +25°C and over the full supply voltage range (+4.50V to +5.50V); refer to Figs. 5 to 7.

Parameter	Symbol	Value		Units	Conditions
		Min	Max		
Programming input (ODE) current low	I_{ODEL}		2.0	mA	V_{ODE} = 0V
Driver OFF leakage (sink)	I_L		100	µA	$0V < V_{ODE} < 0.4V$
Clock high period	t_{CH}	5		ns	
Clock low period	t_{CL}	5		ns	
Input data setup time	t_{IS}	5		ns	
Input data hold time	t_{IH}	0		ns	
Output data hold time	t_{OH}	0		ns	
Output data delay	t_{OD}		30	ns	
Output rise & fall time	t_{ORF}		2	ns	I_{LED} = 80mA, 10Ω to V_{CC}
1st half cycle period	$t1_{CP}$	t_{CL-2}		ns	
2nd half cycle period	$t2_{CP}$	t_{CL-2}		ns	

ADDITIONAL INFORMATION

The following parameters are typical for the SP9960 at +25°C but not tested.

Characteristic	Symbol	Value	Units	Conditions
Thermal resistance, chip-to-case	θ_{CC}	28	°C/W	
Thermal resistance, chip-to-ambient	θ_{CA}	73	°C/W	
Pin capacitance	C_P	3	pF	Pin to supplies

FUNCTIONAL DESCRIPTION

Fig. 2 shows the simplified block diagram of the device. Data arriving at a data input (TDI or EDI pin) is sampled by the positive edge of the appropriate clock (TCI or ECI pin), encoded into a biphase-mark signal, and output as a current at the chosen LED driver (SD or LD pin).

If TTL inputs are to be used (TDI and TCI pins) then the ECL inputs (EDI and ECI) should be left unconnected and vice versa.

Biphase Mark Encoding

Fig. 3 shows how the biphase-mark encoding scheme works. The input data is sampled by the positive edge of the clock. If the data is high (logic '1') then the driver switches to its opposite state i.e., OFF if it was previously ON, or ON if it was previously OFF. If the data is low (logic '0') then the driver does not switch to its opposite state on the positive clock edge.

Regardless of the sampled input data, the driver always switches to its opposite state on the negative edges of the clock.

This form of encoding ensures a high number of transitions in the signal which simplifies the task of clock recovery at a remote detector. Since the data is encoded in terms of transitions, rather than as absolute levels, the signal can be given a net inversion without corrupting the information carried.

LED Drivers

There are two LED driver outputs, the small driver (SD, pin 13) and the large driver (LD, pin 15). The driver used is chosen by V_{EE}:LD (pin 19) which should be tied to V_{EE} (pin 2) to select the large driver and left unconnected to select the small driver., as shown in Table 1.

Typical LED output currents for the small driver are 15mA or 25mA and for the large driver 45mA, 90mA, 125mA or 170mA, determined by the supply connections to the V_{EE}:10, V_{EE}:45 and V_{EE}:80 pins, as shown in Table 1.

When the LED driver is OFF then current is switched to the dummy load pins (DL) which are normally connected to the positive supply. This reduces the ringing which could otherwise occur on switching relatively large currents. The drivers are disabled by pulling the ODE pin low. They are enabled if the ODE pin is left unconnected.

LED output selectors (ODE = O/C)				LED current (mA typ)	
V_{EE}:LD (19)	V_{EE}:10 (3)	V_{EE}:45 (18)	V_{EE}:80 (17)	SD (13)	LD (15)
O/C	O/C	X	X	15	–
O/C	V_{EE}	X	X	25	–
V_{EE}	X	O/C	O/C	–	45
V_{EE}	X	V_{EE}	O/C	–	90
V_{EE}	X	O/C	V_{EE}	–	125
V_{EE}	X	V_{EE}	V_{EE}	–	170

Table 1

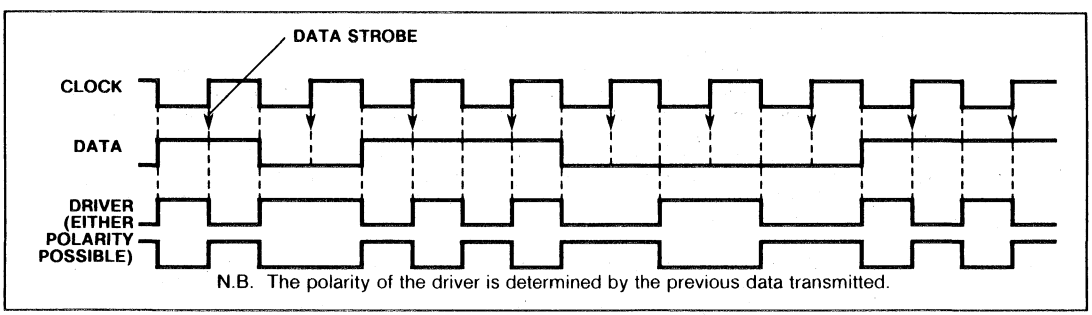


Fig. 3 Encoding alignment

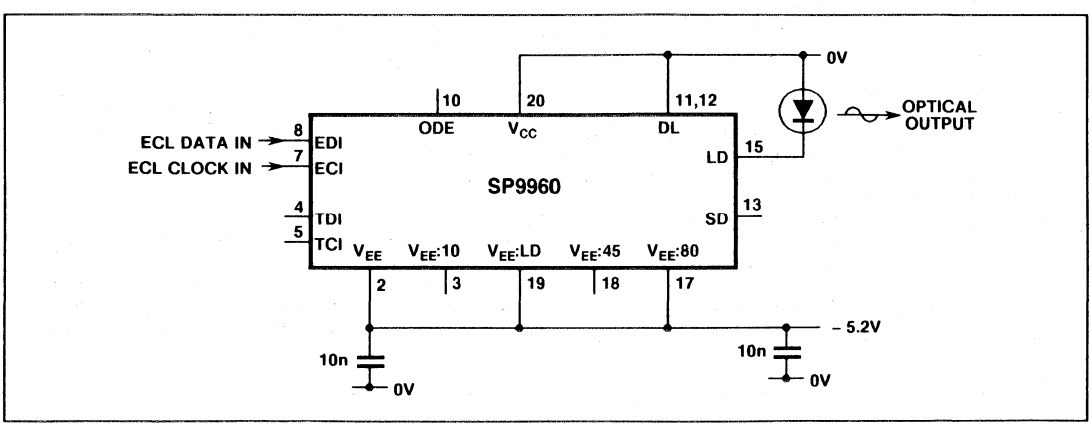


Fig. 4 Typical ECL application circuit - large driver at 125 mA (typical) selected

N.B. For TTL applications the TTL inputs TDI and TCI should be used, VCC should be + 5V and V_{EE} should be 0V.

PIN DESCRIPTIONS

Symbol	LCC Pin No	Pin Name and Description
V_{EE}	2	**Negative Supply (Power Input).** This pin is normally tied to 0V for TTL operation or to -5.2 V for ECL operation.
V_{EE}: 10	3	**10mA Negative Supply (Power Input).** This pin should be tied to the negative supply (VEE) to increase the current sink at the small current LED output driver (SD pin) by 10mA if the small driver is selected. It should be left unconnected otherwise.
TDI	4	**TTL Data Input (TTL Input with Internal Pull-Down).** TTL data is strobed in at this pin by the positive edges of the TTL Clock input (TCI pin). This pin should be left unconnected if the TTL inputs are not to be used. See notes given in this table on V_{CC} and V_{EE}.
TCI	5	**TTL Clock Input (TTL Input with Internal Pull-Down).** The rising edges of this clock is used to strobe the TTL data input (TTI pin). This pin should be left unconnected if the TTL inputs are not to be used. See notes on V_{CC} and V_{EE}.
ECI	7	**ECL Clock Input (ECL Input with Internal Pull-down).** The rising edge of this clock is used to strrobe the ECL data input (EDI pin). This pin should be left unconnected if the ECL inputs are not to be used. See notes on V_{CC} and V_{EE}.
EDI	8	**ECL Data Input (ECL Input with Internal Pull-down).** ECL data is strobed in at this pin by the positive edges of the EC clock input (ECL pin). This should be left unconnected if the ECL inputs are not to be used. See notes given in this table on V_{CC} and V_{EE}.
V_{CC}	10	**Positive Supply (Power Input).** This pin is normally tied to 5V for TTL operation or to 0 V for ECL operation.
DL	11,12	**Dummy Load (Current Sink Output).** Current is switched between these pins and the selected LED drivers (SD or LD) to reduce ringing. They should be connected to the positive supply (V_{CC}).
SD	13	**Small Driver (Current Sink Output).** This is the small current LED output driver. Data supplied at the clock and data pins is encoded and output as a current at this pin if the large driver negative supply pin (V_{EE}:LD) is left unconnected.
LD	15	**Large Driver (Current Sink Output).** This is the large current LED output driver. Data supplied at the clock and data pins is encoded and output as a current at this pin if the latge driver negative supply pin (V_{EE}:LD) is tied to the negative supply (V_{EE}).
V_{EE}: 80	17	**80mA Negative Supply (Power Input).** This pin may be used in conjunction with the V_{EE}:45 pin. It should be tied to the negative supply (V_{EE}) to increase the current sink at the large current LED output driver (LD pin) by 80mA (typically) if the large driver is selected. It should be left unconnected otherwise.
V_{EE}: 45	18	**45mA Negative Supply (Power Input).** This pin may be used in conjunction with the V_{EE}:80 pin. It should be tied to the negative supply (V_{EE}) to increase the current sink at the large current LED output driver (LD pin) by 45mA (typically) if the large driver is selected. It should be left unconnected otherwise.
V_{EE}: LD	19	**Large Driver Negative Supply (Power Input).** This pin should be tied to the negative supply (V_{EE}) if the large current LED output driver (LD pin) is to be used. It should be left unconnected if the small current LED output driver (SD pin) is to be used.
ODE	20	**Output Driver Enable (Programming Input with Internal Pull-up).** This pin should be left unconnected for normal operation. If it is low then the LED output driver is disabled.

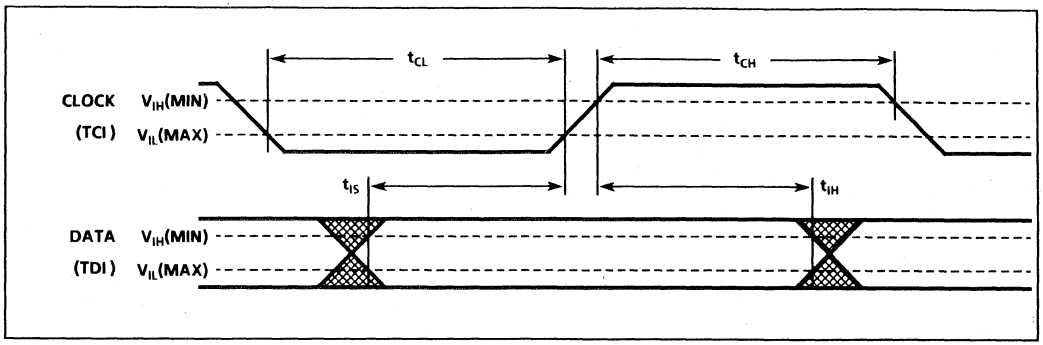


Fig. 5 Digital Switching Characteristics - TTL Input

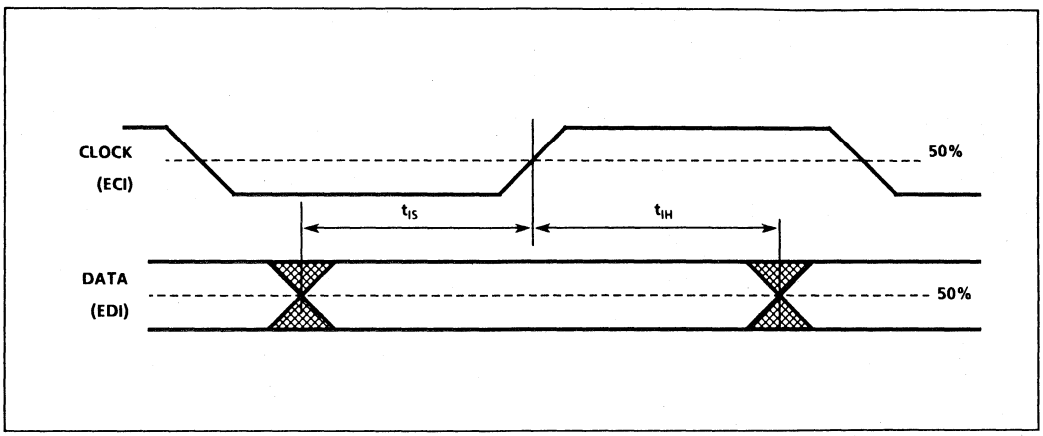


Fig. 6 Digital Switching Characteristics - ECL Input

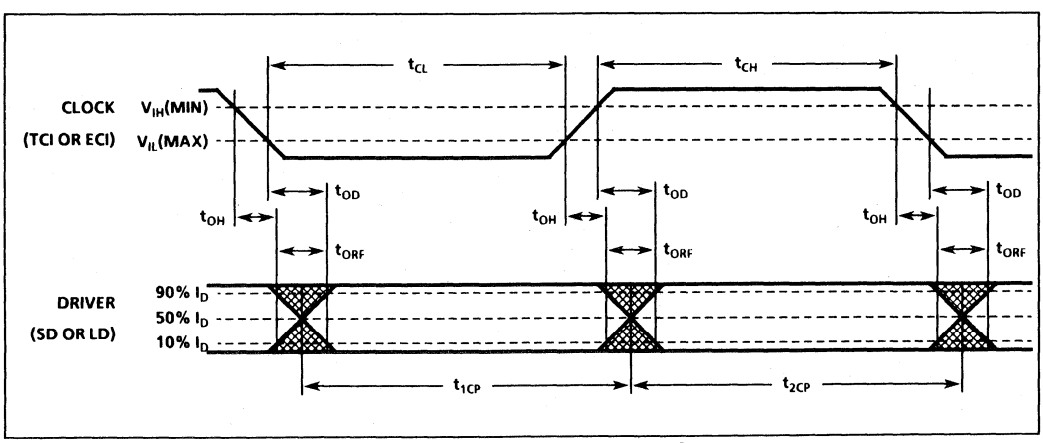


Fig. 7 Digital Switching Characteristics - Output

Section 6
Other Telecoms Circuits

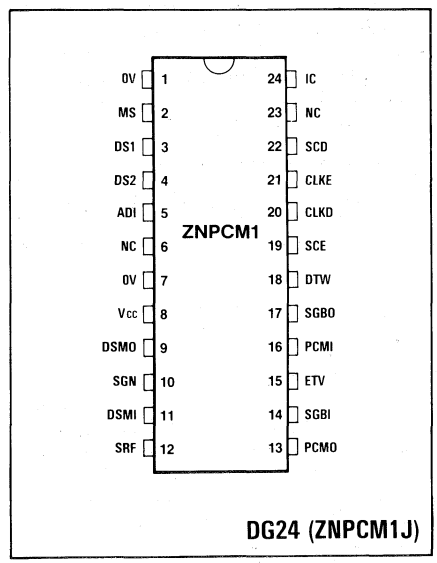
DS3135-1.0

ZNPCM1

SINGLE CHANNEL CODEC

FEATURES

- Converts a Delta-Sigma Modulated Digital Pulse Stream into Compressed 'A'-Law PCM and Vice-Versa.
- Enables Realisation of a Single Channel Codec Circuit with Minimum Component Usage.
- Pin Selectable Input/Output Interface Providing either Single Channel Operation at 64Kbit/s or up to 2048kbit/s for Multi-Channel Operation (2048kHz External Clock).
- Encoder and Decoder can be Clocked Asynchronously (Useful for PCM Multiplex Applications).
- Optional Alternate Digit Inversion.
- Pin and Function Compatible with AY-3-9900.
- Fully TTL Compatible.
- Single 5V Supply.



Pin connections - top view

DESCRIPTION

The ZNPCM1 integrated circuit is the result of a joint development programme with British Telecom. Designed for use in single channel Codec systems, the device accepts a delta-sigma modulated pulse stream at 2048kbit/s (2048kHz external clock) and converts it into 8K sample compressed 'A'-law PCM. In the decode direction, the device performs the reverse function.

A flexible serial PCM input/ouput interface is provided, allowing operation in a single channel mode at 64Kbit/s or at up to 2048kbit/s (2048kHz external clock). for a multi-channel burst format. Digit delay control is provided to compensate for transmission delays.

Optional alternate digit inversion is provided and the encoder and decoder can be clocked asynchronously if required for use in PCM multiplex applications. Designed for use with a 2048kHz system clock, when operated with the required delta-sigma modulator and demodulator, the device performance complies with BT specification RC5549B and CCITT recommendations G711/G712 (1972).

The ZNPCM1 is guaranteed to operate up to 2048kHz and will typically operate up to 4MHz. Operation is from a single 5V power supply, with a typical power dissipation of 400mW.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	+7 Volts
Input Voltage, V_{IN}	+5.5 Volts
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
High-level Output Current, I_{OH}	—	—	−400	μA
Low-level Output Current, I_{OL}	—	—	4	mA
Operating Temperature Range, T_{amb}	0	—	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating temperature range).

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage		2.5	—	—	V
V_{IL}	Low level input voltage		—	—	0.8	V
V_{OH}	High level output voltage	V_{CC} = Min., I_{OH} = Max.	2.4	3.5	—	V
V_{OL}	Low level output voltage	V_{CC} = Min., I_{OL} = Max.	—	—	0.4	V
I_{IH}	High level input current	V_{CC} = Max., V_{IH} = Min.	—	0.2	0.4	mA
I_{IL}	Low level input current	V_{CC} = Max., V_{IL} = Max.	—	−1	−10	μA
I_{CC}	Supply current	V_{CC} = Max.	—	80	110	mA
t_{vw}	Encoder timing vector pulse width		—	488	—	ns
t_{vv}	Encoding timing vector pulse width with edge variation		—	—	100	ns
t_{ww}	Decoder timing waveform pulse width		10	15.6	—	μs
f_{max}	Operating frequency		2.048	4	—	MHz
t_r & t_f	Rise and fall times	0.4V to 3V Transition	5	—	40	ns
t_{pw}	Pulse width	Between 1.5V levels	200	—	—	ns
C_I	Input capacitance		—	—	10	pF

PIN CONFIGURATIONS

Pin	Notation	Comments
1	0V	
2	MS	MODE SELECT (Note 1) Logic 0 = External pcm I/O interface timing Logic 1 = Internal pcm I/O interface timing
3	DS1	DECODER SELECT 1 and 2 (Note 2)
4	DS2	A two bit binary word selects required digit delay between encoder and decoder. DS1 DS2 Digit Delay 0 0 0 0 1 1 1 0 2 1 1 3
5	ADI	ALTERNATE DIGIT INVERSION Logic 0 = No. ADI Logic 1 = ADI
6	N.C.	NO CONNECTION
7	0V	
8	V_{CC}	
9	DSMO	DELTA-SIGMA MODULATED OUTPUT SIGNAL
10	SGN	SIGN BIT OUTPUT Sign bit from the encoder, used to operate on the delta-sigma modulator to reduce d.c. offset effects.
11	DSMI	DELTA-SIGMA MODULATED INPUT
12	SRF	SPECTRAL REDISTRIBUTION FUNCTION Output signal used to operate on the delta-sigma modulator to reduce low frequency quantisation noise.
13	PCMO	PCM OUTPUT
14	SGBI	SIGNALLING BIT INPUT Facility for adding signalling bit(s) to the output pcm stream.
15	ETV	ENCODER TIMING VECTOR A pulse defining the beginning of each frame used to maintain encoder timing.
16	PCMI	PCM INPUT
17	SGBO	SIGNALLING BIT OUTPUT Serial output for extracting signalling bit(s) from the incoming pcm stream.

PIN CONFIGURATIONS *(continued)*

Pin	Notation	Comments
18	DTW	DECODER TIMING WAVEFORM A pulse used to indicate to the decoder when the input pcm stream is in the input register (required only when external shift clocks are used).
19	SCE	ENCODER SHIFT CLOCK Used to control the output of serial pcm data from the encoder (when MS is low).
20	CLKD	DECODER MAIN CLOCK
21	CLKE	ENCODER MAIN CLOCK
22	SCD	DECODER SHIFT CLOCK Used to control the input of the serial pcm data to the decoder (when MS is low).
23	N.C.	NO CONNECTION
24	I.C.	INTERNAL CONNECTION Make no external connection to this pin.

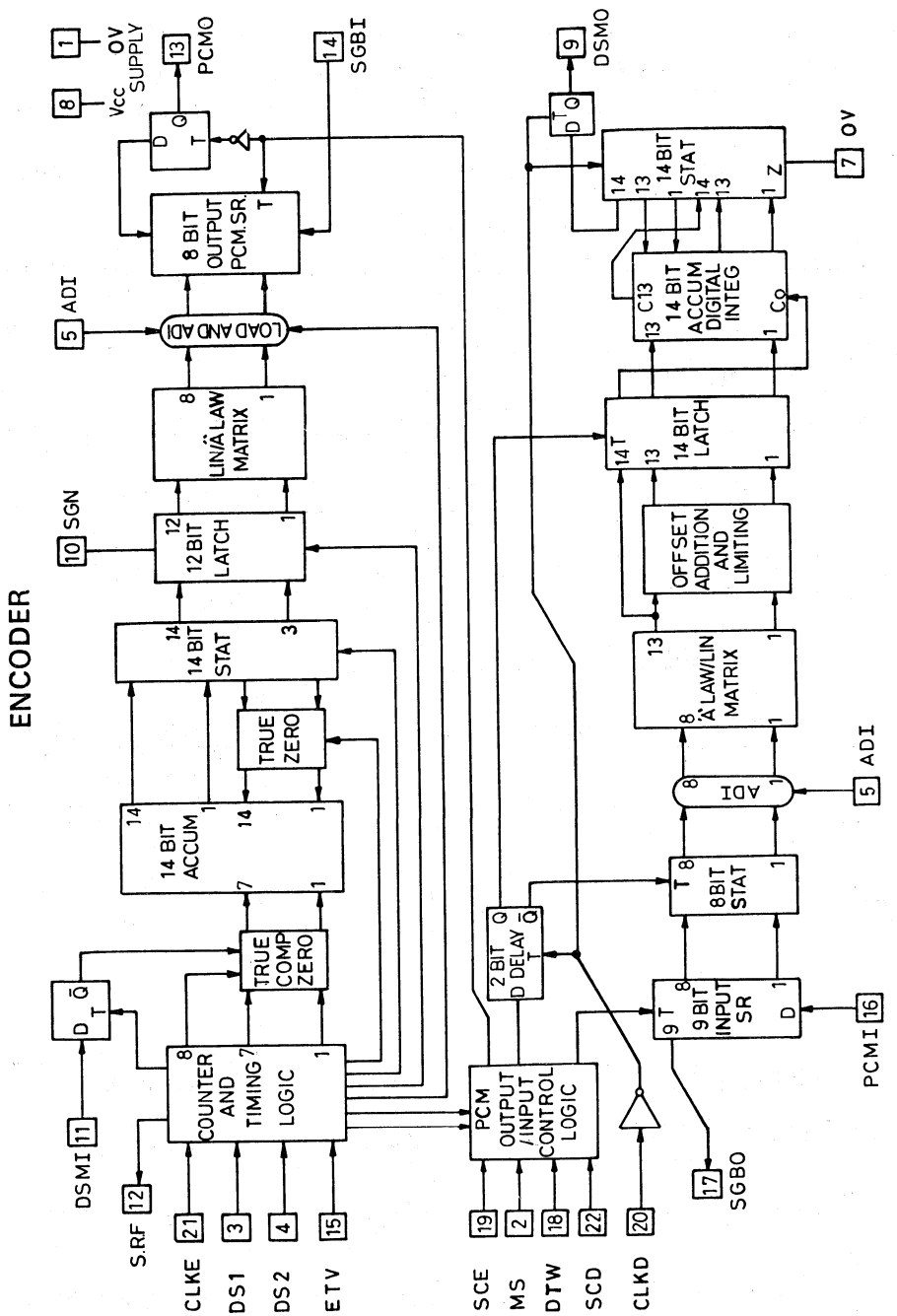
Notes:

1. With MS low (logic 0) serial PCM transmission is under the control of an externally generated shift clock SCE which can vary from 64 kHz to 2,048 kHz. The timing of this input function allows the insertion of a number of signalling bits into the PCM stream via the SGB1 input. In the high (logic 1) state the 8 bit PCM codeword will be transmitted at a rate of 64K bit/sec and each codeword will occupy the full 125 μs frame period with the leading edge of the first bit occurring at a time defined by the ETV pulse.

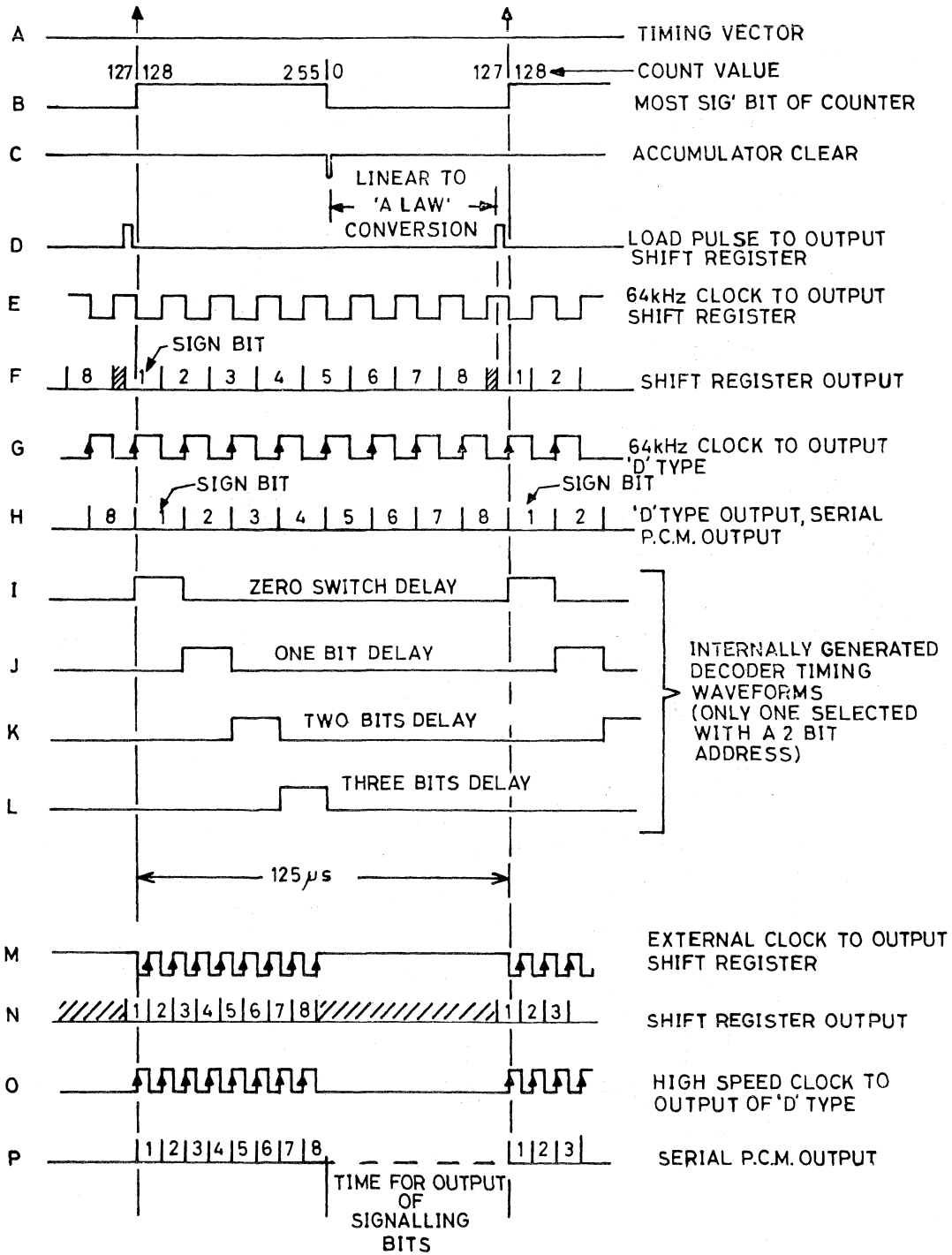
2. Delays through the transmission network, normally under the control of transmission switches, may cause the decoder input pulse stream to be delayed in time by a number of digits from the original transmitted pulse. To compensate for this delay two control inputs, DS1 and DS2, are provided. Consequently when MS is in the high state discrete digit delays of 0 to 3 periods may be selected resulting in a controlled shift of decoder timing in order to re-align Bit 1 in its correct position in the input register.

   When using an externally generated clock (i.e. MS in low state) an input shift clock (SCD) and timing waveform (DTW) are required to ensure that Bit 1 of the input codeword occupies its correct position in the input shift register.

FUNCTIONAL DIAGRAM

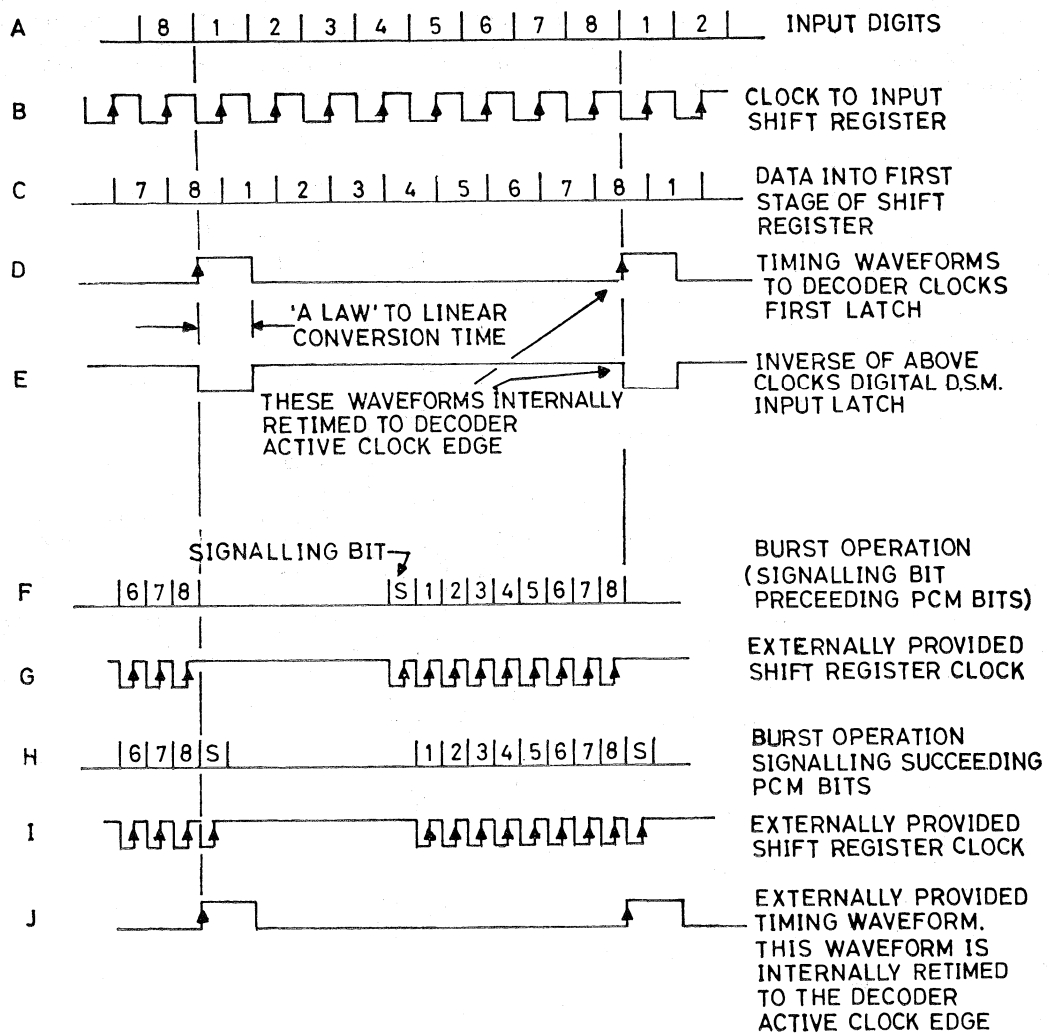


TIMING DIAGRAM
ENCODER



TIMING DIAGRAM

DECODER



APPLICATIONS INFORMATION

(a) A Single Channel Codec

Fig. 1 shows a block diagram of a single channel Codec using the ZNPCM1. The circuit accepts a band limited analogue input signal (300 – 3,400 kHz) and converts it to one bit/sample delta sigma code format at a high sampling rate. The dsm bit stream is then converted by the ZNPCM1 into 8-bit compressed pulse code modulation (pcm) code words at the standard rate of 8K samples/sec, which is then converted into serial format for transmission serially at 64K bit/sec. External timing signals can be used to increase the transmission bit rate to 2,048K bit/sec. to allow for multiplexing in a burst format (see application b).

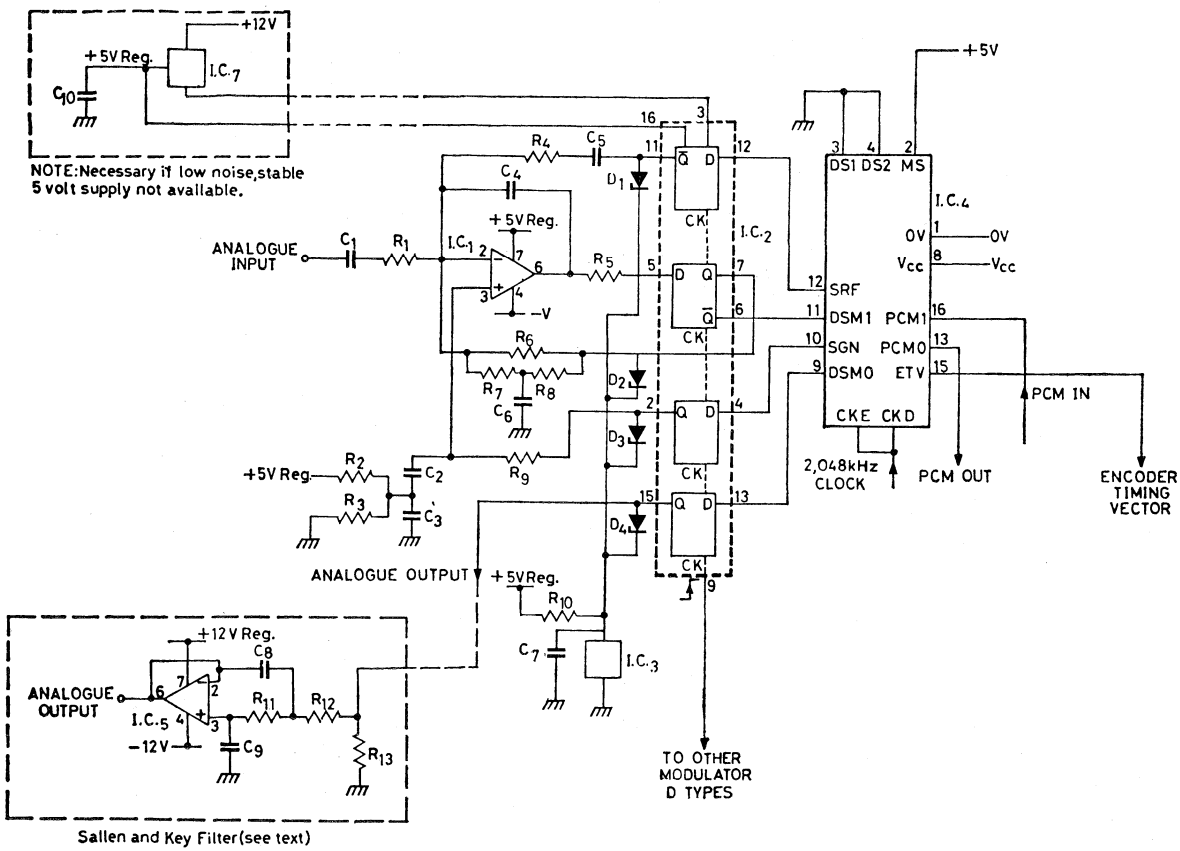


Fig. 1.

The pcm input interface will accept either a 64K bit/sec. bit stream or, by the application of external timing signals, a bit rate of 2,048K bit/sec. in burst format. This is then converted by the ZNPCM1 into a dsm bit stream at 2,048K bit/sec. The dsm demodulator accepts this bit stream and produces one of two precisely defined analogue levels per single bit sample. The analogue waveform can then be recovered via a low pass filter, cutting off just above the highest signal frequency to be recovered (3.4 kHz).

Output voltages of the dsm circuit are stabilised by supplying the quad D-type from a 5 volt regulator, which is always associated with the Codec, and clamping the high state output voltages to a 2.45V reference by the use of Schottky diodes. These also help to match the voltages influencing the d.c. alignment conditions and minimise the effects of power supply variations and noise. Resistor ratio stability is obtained, along with a small modulator/demodualtor physical size by implementing the resistors and small capacitors as an in-line hybrid. More details of the operation of the dsm circuit are outlined in the Plessey brochure 'A Single Channel Codec'.

An interesting development, again in co-operation with British Telecom, is the integrated circuit dsm solution, the ZNPCM2. This will reduce the circuitry surrounding the ZNPCM1 to a single I.C. and seven capacitors.

The Codec performance related to CCITT criteria is outlined in Fig.2.

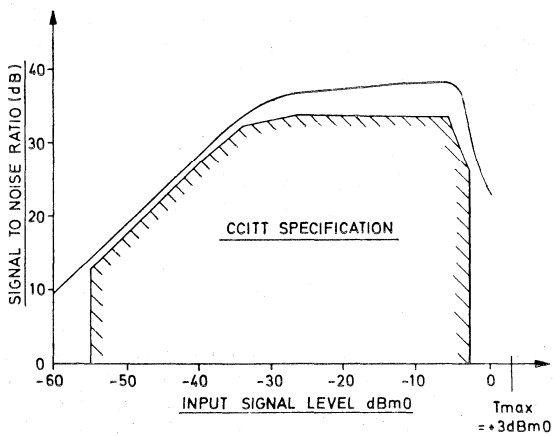


Fig. 2.

(b) A 30 Channel PCM Codec Solution

Traditionally the code conversion process on branch-to-main telephone exchange systems has been performed using multiplexed codecs. Historically the reason for this has been the codec specification where the signal-to-noise and gain-linearity constraints imposed on the systems have resulted in the use of expensive hybrid codecs. It might seem immediately obvious that the use of single channel codecs offers a more attractive solution, however a comparison of one of the major performance criteria is first of all necessary, that of power dissipation. Indeed, an initial comparison using the conventional 30 Channel PCM system shows the single channel codec approach to disadvantage. However, a more detailed analysis, using the single channel codecs in a power switching mode, shows this technique to be compatible with time shared codecs. This is described in section (d).

Let us first of all consider the system approach for using the single channel codecs in a 30 channel PCM system by looking at Fig.3.

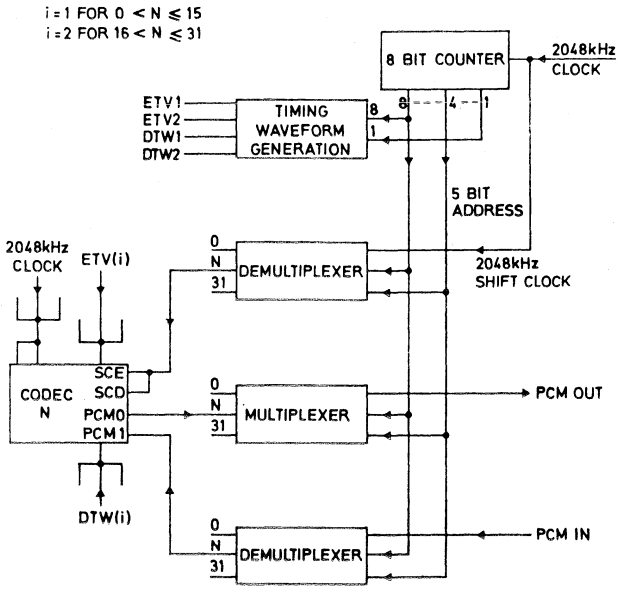


Fig. 3.

Fig. 3 shows how a 32 time slot (Note: A 30 Channel system has in fact, 32 time slots, the two additional ones being for signalling notation and synchronisation), 2,048K bit/sec. multiplex can be formed and decoded using 30 single channel codecs, when the two directions of transmission operate synchronously. Only the Nth codec is shown, connected to the 'Nth' port of the 32 port multiplexer and demultiplexers. When the 5-bit address equals N the 2,048 kHz shift clock is routed through the 'Nth' codec for eight clock pulses as shown in Fig. 4(a). The shift-in and shift-out clock terminals of the codec are commoned together. Since the shift-out terminal uses a negative active clock edge and the shift-in terminal uses a positive active clock edge the pcm digits for the two directions may be in exact time alignment. This is compatible with using the same 5-bit address for the multiplexer and the other demultiplexer.

The Encoder Timing Vector (ETV) and the Decoder Timing Waveform (DTW) may be derived from a counter driven by the 2,048 kHz clock and commoned across a number of codecs. For a 32 time slot multiplex, two sets of ETV's and DTW's should be generated with a half frame displacement as shown in Figs. 4(b) and 4(c). The first pair will supply ports 0 to 15 and the second pair ports 16 to 31, and consequently allowing the shift activity to be kept well clear of the timing waveforms for a given codec.

For a conventional 32 time slot codec ports 0 and 16 correspond to the synchronisation and signalling channels respectively.

Fig. 5 shows a similar arrangement for generating and decoding a 32 time slot multiplex when the two directions of transmission operate asynchronously. The two directions are operated quite independently but using similar principals to those previously discussed. It should again be noted that two sets of ETV's and DTW's should be used.

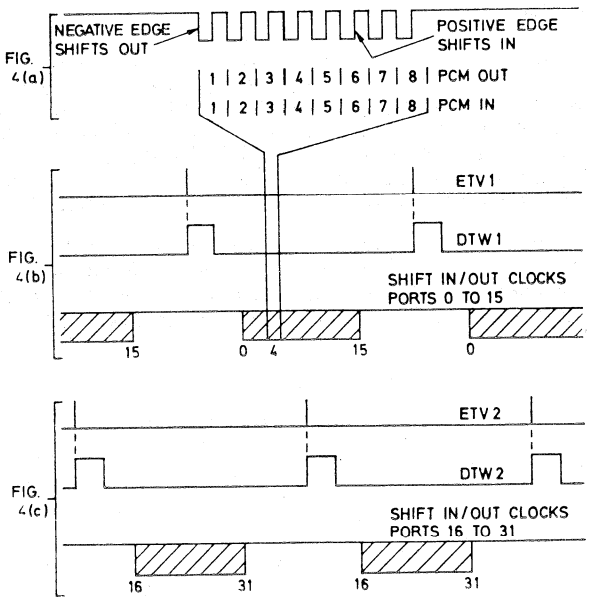


FIG. 4(a)
NEGATIVE EDGE SHIFTS OUT
POSITIVE EDGE SHIFTS IN
1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | PCM OUT
1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | PCM IN
FIG. 4(b)
ETV1
DTW1
SHIFT IN/OUT CLOCKS PORTS 0 TO 15
15
0 4
15
0
FIG. 4(c)
ETV2
DTW2
SHIFT IN/OUT CLOCKS PORTS 16 TO 31
16
31
16
31

Fig. 4.

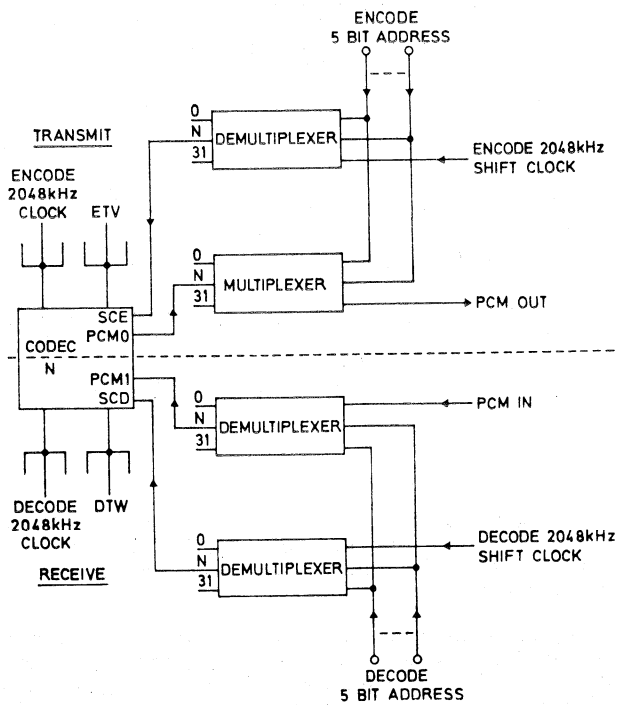

ENCODE 5 BIT ADDRESS
TRANSMIT
ENCODE 2048kHz CLOCK
ETV
0
N
31
DEMULTIPLEXER
ENCODE 2048kHz SHIFT CLOCK
MULTIPLEXER
PCM OUT
SCE
PCM0
CODEC
N
PCM1
SCD
PCM IN
DEMULTIPLEXER
DECODE 2048kHz CLOCK
DTW
RECEIVE
DEMULTIPLEXER
DECODE 2048kHz SHIFT CLOCK
DECODE 5 BIT ADDRESS

Fig. 5.

(c) Switching Applications

The ZNPCM1 can be used in a variety of ways to satisfy switching applications. One technique is to operate directly on the 2,048K bit/s digit stream produced by the circuit arrangement shown in Fig. 3, where each codec has a defined time slot in the bit stream. An alternative technique would be to derive the address applied to the multiplexer and demultiplexer from the contents of a random access memory (RAM) which defines the codec to be used in a given time slot, in an exchange of PCM codewords between the codec and an intermediate store. In this mode of use the codec interface is effectively used as a time switch store.

The circuit shown in Fig 5 can be used without an intermediate store where again the codec addresses are derived from RAM's. The encode address defines the 'source' and the decode address the 'sink' in a given time slot. The decode address may be delayed with respect to the encode address by an integer number of 2,048 kHz clock periods to take account of any small fixed switching delay.

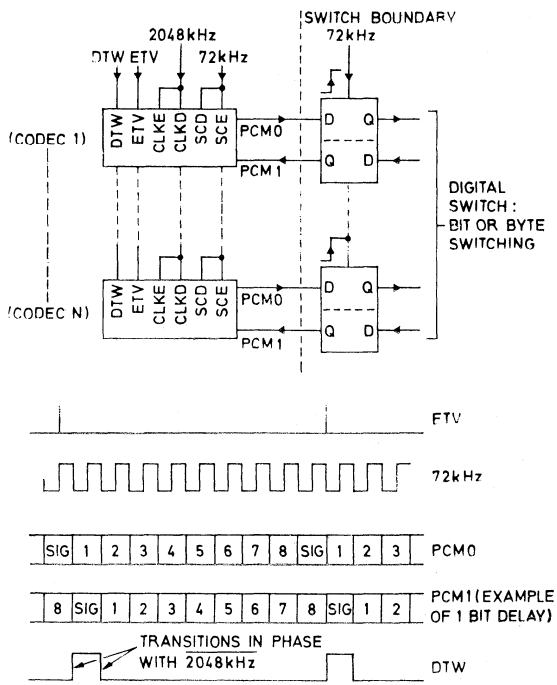


Fig. 6.

Fig. 6 shows an arrangement where the codecs input and output continuously, allowing 9-bits (8 PCM plus 1 signalling) to be exchanged in each 125 μs sample period. All the codecs may be supplied with common ETV, DTW, 2,048 kHz and 72 kHz waveforms. Each bit is retimed in the digital switch using a latch.

The digital switch may be operated using a bit switching arrangement, combined with the extraction and insertion of the signalling bits. Alternatively the bits may be reformatted into bytes and then byte switching performed. If the signalling is handled separately to the pcm codewords then a 64K bit/s rate can be used to and from the codec. This is compatible with using the codecs internal clock mode (MS = 1) in which case the only common timing waveforms required at the codec are the 2,048 kHz clock and the ETV.

(d) Power Switching

Comparisons have previously been made between shared and single channel codecs where these comparisions were reduced to one of power dissipation. Considerable power savings can be made by using the codecs in such a mode that they are only powered-up when required for use.

It is interesting to compare the power dissipation of an eight channel system using in one case eight ZNPCM1s in a power switching mode and, in the other case, one of the more popular time shared codecs which caters for eight channels. One single channel codec dissipates 600 mW and the time shared codec dissipates 1500 mW.

If the channel occupancy is p, then the average power dissipation per channel for the time shared codec is given by

$$W_{TS} = 1 - (1-p)^8 \frac{1500}{8} \text{ mW}$$

This assumes the time shared codec is only powered-up when any of the eight channels are required for use.

The average power dissipation per channel using the single channel codecs is simply given by

$$W_{SC} = p.600 \text{ mW}$$

Fig. 7 shows a plot of power dissipation versus channel occupancy ; p for both approaches. The busy period average channel occupancies are likely to be in the range 0.2 to 0.15, clearly the lower end of the curves. Taking a figure of p = 0.06, for example, then the single channel codec dissipates only 36 mW per channel, approximately 50% less than the time shared codec. As the graph shows even for very busy exchanges given values for p of up to 0.3 shows the ZNPCM1 system to dissipate less power.

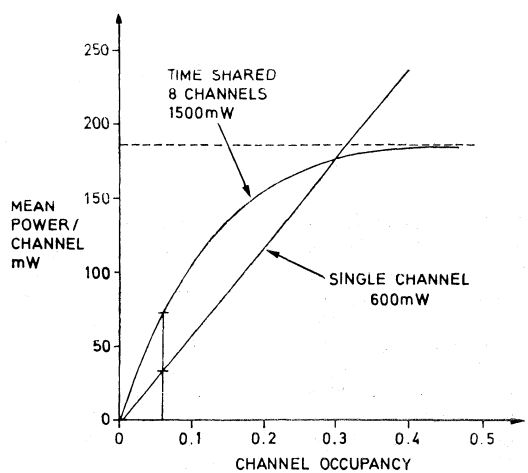


Fig. 7.

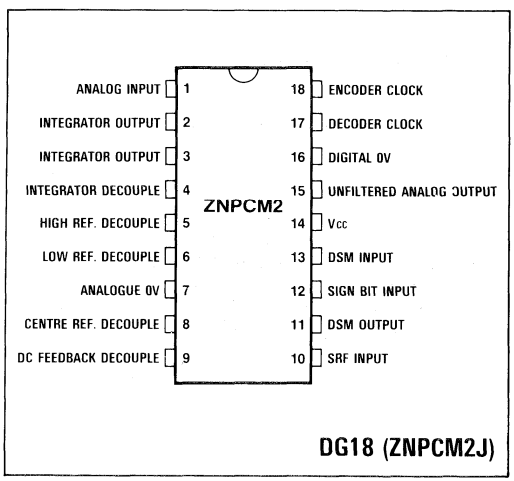
DS3136-1.0

ZNPCM2

DELTA SIGMA MODULATOR/DEMODULATOR

FEATURES

- Converts Analog Input Signal into Delta-Sigma Modulated (DSM) Signal to be used as Input for ZNPCM1 Codec IC.
- Converts DSM Signal from ZNPCM1 into Level-Defined Digital Pulse Stream for Conversion to the Analog Equivalent Signal using Low-pass Filter Techniques.
- High Signal-to-Noise Ratio.
- Monolithic IC Combining Analog and Digital Circuitry.
- Single 5V Supply
- 18-Lead Ceramic DIL Package



Pin connections - top view

DESCRIPTION

The ZNPCM2 Delta-Sigma Modulator/Demodulator (DSM) IC is designed for use in conjunction with the GEC Plessey Semiconductors ZNPCM1 or the GI AY-3-9900 Codec ICs as the conversion unit in pulse code modulation communication systems. The ZNPCM2 modulator function converts analog speech or data signals into a sampled signal of one bit per sample at a high sampling rate. The demodulator function produces an output signal having one of two well-defined voltage levels in response to the single input bit per sample input signal. The original signal can then be recovered using low-pass filter techniques.

The ZNPCM2 provides excellent signal-to noise ratio as a result of innovative circuit techniques developed by British Telecom. A rectangular input waveform designated as a spectral redistribution function (SRF) is provided and this modifies the quantisation noise spectrum, moving the noise components to higher frequencies.

By varying the amplitude and phase of the SRF waveform, the net effects on the PCM outputs from the Codec system can be made to be zero if the SRF is sampled synchronously within the system. In addition, a complex feedback network is used in the DSM circuit to provide increased feedback at low frequency which results in the relative attenuation of low frequency quantisation noise components below 32kHz.

DC alignment to better than 0.01% at low signal amplitudes is achieved at the output by use of a feedback loop minimising both the DSM voltage offset and the digital code offset. This technique makes use of the fact that the PCM code words have a sign and magnitude format and the result eliminates the need for component trimming.

Designed using the same technology as the ZNPCM1 Codec I.C., the ZNPCM2 combines both linear and digital circuits on the same monolithic I.C. Packaged in an 18-lead ceramic (ZNPCM2J) DIL, the device is designed to operate over the temperature range 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... +7 volts
Digital Input Voltage, $V_{IN(D)}$ ..... +5.5 volts
Analogue Input Voltage, $V_{IN(A)}$ ..... 4 volts pk-to-pk
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage	4.75	5.0	5.25	V
High-level Output Current, I_{OH} (Digital Outputs)	—	—	−400	μA
Low-level Output Current, I_{OL} (Digital Outputs)	—	—	4	mA
Analogue Output Impedance, Z_{AO}	—	100	—	Ω
Operating Temperature Range, T_{amb}	0	—	70	°C

ELECTRICAL CHARACTERISTICS (over the recommended operating temperature range).

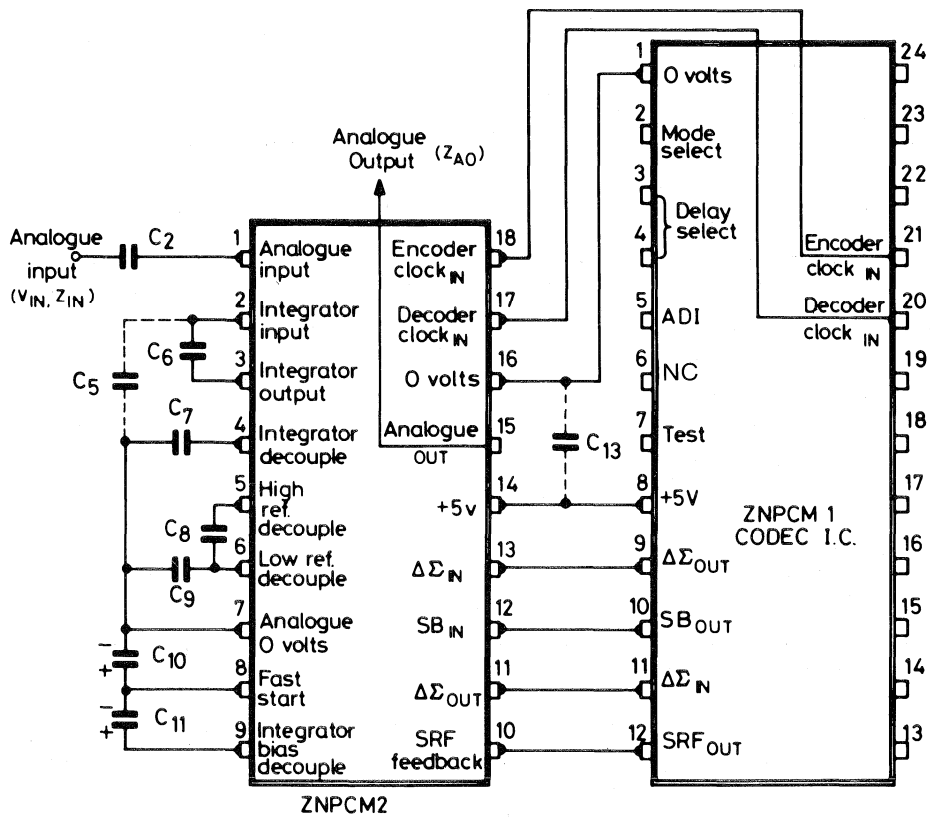
(a) Digital Inputs and Outputs.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage		2.3	—	—	V
V_{IL}	Low-level input voltage		—	—	0.8	V
V_{OH}	High-level output voltage	V_{CC} = Min, I_{OH} = Max.	2.4	4	—	V
V_{OL}	Low-level output voltage	V_{CC} = Min, I_{OL} = Max.	—	—	0.4	V
I_{IH}	High-level input current	V_{CC} = Max, V_{IH} = Min.	—	0.2	0.4	mA
I_{IL}	Low-level input current	V_{CC} = Max, V_{IL} = Min.	—	—	10	μA
I_{CC}	Supply current	V_{CC} = Max.	—	24	—	mA
f	Operating frequency		—	2,048	—	kHz
t_r & t_f	Rise and fall time	0.4V − 3.0V transition	5	—	40	ns
t_{pd}	Propagation delay	Clock $\varnothing_E$ or $\varnothing_D$ to DSM output 2.5V level	—	40	60	ns
t_{pw}	Pulse width	Between 1.5V levels	200	—	—	ns

(b) Analogue Input and Output.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Analogue Input Voltage for 0dBm0	Peak-to-peak	—	1.4	—	V
Z_{IN}	Analogue Input Impedance	Measured at 1kHz	80	100	—	kΩ
V_C	D.C. Voltage across C_{11}	V_{CC} = Max.	—	±3.0	±5.0	mV

DSM CODEC INTERFACE



NOTES

1 The external high frequency decoupling between pins 5, 6 and 7 should be of minimal impedance (i.e. in the range of 1 to 20 MHz). Low loss capacitors connected via minimal conductor path lengths and inductances are required. Suitable capacitors are 0.22μF monoblock types. Total connection length and resistance including capacitor leads should be as follows:

Pins 5 to 6 <10mm and <0.1Ω
Pins 6 to 7 <16mm and <0.1Ω

2 Analogue ground pin 7 and digital ground pin 16 must be linked externally. Ideally, this should be their only connection; however, if it is essential that the two 0V systems are connected at a point remote from the ZNPCM2 then pin 16 should remain connected to the analogue ground only.

3 Performance of the ZNPCM1 and ZNPCM2 is layout dependent and an optimum layout is shown on page 6-20. Capacitors C_5 and C_{13} are optional but may improve performance in some instances.

PERFORMANCE

The codec combination of the ZNPCM1 and ZNPCM2 meets all the performance requirements of the C.C.I.T.T. recommendation G712 with good safety margins. Using a standard pcm multiplex tester and a spectrum analyser the following performance figures result:

(1) Idle Channel noise: −70dBm0p (See Fig. 1).
C.C.I.T.T. recommendation = −65dBm0p

(2) Signal-to-noise ratio and gain level linearity: Figs. 2(a) and 2(b) show the results using a 450 − 550kHz pseudo-random noise test.

(3) Intermodulation distortion: measured products are at least 10dB and on average 18dB better than C.C.I.T.T. recommendations.

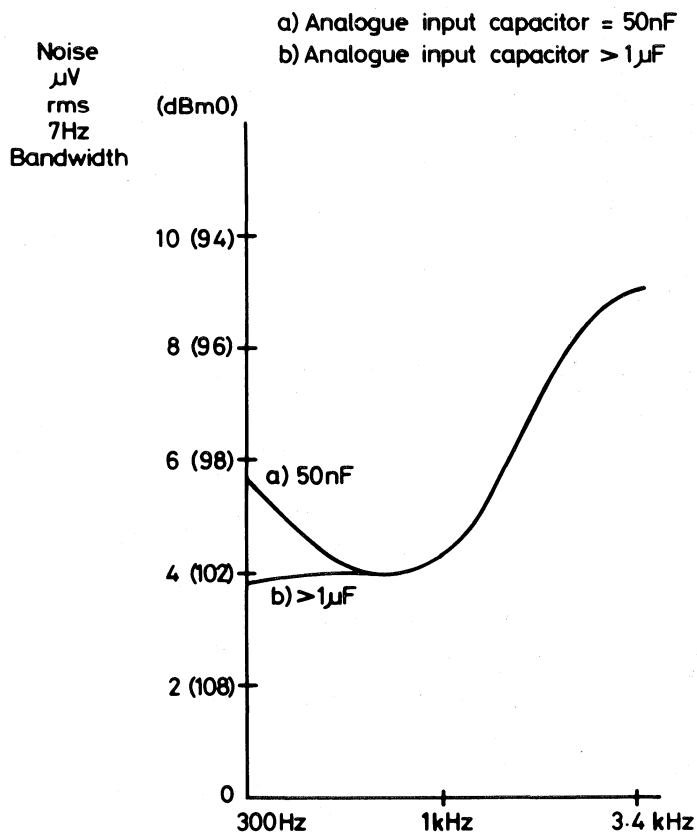
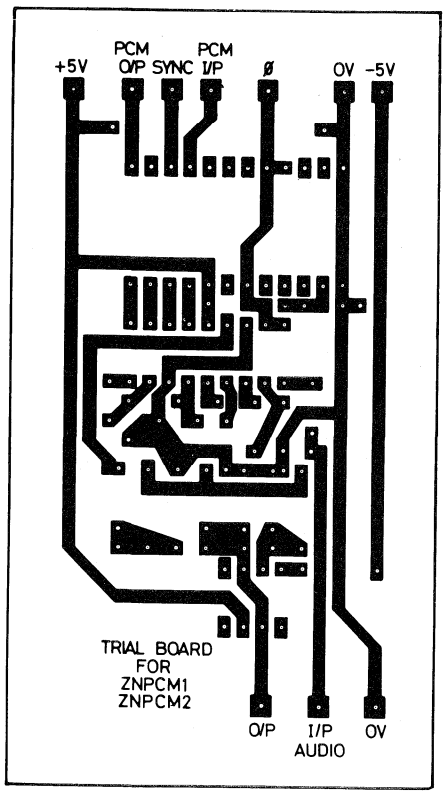
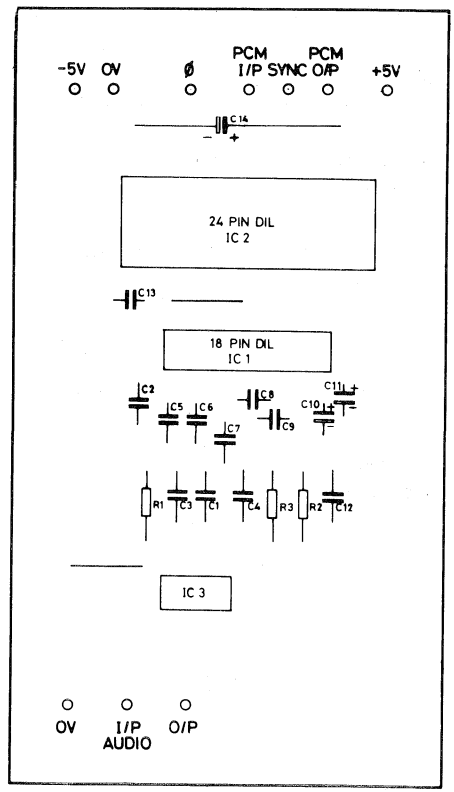


Fig. 1. Idle Channel Noise Spectrum

BASIC SYSTEM BOARD FOR ANALOGUE TO ANALOGUE PERFORMANCE EVALUATION





P.C. BOARD

COMPONENT LAYOUT

ACTUAL SIZE

ZNPCM1 & ZNPCM2 TRIAL UNIT

Component List (Tolerances ±20% unless otherwise shown)

IC1	ZNPCM2	C6	47pF ±5%
IC2	ZNPCM1	C7	4.7nF ±5%
IC3	741 Op Amp	C8	0.22μF
R1	91k0 2%	C9	0.22μF
R2	91k0 2%	C10	10μF, 16V Tantalum Electrolytic
R3	100k0	C11	10μF, 16V Tantalum Electrolytic
C1	0.022μF	C12	47nF
C2	47nF	C13	0.1μF Ceramic
C3	100pF ±2%	C14	6.8μF, 10V Electrolytic
C4	1nF ±2%		
C5	10pF		

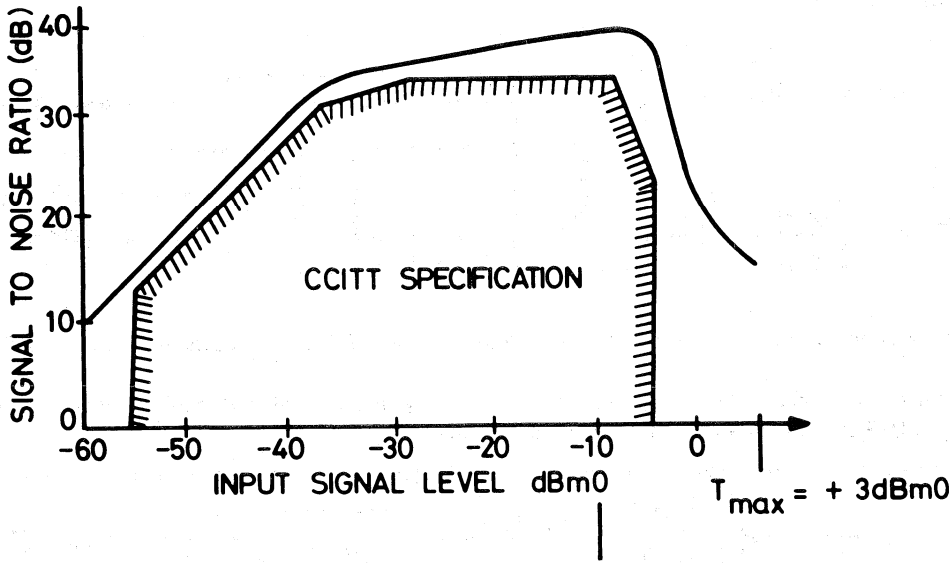


Fig. 2(a). Signal to Noise Ratio 'A Law'

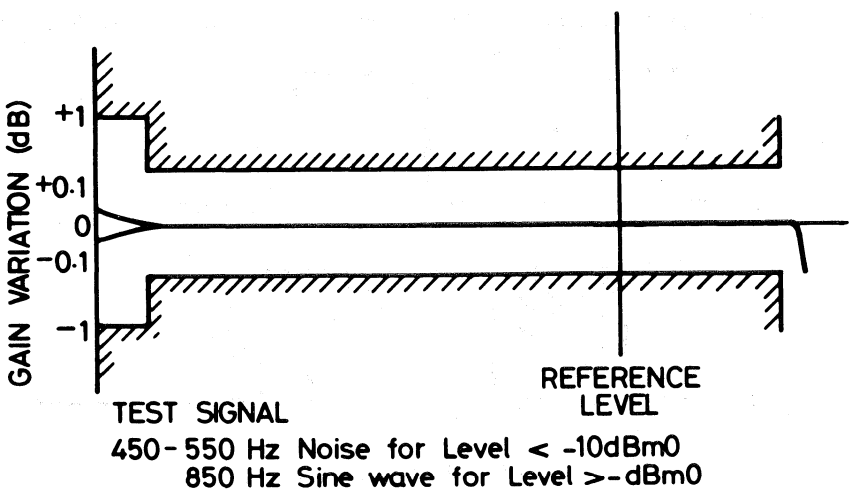
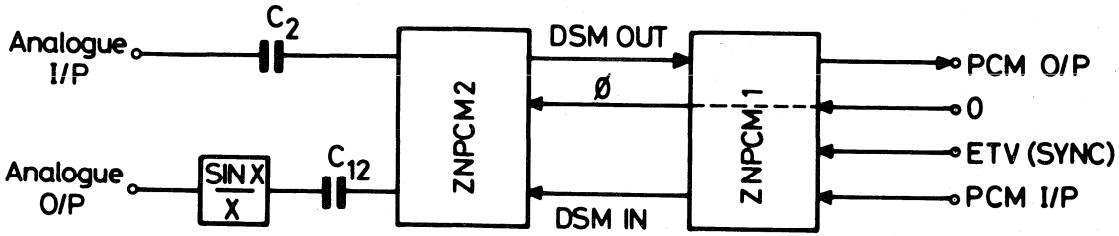


Fig. 2(b). Gain to Signal Level 'A Law'

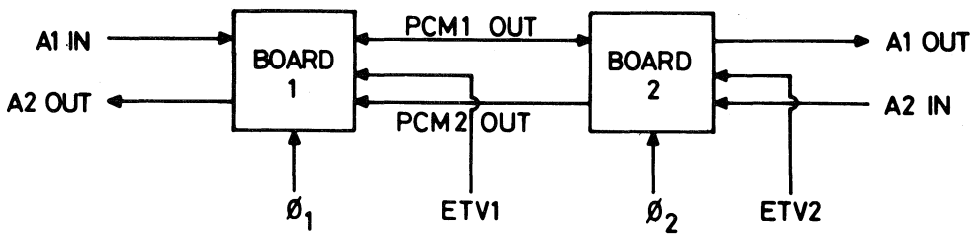
SCHEMATIC



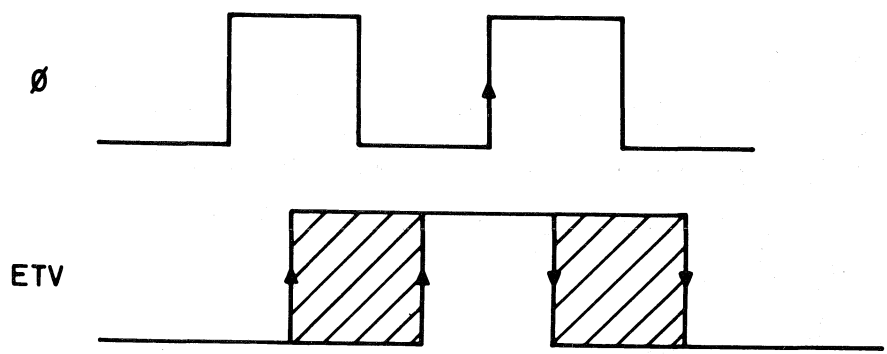
Single Channel Codec System Operating in Internal Mode (PCM at 64K bits/sec. without ADI).

Performance of the ZNPCM1/2 may be simply evaluated by linking PCM O/P to PCM I/P and comparing Analogue O/P to Analogue I/P. No ETV (Sync) signal is required for this.

For a more comprehensive evaluation two boards are required connected on the configuration shown,



$Ø_1$ and $Ø_2$ must be the same frequency and ETV1 and ETV2 can be common or up to 30 clock periods displaced.



WAVEFORMS SHOWING ETV TOLERANCE

DS3137-1.0

MS2014

DIGITAL FILTER AND DETECTOR (FAD)

The MS2014 is a real time general purpose digital signal processor (DSP) which is easily programmed to perform digital filtering and level detection. The architecture of the FAD comprises a cascadable second order recursive filter and level detector using dedicated multipliers, adders and delay elements.

The data controlling the response of the MS2014 is stored in an external PROM or RAM and consists of a list of filter coefficients and comparison levels. This simple data format means that the user does not need an expensive development system at the design stage (in contrast to other DSP devices, which use microprocessor-based structures and require considerable software development effort to realise their function). The off-chip data memory allows for easy adaptive control, even when complicated algorithms are to be implemented.

The filter and detector have been designed to give maximum flexibility in use and can easily generate most of the functions required in tone detector, spectral analysis, adaptive filter and speech synthesis systems.

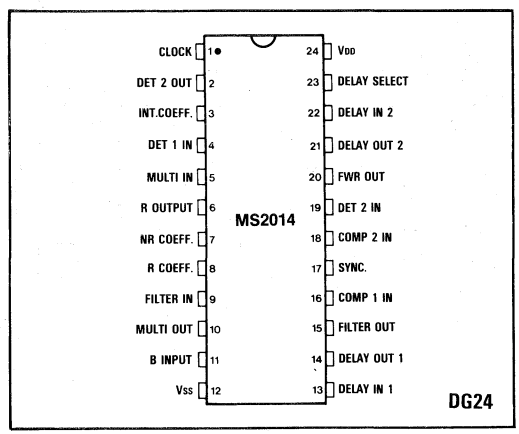


Fig.1 Pin connections - top view

FEATURES

- Linear 16-Bit Data
- 13-Bit Coefficient
- 2MHz Operating Clock Frequency
- Serial Operation
- 448 Bits of On-Chip Shift Register Data Storage for 8th Order Multiplex
- Nth Order Multiplexing ($N \leqslant 8$)
- TTL Compatible
- Single +5V Supply

APPLICATIONS

- Low Cost Digital Filtering
- Level Detection
- Spectral Analysis
- Tone Detectors (Multi-Frequency Receivers)
- Speech Synthesis and Analysis
- Data Modems
- Group Delay Equalisers (All-Pass Networks)

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD})	-0.5V to +7V
Input voltage	-0.5V to +7V
Maximum output voltage	+7V
Temperature: Storage	-65°C to 125°C
Operating	0°C to 70°C

NOTE
All voltages with respect to V_{SS}.

PIN NAMES

	Name	Function	I/O
1	Clock	Single phase clock input	I
2	Detect 2 Out	Output from detector 2	O
3	Int.Coeff	Integrator coefficients	I
4	DET 1 In	Detector 1 input	I
5	Mult In	Input to NR B multiplier	I
6	R Output	Output of recursive section	O
7	NR Coeff	Non-recursive (NR) coefficient input	I
8	R Coeff	Recursive coefficient input	I
9	Filter In	Data input to filter section	I
10	Mult Out	Output from B multiplier	O
11	B Input	Input from B multiplier	I
12	V_{SS}	0V	
13	Delay In 1	Input from filter external delay	I
14	Delay Out 1	Output to filter external delay	O
15	Filter Out	Data output from filter section	O
16	Comp 1 In	Comparison level 1 input	I
17	Sync	Synchronisation pulse input	I
18	Comp 2 In	Comparison level 2 input	I
19	DET 2 In	Input for detector 2 via FWR	I
20	FWR Out	FWR output from Det 2 In data	O
21	Delay Out 2	Output from detectors 1 and 2, and connection to detector external delay	O
22	Delay In 2	Input from detector external delay	I
23	Delay Select	Internal/External delay selector	I
24	V_{DD}	+5V supply	

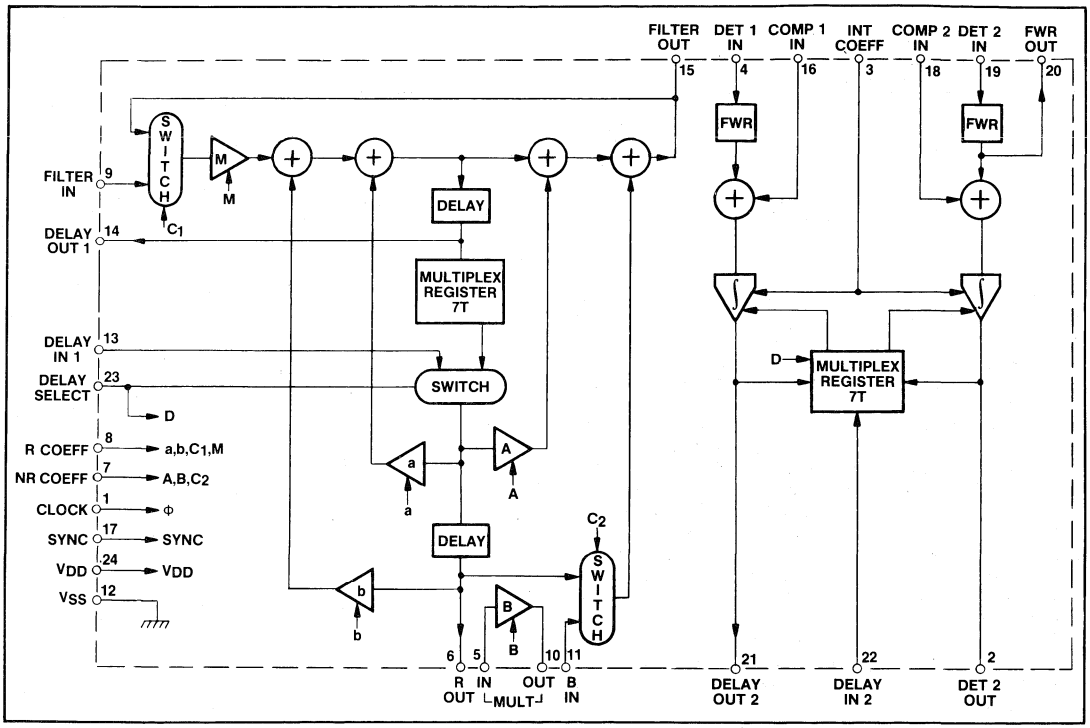


Fig.2 Block diagram

PERFORMANCE

A sample throughput of 64000 samples/s is guaranteed. Thus using a sampling period of 125μs (8000 samples/s) the following may be realised:

8 bi-quadratic 2nd-order recursive filter sections;
plus 16 full-wave rectification operations;
plus 16 1st-order leaky integrations;
plus 16 level comparisons.

Filters of more than 16th order are possible but will require a lower sampling rate or more than one MS2014.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Supply voltage	V_{DD}	4.75	5.25	V	
Input voltage (high state) except clock	V_{IH}	2.2	-	V	
Input voltage (low state) except clock	V_{IL}	-	0.7	V	
Input voltage (high state) clock	V_{IHC}	4.5	-	V	
Input voltage (low state) clock	V_{ILC}	-	0.5	V	
Clock rise and fall time	t_{cl}		30	ns	10% - 90% (Note 1)
Clock frequency	f_{cl}	0.5	2.048	MHz	
Operating temperature	T_{amb}	0	70	°C	

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = +5V T_{amb} = 25°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	I_{DD}		90	120	mA	
Output voltage, low	V_{OL}	-	-	0.5	V	I_{OL} = 0.4mA (Note 2)
Output voltage, high	V_{OH}	2.7	3.4	-	V	I_{OH} = -40μA (Note 2)
Input capacitance (except clock)	C_{in}		5	7	pF	
Input capacitance (clock)	C_{inc}		25		pF	
Input data set up time	t_{is}	50	-	-	ns	Fig.7
Input data hold time	t_{ih}	150	-	-	ns	Fig.7
Output data delay time	t_{os}	-	-	200	ns	Fig.7

NOTES
1. An operating clock frequency of 2.048MHz is guaranteed over the supply voltage range and the full operating temperature range.
2. The output stage is designed to drive a standard TTL LS gate (74LS series).

FUNCTIONAL DESCRIPTION

The Filter Section

The filter section provided in the MS2014 is a second order recursive type (see Fig.3). This structure was chosen because of its good coefficient sensitivity and predictable round-off, limit-cycle and overflow properties. Higher order filters are easily produced by cascading sections in a similar manner to analogue active filter design.

The transfer function of the section is given by:

$$H(z) = M \frac{[1 + Az^{-1} + Bz^{-2}]}{[1 - az^{-1} - bz^{-2}]} \quad \ldots (1)$$

The coefficients *a* and *b* define a pair of complex poles, whilst *A* and *B* define a pair of complex zeros. The Scaling Factor *M* is necessary because many filters have greater than unity gain, hence there is a danger of numeric overflow in the filter arithmetic. In the MS2014 this scaler multiplies by a factor of

$$M = (\tfrac{1}{2})^n \text{ where } 0 \leqslant n \leqslant 13$$

The multipliers in the MS2014 are serial/parallel types which require the coefficient data as a static parallel word. To minimise the number of pins on the device, this data is loaded serially and stored in a SIPO shift register. Each multiplier requires the coefficient data to be in 2s complement form with 12 bits for the fractional part of the number.

The range for the coefficients are:

$$\begin{aligned} 2 &> A \geqslant -2 \\ 2 &> a \geqslant -2 \\ 1 &\geqslant B \geqslant -1 \\ 1 &> b \geqslant -1 \end{aligned}$$

For the *A,a* coefficients there is an added bit ($a_S A_S$) to give the extra ±1 range, which gives a total of 14 bits for the *A,a* coefficients and 13 bits for *B,b*.

The second-order filter is very easily multiplexed by increasing the delay function in steps of *T* (where *T* is the computation period*) and time-sharing the arithmetic elements. The limit on this process is the maximum clock rate of the MS2014. With a 32 bit computation cycle the clock rate f_{cl} is given by:

$$f_{cl} = 32 \times f_s \times Y$$

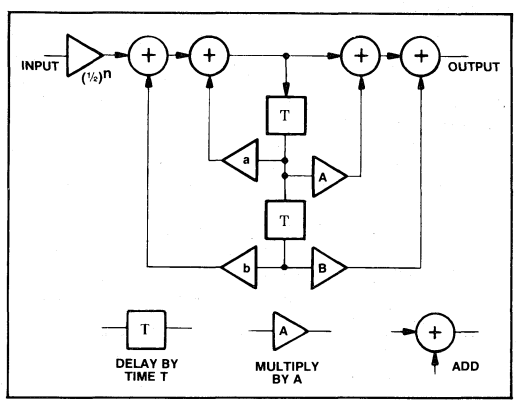


Fig.3 Basic 2nd order filter section

where *Y* is the number of times the filter is multiplexed and f_s is the sampling rate (the reciprocal of the sampling period T_s **). In telephony applications it is usual for f_s to be 8000 samples/s; hence at the maximum guaranteed clock rate of 2048kHz, *Y* must be less than or equal to 8.

By presenting an input sample during every 32-bit computation cycle, 8 separate second-order filters can be implemented. As the inputs can be independent of each other the filter is then said to be 'channel multiplexed'.

Filters of higher order can be built by feeding the output data emerging from one second-order section back to the input via an on-chip data selector, which is enabled by the control bit C_1; since the delay between the input and output of the filter section is 32 clock periods, the data arrives at the beginning of the next computation cycle. Thus by controlling the data selector two or more second-order filter sections can be cascaded. This arrangement allows any combination of filter and channel multiplexing to be achieved.

Higher orders of channel or filter multiplex require the connection of additional delay. For 8th-order multiplex, a delay of *7T* (224 bits) is provided on chip; together with the inherent delay *T* (32 bits) of the computation cycle, this

*T = computation period = 32 x (1/2048k)s = 15.63μs i.e. 32 bits at 2048 kbit/s clock rate.

**T_S = sampling period = (1/8000)s = 125μs at a sampling rate of 8kHz i.e. 256 bits at 2048 kbit/s clock rate.

makes up the necessary $8T$ delay. Other orders of multiplex require the external connection of $(Y - 1) \times 32$ bits of delay.

The detector function is carried out by 'full wave rectifiers' followed by comparators and leaky integrators. By interconnecting these in different ways various absolute and relative level decisions can be made.

The 'Full Wave Rectifiers'

Data entering the 'full wave rectifiers' is inverted if the sign bit of the word is a '1' (i.e. negative). The 1LSB error generated by this is insignificant and does not materially affect operation of the detector.

The Integrators

The integrators in the MS2014 are unity gain variable-leak-factor types. Fig.4 shows the internal arrangement. The leak factor

$$1\text{-}2^{-(K+1)}$$

controls the rise time of the integrator, the relationship is given in Table 1.

Level Detection

Both relative and absolute level detectors can be implemented in the MS2014. Fig.5 shows the arrangement for an absolute level detector. The sign bit of the data word emerging from the integrator is '1' if the mean level of the filter output is greater than the comparator input level.

Relative level detection can be achieved by using the arrangement of Fig.6. In most applications where relative level sensing is required, the filtering can be arranged such that $B = 1$ (i.e. the complex zeros are located on the unit circle in the z plane), this allows the B multiplier to be used for scaling the relative levels. In this application the B coefficient must be negative.

Leak factor	Rise time (0 to 90%)
1/2	3 Ts + T
3/4	8 Ts + T
7/8	17 Ts + T
15/16	35 Ts + T
31/32	72 Ts + T
63/64	146 Ts + T
127/128	293 Ts + T
255/256	588 Ts + T

Table 1 Integrator rise times

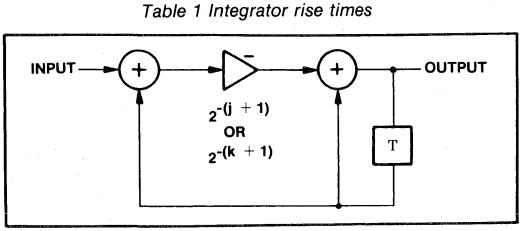


Fig.4 Leaky integrator

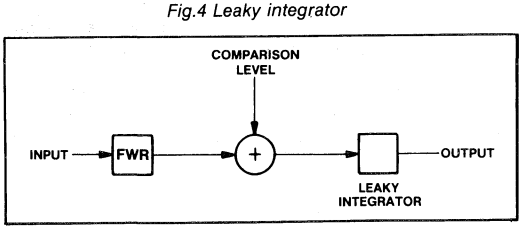


Fig.5 Simple level detector

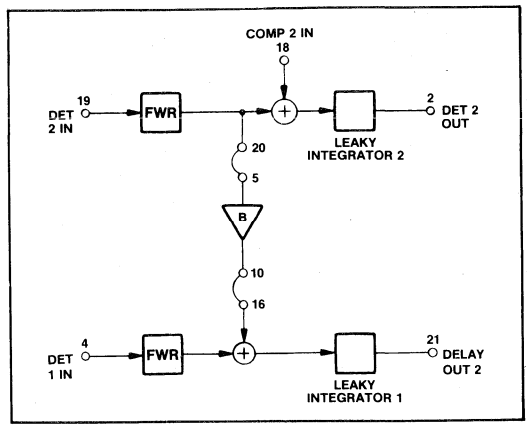


Fig.6 Relative level detection

FILTER DESIGN WITH THE MS2014

One of the commonest techniques for designing analogue filters is to factor the transfer function into blocks which can be realised by second order filter sections. Most designs of this type are done using tables which give coefficients for equations of the form:

$$H(s) = \frac{Cs^2 + Ds + K}{Es^2 + Fs + 1} \quad \ldots (2)$$

Since the MS2014 filter section is a general second-order structure, the same design technique can be employed. By using the Bilinear Transform:

$$s = \frac{2\ (1 - z^{-1})}{T\ (1 + z^{-1})} \quad \ldots (3)$$

it is possible to design digital filters from analogue prototypes. By substituting equation (3) into (2) and re-arranging the result into the form of equation (1) the following relationships are derived:

$$A = \frac{2KT^2 - 8C}{4C + 2DT + T^2}$$

$$a = \frac{8E - 2T^2}{4E + 2FT + T^2}$$

$$M = \frac{4C + 2DT + KT^2}{4E + 2FT + T^2} \quad \ldots (4)$$

$$B = \frac{4C - 2DT + KT^2}{4C + 2DT + KT^2}$$

$$b = \frac{2FT - 4E - T^2}{4E + 2FT + T^2}$$

These five equations allow an analogue filter design to be transformed into digital form.

In addition to the four coefficients required by the filter section the data streams fed to the NR and R coefficient inputs include the four bits setting the Scaling Factor M (M_1 to M_4) and two selector control bits C_1 and C_2.

When $C_1 = 1$, data applied to FILTER IN (pin 9) goes to the filter section, when $C_1 = 0$ data emerging on FILTER OUT (pin 15) is fed back to the filter at the start of the next computation cycle.

When $C_2 = 0$ the B multiplier is by-passed by a direct connection, setting $B = 1$.

Table 2 shows the format of the serial data words for the NR and R coefficient inputs. The timing diagram (Fig.7) shows where this fits into the computation cycle. The synchronising pulse (SYNC) is coincident with the first clock pulse of the cycle and must be low before the rising edge of

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Clock Pulse Number
C_1	M_1	M_2	M_3	M_4	**b Coeff.** msb.....lsb													a_s	**a Coeff. (Recursive)** msb.....lsb													
X	X	X	X	C_2	**B Coeff.** msb.....lsb													A_s	**A Coeff. (Non-Recursive)** msb.....lsb													
0.125					0													0.73217773437														
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	1	1	0	1	1	1	R
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NR

Table 2 Filter data format

the clock. The SYNC pulse is applied every *Y* clock pulses, where *Y* = CLOCK RATE/SAMPLING RATE.

Coefficient Conversion

After the coefficients have been obtained (from the Bilinear Transform or FAD Development Program) they must be assembled in the format given in Table 2. The FAD Development Program gives the multiplier coefficients in a ready-to-use binary string format, other techniques will give numerical values for the coefficients which must be converted into binary strings.

Coefficient Conversion Algorithm for '*A*'

The algorithm for converting *A* or *a* to binary is as follows:

Obtain $A = \frac{|A|}{2} . 8191$

Convert *A* into a binary number (13 bits)

If *A* is positive INVERT THE MSB AND APPEND '0' AS NEW MSB.

If *A* is negative INVERT ALL BITS AND APPEND '1' AS NEW MSB, then ADD '1' LSB.

Conversion of '*B*' Coefficients

Obtain $B = B.4096$

Convert *B* into a binary number (12 bits)

If *B* is negative INVERT ALL BITS, ADD '1' LSB AND APPEND '1' AS NEW MSB.

If *B* is positive APPEND '0' AS NEW MSB.

In addition to the coefficient data streams one further input must be set up. DELAY SELECT (pin 23) is the control pin used to select the internal *7T* delay. A '1' maintained on pin 23 selects the internal delay and a '0' the external option. The *B* multiplier is independent of the rest of the circuit and may be used for any purpose, although usually it will form part of either the filter or detect functions. In each case the appropriate connections must be made externally.

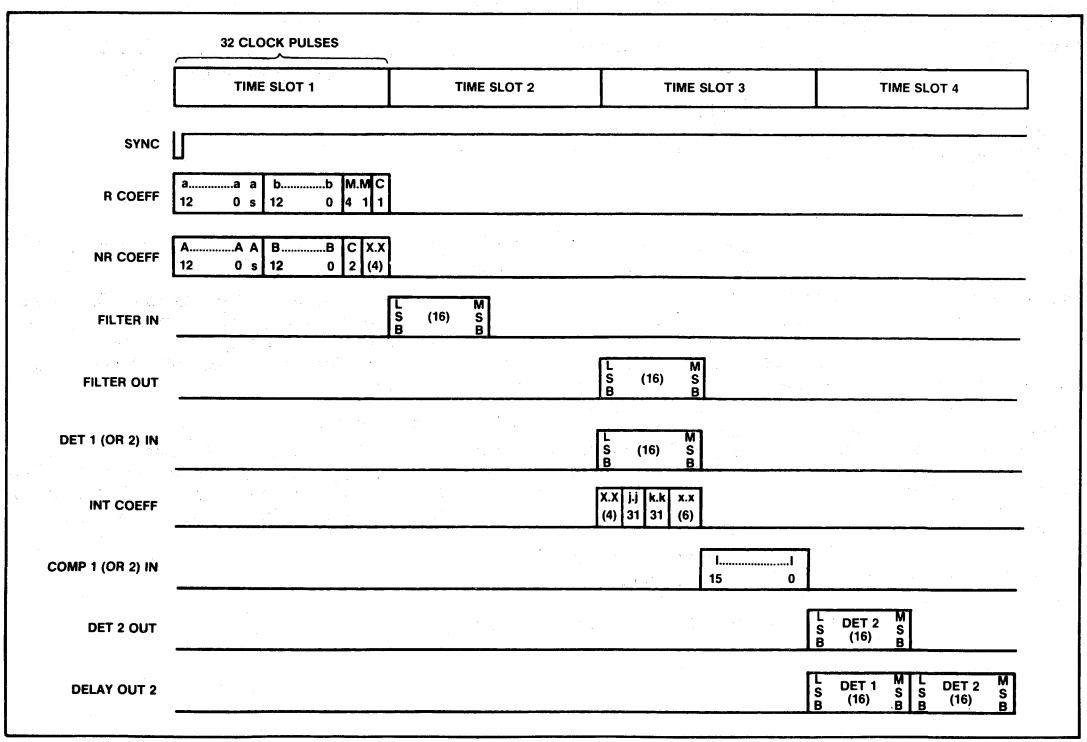


Fig.7 Timing diagram

Clock pulse number	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Integrator coefficients	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	K_1	K_2	K_3	J_1	J_2	J_3	X	X	X	X
Comparison level 1 or 2	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	P_9	P_{10}	P_{11}	P_{12}	P_{13}	P_{14}	P_{15}	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 3 Detector data format

Programming the Detector

Control data for the detect function is supplied by an external memory to the INT COEFF input (pin 3) and to the COMP 1 IN and COMP 2 IN inputs (pins 16 and 18) of the MS2014. The relative positions in time of the input sample data, detect function control data and output sample data are shown on the timing diagram (Fig.7).

Note that it is possible to economise on memory by strapping pin 3 either to pin 16 or to pin 18, since valid data for either combination of pins occurs at different times in the computation cycle. There are two integrator scaling factors in the INT COEFF data stream. The j_1, j_2, j_3 data bits determine the integrator coefficient for the data stream applied to DET 1 IN (pin 4) and the k_1, k_2, k_3 data bits for the DET 2 IN (pin 19) data stream; their definitions and clock pulse positions are given in Table 3.

In most applications, the comparison levels *l* and *m* applied to COMP 1 IN (pin 16) and COMP 2 IN (pin 18) will be negative quantities, and as they are coded in two's complement, each sign bit at clock pulse 32 will be a '1'. However,a positive quantity can be input by setting the sign bit to '0'. In this case, care must be taken to ensure that the addition of the DET data and the COMP data does not result in a number greater than unity and cause overflow, since no protection against overflow is provided in either detect function.

NOTE Round-off errors in the detector section may result in the integrator 'jamming' if the signal is below the 4 LSBs. Consequently, the available dynamic range is limited to the 12 MSBs.

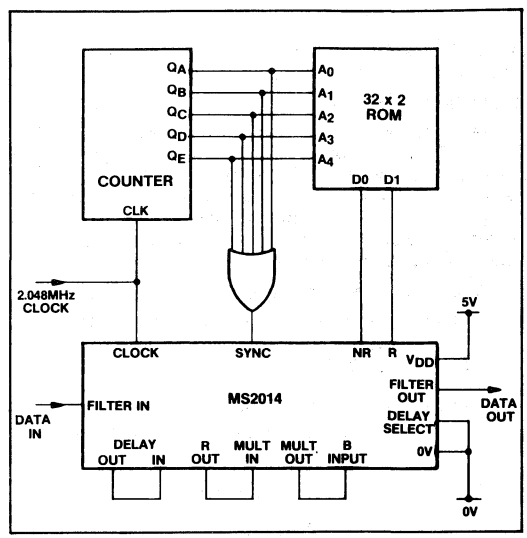


Fig.8 2nd order 32kHz bandwidth filter

TYPICAL APPLICATIONS CIRCUITS

A Second-Order High Sampling Rate Filter (Fig.8)

This is the simplest filter arrangement for the MS2014. No external delay is required so that DELAY 1 IN is connected to DELAY 1 OUT and DELAY SELECT is grounded.

A ÷32 counter generates the 5-bit wide address for the coefficient ROM. A 5-input OR gate on the address lines generates the SYNC pulse every 32 clock cycles so that at a 2.048MHz clock rate the sample rate is 64000 samples/second giving a maximum bandwidth of 32kHz.

If the desired *B* coefficient is not unity then ROUT (pin 16) must be connected to MULT IN (pin 5) and MULT OUT (pin 10) to *B* INPUT (pin 11).

A 16th Order Filter 8kHz Sample Rate Fig.9)

In this example DELAY SELECT (pin 23) is high so that the internal *7T* delay is switched in. Input data is applied during the first computation cycle (the one with the SYNC pulse in it) and coefficient data is loaded in the last computation cycle.

Channel Multiplexed Second Order Filter 8kHz Sampling

The hardware for this filter is identical to Fig.9. However, input data is provided during each computation cycle and each cycle contains a separate output. If the filter required for each channel is identical, then the coefficient memory need only be 32 x 2 bits.

Other Configurations

Sampling rates other than 64kHz and 8kHz can be achieved either by reducing the clock rate and/or by using external delays in place of the internal *0/7T*. The use of external delay also allows different orders of multiplexing.

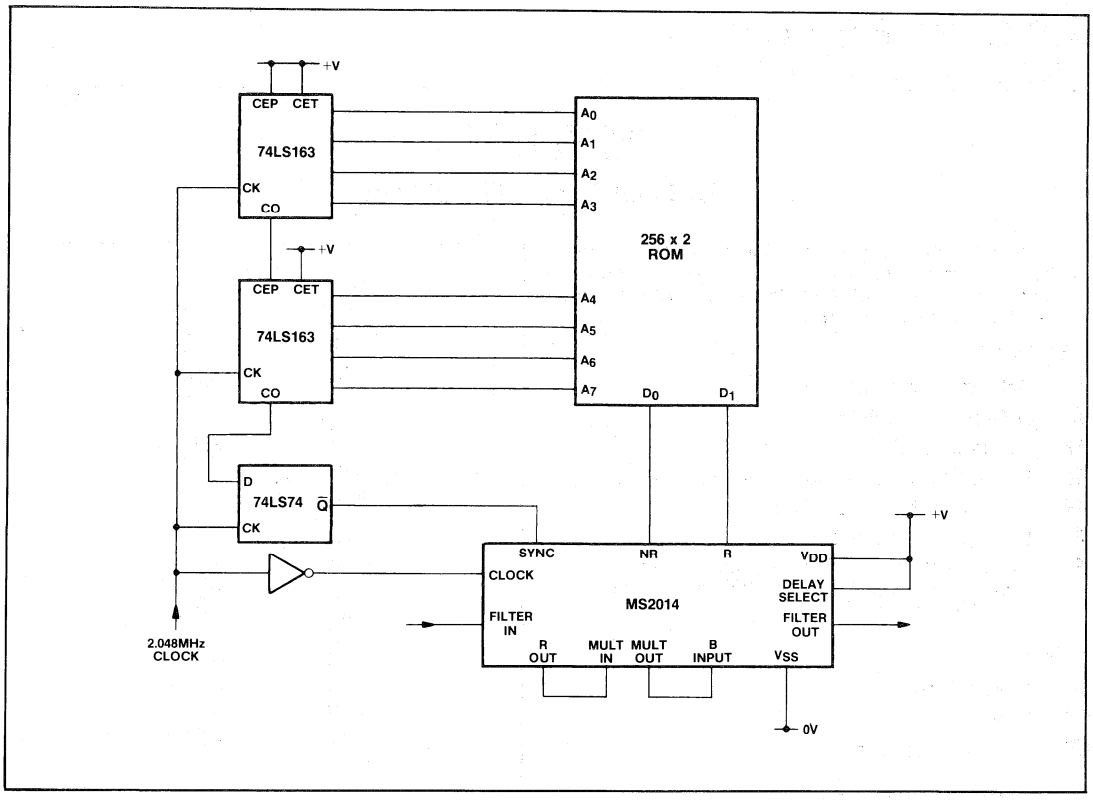


Fig.9 A 16th order 4kHz bandwidth filter

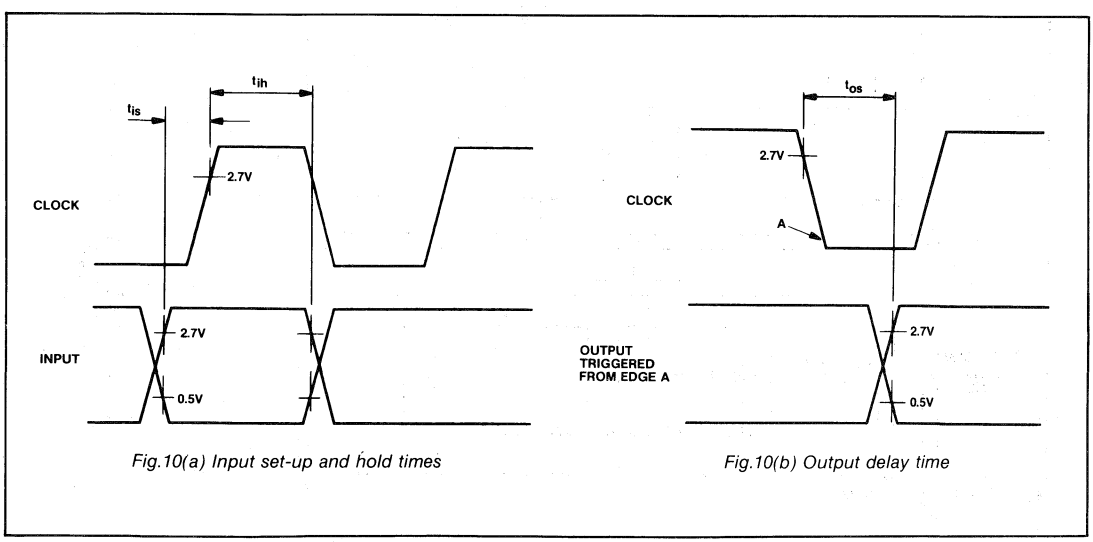


Fig.10(a) Input set-up and hold times

Fig.10(b) Output delay time

Fig.10 Input and output timing

DS3138-1.0

MV6001

HDLC/DMA CONTROLLER

The MV6001 is a combined HDLC transceiver and DMA controller capable of providing serial communications at rates up to 128K bits/second, and handling direct memory access clock rates up to 8MHz.

FEATURES

- Data Rates up to 128K Bits/s
- DMA Rate up to 8MHz
- Low Power CMOS
- Simple Interfacing to Popular 8-Bit Processors
- Frame Length up to 2K Bytes
- Low Host-Processor Overhead
- Conforms to ECMA40 and Related Standards (CCITT X.25, X.75, 1.440, ISO3309, ANSI X3.66, FED-STD 1003, FIPS71)

APPLICATIONS

- ISDN Terminals
- LANs
- X25 p.s.s. Networks

ORDERING INFORMATION

MV6001 B0 DP (Commercial Plastic DIP)
MV6001 B0 DG (Commercial Ceramic DIP)

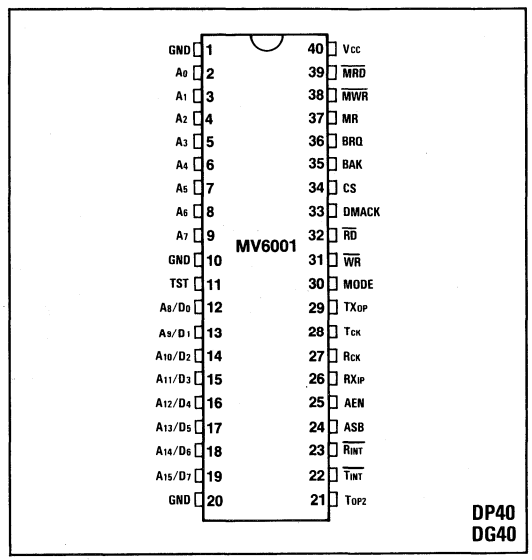


Fig.1 Pin connections - top view

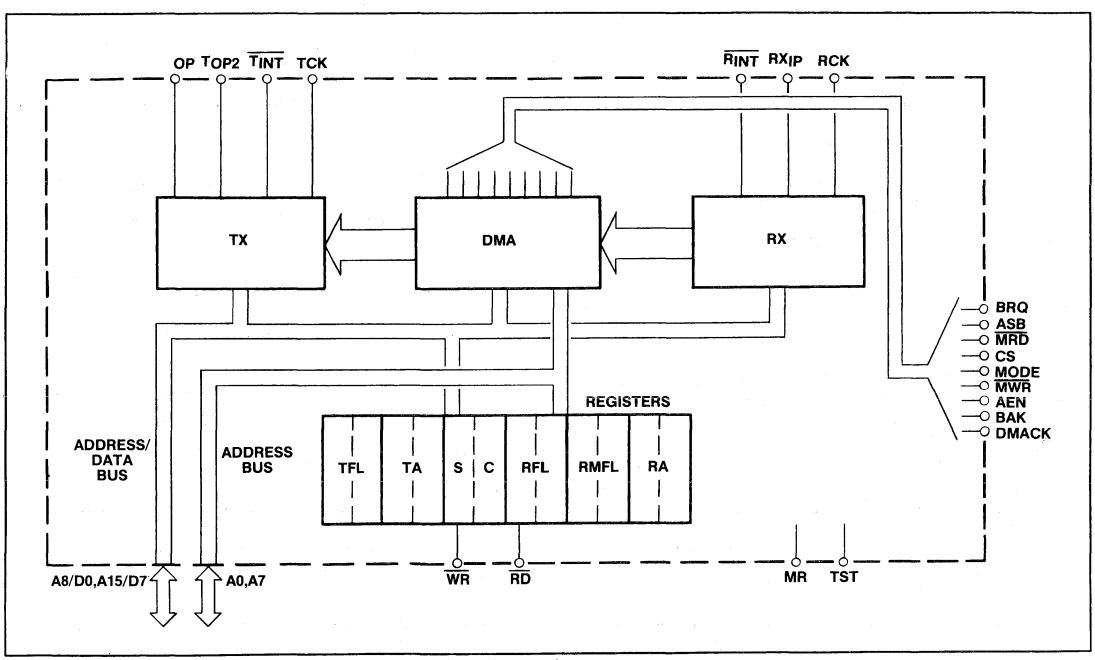
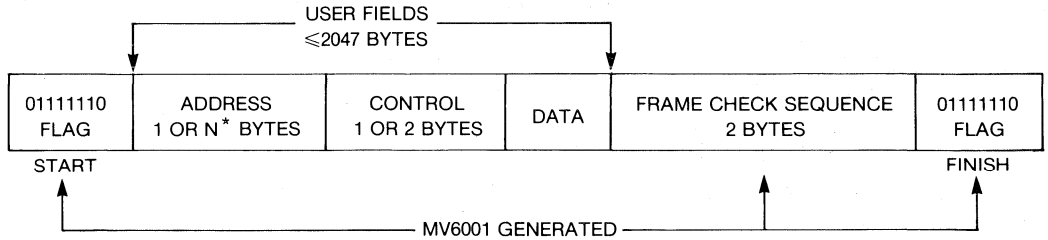


Fig.2 Block diagram

PIN DESCRIPTION

Pin No.	Name	I/O	Function
1,10,20	GND		**0V supply.** All 3 pins must be connected.
2 - 9	A_0 - A_7	I/O	**Address Bus.** Output for memory A_0 - A_7 addressing. Input for register addresses A_0 - A_3.
11	TST	I	**Test Enable.** Tie to GND for normal operation.
12 - 19	A_8/D_0 - A_{15}/D_7	I/O	**Data Bus/High Order Address.** Multiplexed data and address bus.
21	T_{OP2}	O	**Transmitter Out.** Alternative output to TX_{OP}. This output is not affected by loop back (see Operating Notes - LOOPBACK).
22	$\overline{T_{INT}}$	O	**Transmitter Interrupt.** An interrupt is generated whenever transmission of a frame is ended, either following the last FCS byte of a complete frame of when an abort sequence is transmitted. The interrupt is reset by the control register.
23	$\overline{R_{INT}}$	O	**Receiver Interrupt.** An interrupt is generated whenever a frame is received. The interrupt is reset by the counter register.
24	ASB	O	**Address Strobe.** Strobes the Address High byte from the Data/Address Bus into an external latch.
25	AEN	O	**Address Enable.** Enables the external address latch.
26	RX_{IP}	I	**Receiver Input.** Serial HDLC data input, clocked in by RCK.
27	RCK	I	**Receiver Data Clock.** Provides clock to the receiver section, frequency should be at the required data rate, this need not necessarily the the same as the transmit data rate.
28	TCK	I	**Transmitter Data Clock.** This input provides a clock signal for the transmitter section and should be set to the desired transmit data rate.
29	TX_{OP}	O	**Transmitter output.** Main transmitter output for serial data.
30	MODE	I	**Bus Control Mode Select.** Controls the polarity of BAK and BRQ. MODE = V_{CC} gives active LOW, MODE = GND gives active HIGH.
31	$\overline{WR}$	I	**Write Register.** Loads data from data bus into register addressed by A_0 - A_3.
32	$\overline{RD}$	I	**Read Register.** Reads addressed register onto data bus.
33	DMACK	I	**DMA Clock.** This input provides clock to the DMA section. The DMA clock rate should be at least ten times the sum of the transmit and receive data rates.
34	CS	I	**Chip Select.** Enables $\overline{RD}$ and $\overline{WR}$ inputs.
35	BAK	I	**Bus Acknowledge.** Input from processor relinquishing control of bus. See pin 30, Bus Mode Select.
36	BRQ	O	**Bus Request.** Output to processor requesting the bus for a DMA cycle. See pin 30, Bus Mode Select.
37	MR	I	**Master Reset.** Resets everything.
38	$\overline{MWR}$	O	**Memory Write.** This is a three-state output to write data into memory during DMA cycles.
39	$\overline{MRD}$	O	**Memory Read.** 3-state output to read data from memory during DMA cycles.
40	V_{CC}		+5V ± 10% supply.

HDLC FRAME CONSTRUCTION



*N is any integer

Fig.3

Fig.3 shows the construction of an HDLC frame. The start and finish of the frame are determined by FLAGS (the binary pattern 01111110). To prevent spurious recognition of flags in the user fields, the transmitter automatically inserts a '0' after five successive '1's. The inserted '0's are removed by the receiver, and hence are not seen by the user. Each HDLC frame contains a 2 byte frame check sequence produced by a cyclic redundancy generator in the transmitter. This sequence is checked by the receiver to validate the frame.

There are two other sequences which have specific meanings - IDLE and ABORT. The IDLE state is the transmission of at least 15 continuous '1's without inserted zeros. ABORT is 7 to 14 consecutive '1's without inserted zeros sandwiched between two zeros.

FUNCTIONAL DESCRIPTION

The MV6001 consists of four main sections; transmitter, receiver, DMA unit and register bank. Each of the transmitter, receiver and DMA unit have their own clocks running at the required data rates. There are no restrictions on the relative timing between transmit and receive clocks, the DMA clock rate should be greater than ten times the sum of the transmit and receive clock rates.

Transmission

In its steady state the transmitter produces a continuous stream of FLAGS until the control register is loaded with a transmit instruction. The transmitter then, at intervals, requests the DMA unit to fetch a byte of data. This is then transferred from the system memory via the data bus to the transmitter. (If the DMA unit should fail to fetch a byte of data by the time the next request arrives then an under-run will occur and the transmitter will transmit an ABORT sequence). Data is converted into a serial stream with inserted zeros after five ones, and the 16-bit frame check sequence is appended at the end of each frame. As soon as the last bit of the FCS has been clocked out, the $\overline{T_{INT}}$ output goes low to inform the processor that transmission has ended.

INITIALISATION

To start transmission, two items of information are required - the start address for the data to be transmitted, and the length of the user fields are loaded into the TA and TFL registers respectively, after which the transmit enable bit (D_0) can be set at any time to start transmission. Once a transmission has been started, the only way it can by stopped is to set the abort bit (D_1). The transmitter will then transmit the abort sequence followed by flags. Transmitter reset (D_2) resets the transmitter interrupt $\overline{T_{INT}}$, clears the TA and TFL registers and bits D_0 and D_1 of the status register. Transmitter reset is disabled during a transmission.

Interrupt

A transmitter interrupt ($\overline{T_{INT}}$) is generated whenever a transmission ceases, the status register can then be read to check if the frame was aborted or not. The interrupt is reset by writing a transmitter reset to the control register. NB. The status register must be read before a transmitter reset as this will alter the contents of the status register.

Status

The transmitter has two status bits - transmitting data (D_0) and abort (D_1). The transmitting data bit should always be low after $\overline{T_{INT}}$ signifying that transmission is ended. The abort bit will be high whenever a frame is aborted either by an abort instruction to the control register, or internally due to an under-run.

Reception

The receiver accepts serial data, removes inserted zeros and checks the frame check sequence. For each byte of data received, the receiver section generates a DMA request to transfer the data to memory. If the DMA controller fails to make the transfer before the next request from the receiver, then the receiver will drop out and give a receiver interrupt with the code in the status register for overrun. If the number of bytes received reaches the number in the receive maximum frame length register the receiver will drop out and give an interrupt with the code in the status register for frame too long.

Initialisation

The RA register (2 bytes) is loaded with the address where the first received byte of data is to be stored. The RMFL register (11 bits) is loaded with the maximum number of bytes in the user fields plus 3 bytes (+2 bytes for the FCS, +1 byte because an interrupt will occur when the frame length is equal to the length set by the number in the register).

Control

The receiver has two control bits in the control register, receive enable (D_3) and receive reset (D_4). Once the RA and RMFL registers have been loaded, the receive enable bit can be set at any time to allow the receiver to receive a frame. Once set, the receive enable bit cannot be overwritten and receive reset is disabled until a frame has been received.

Receiver reset will reset the R_{INT} interrupt bit, registers RFL, RMFL, RA and bits D_2 - D_7 of the status register.

Interrupt

A receive interrupt ($\overline{R_{INT}}$) is generated whenever a frame is received. The status register can then be read to check the status of the received frame. The interrupt is reset by writing a receiver reset to the control register. Since the reset will clear the receiver bits in the status register, the register must be read before writing the reset to the control register.

Status

The receiver uses bits D_2 - D_7 of the status register (see Figs. 5 and 6). A valid frame is indicated by both 'overrun' (D_6) and 'frame too long' (D_7) bits being high. Following $\overline{R_{INT}}$ the 'free to receive' bit (D_2) should be low, indicating that a frame has been received. The abort, overrun and long frame bits will be set according to the state of the frame received. The flag (D_4) and idle (D_3) bits monitor the incoming signal continuously even when the receiver is disabled.

Frame Length Register

Having received a frame and read the status register, the received frame length can be read from the RFL register. The frame length is given as an eleven bit number and includes the 2 FCS bytes in the count. The register should be read before a receiver reset.

Loopback

Bit D_7 of the control register, the loopback bit is provided for testing purposes. When the bit is set high an internal connection is made between the transmitter output and receiver input. The main transmitter output (TX_{OP}) transmits IDLE (transmitted data is always available on T_{OP2}). The receiver is clocked from TCK. The loopback bit will respond to every write to the control register.

Direct Memory Access (Fig.11)

All data transfers to or from memory are carried out by the DMA controller. Each time it receives a request from the transmitter or receiver it will carry out one DMA cycle, i.e. only one byte is transferred at a time. Clashes between transmitter and receiver are resolved in favour of the receiver, otherwise operation is on a first come, first served basis.

Registers

Fig.7 shows the addresses for the various instruction and status registers. All registers are readable from and writable to except for S, C and RFL. The S and C registers have the same address, which one is accessed is determined by whether a read (status) or write (control) operation is carried out. Transmitter registers should not be written to when transmitting (except to ABORT a frame), likewise receiver registers should not be written to when receiving. The TA and RA registers update continuously during transmission and reception respectively, giving the next address to be read from or written to.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
LOOPBACK ENABLE	DON'T CARE	DON'T CARE	RECEIVE RESET	RECEIVE ENABLE	TRANSMIT RESET	TRANSMIT ABORT	TRANSMIT ENABLE

Fig.4 Control register

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
RECEIVED FRAME TOO LONG	RECEIVED OVERRUN FRAME	RECEIVED ABORT	RECEIVING FLAGS	RECEIVING IDLE	FREE TO RECEIVE	TRANS-MISSION ABORTED	TRANS-MITTING DATA

RECEIVE BITS — TRANSMIT BITS

Fig.5 Status register

Status Register								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Condition
X	X	X	X	X	X	0	1	Currently transmitting data
X	X	X	X	X	X	0	0	Transmitter disabled, transmission COMPLETE (status read after an interrupt)
X	X	X	X	X	X	1	0	Transmitter disabled, transmission ABORTED (status read after an interrupt)
X	X	X	X	X	1	X	X	Receiver enabled, free to receive
X	X	X	0	0	X	X	X	Currently receiving data
X	X	X	0	1	X	X	X	Receiving IDLE
X	X	X	1	0	X	X	X	Receiving FLAGS
0	0	1	X	X	0	X	X	Receiver disabled, ABORTED frame received (status read after an interrupt)
0	1	0	X	X	0	X	X	Receiver disabled, OVERRUN frame received (status read after an interrupt)
1	0	0	X	X	0	X	X	Receiver disabled, TOO LONG frame received (status read after an interrupt)
1	1	0	X	X	0	X	X	Receiver disabled, VALID frame received (status read after an interrupt)

Fig.6 Status conditions

Register	Function	Length (Bits)	Address (Hex)	A_3	A_2	A_1	A_0	R/W
TFL	Transmitter Frame Length LS Byte	8	2	0	0	1	0	R/W
	Transmitter Frame Length MS Byte	3	3	0	0	1	1	R/W
TA	Transmitter Address LS Byte	8	6	0	1	1	0	R/W
	Transmitter Address MS Byte	8	7	0	1	1	1	R/W
S	Status	8	9	1	0	0	1	R
C	Control	8	9	1	0	0	1	W
RFL	Receiver Frame Length LS Byte	8	A	1	0	1	0	R
	Receiver Frame Length MS Byte	3	B	1	0	1	1	R
RMFL	Receiver Maximum Frame Length LS Byte	8	C	1	1	0	0	R/W
	Receiver Maximum Frame Length MS Byte	3	D	1	1	0	1	R/W
RA	Receiver Address LS Byte	8	E	1	1	1	0	R/W
	Receiver Address MS Byte	8	F	1	1	1	1	R/W

Fig.7 Register addresses

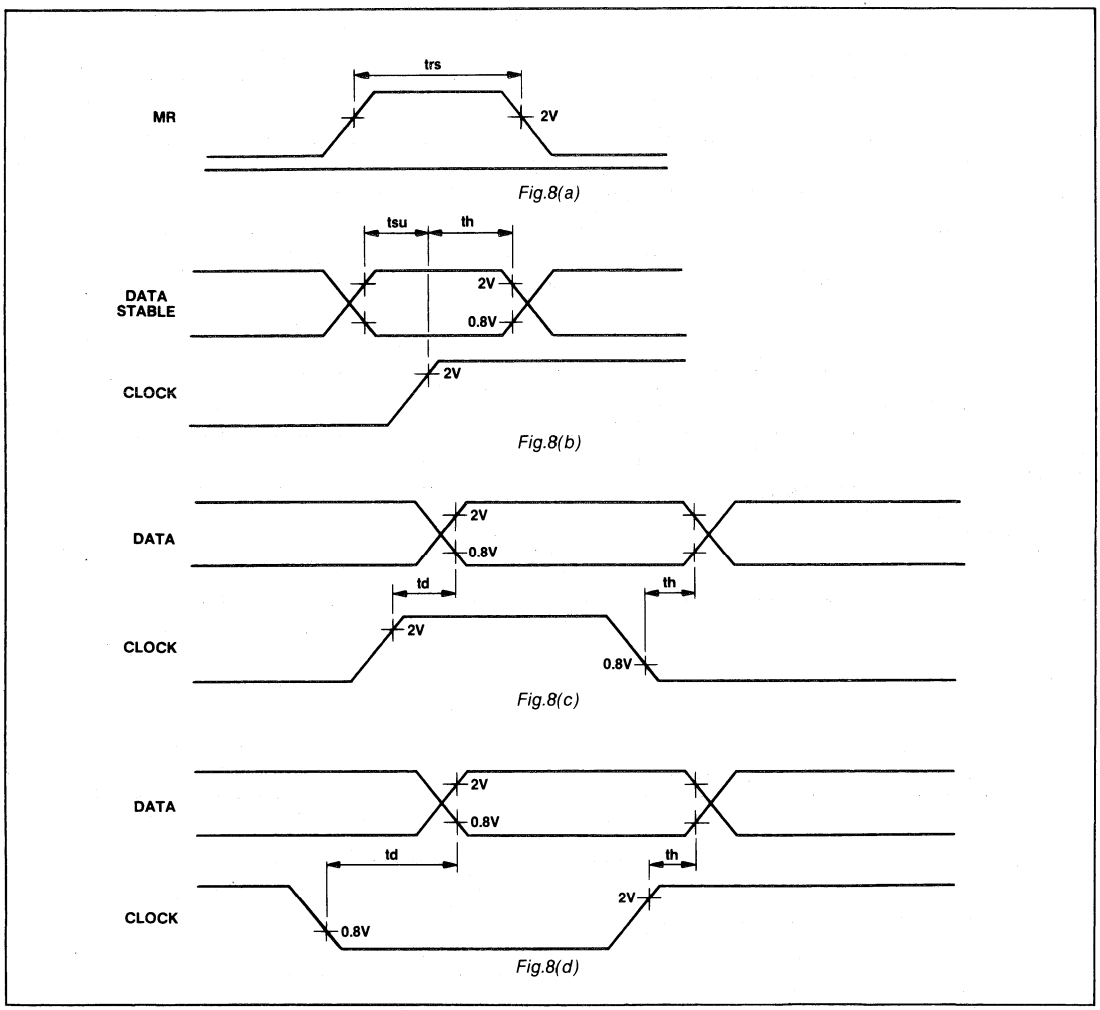


Fig.8 Timing diagram

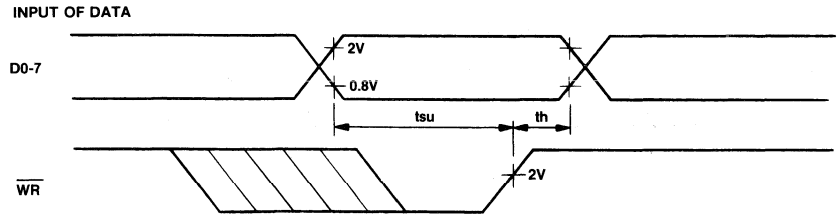


Fig.9(a)

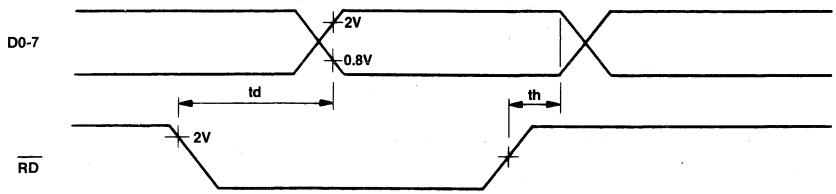


Fig.9(b)

Fig.9 Register timing

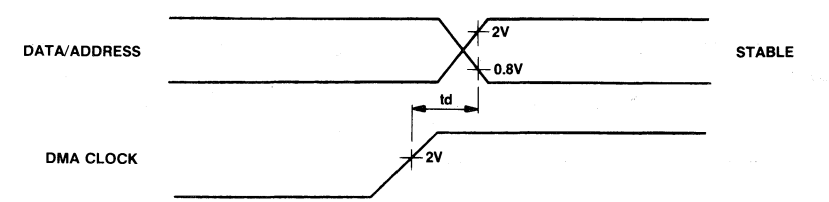


Fig.10 DMA timing

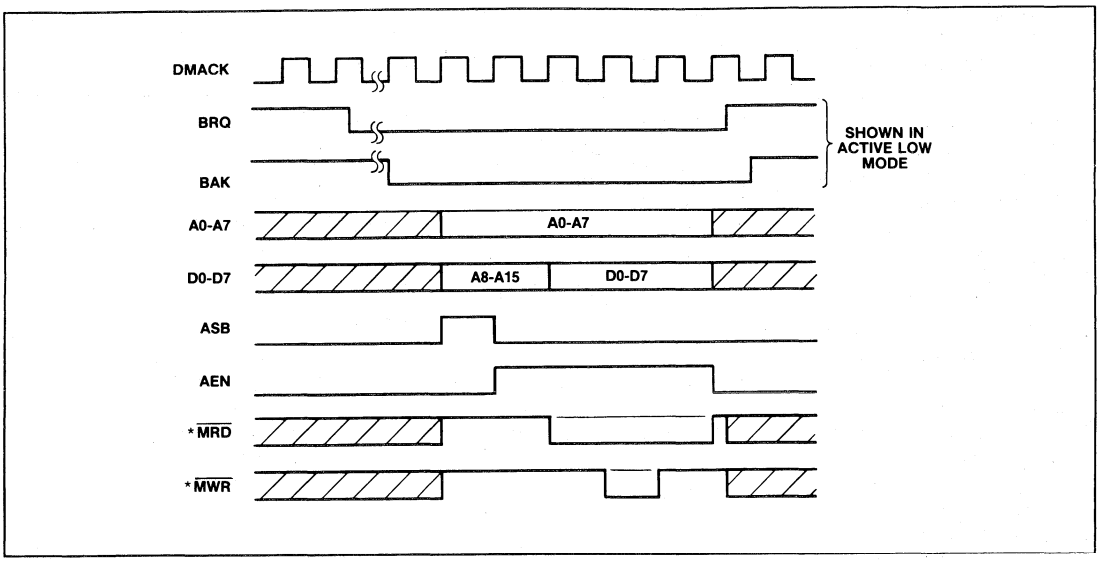


Fig.11 DMA cycle timing

* During a read cycle, $\overline{MWR}$ stays high and similarly during a write cycle $\overline{MRD}$ stays high. All other external signals are the same for both cycles.

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	-0.3V to 7.0V
Input voltage V_{IN}	-0.3V to V_{CC} +0.3V
Output voltage V_{OUT}	-0.3V to V_{CC} +0.3V
Clamp diode current per pin I_K (See Note 2)	±18mA
Static discharge voltage	
Storage temperature T_S	-65°C to +150°C
Ambient temperature with power applied T_{amb}	-40°C to +85°C

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation of 1 second should not be exceeded, only one output to be tested at any one time.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C, V_{CC} = 5.0V ± 10%, Ground = 0V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	V_{CC}-2			V	I_{OH} = 0.8mA
Output low voltage	V_{OL}			0.4	V	I_{OL} = 1.6mA
Input high voltage	V_{IH}	2.2			V	
Input low voltage	V_{IL}			0.8	V	
Input leakage current	I_L	-10		+10	μA	GND ≤ V_{IN} ≤ V_{CC}
V_{CC} current	I_{CC}			1	mA	T_{amb} = -40°C to +85°C
Output leakage current	I_{OZ}	-50		+50	μA	GND ≤ V_{OUT} ≤ V_{CC}
Output S/C current	I_{OS}	15		80	mA	V_{CC} = Max

Switching Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Maximum DMA clock frequency	FDMACK	8			MHz	
Maximum TX clock frequency	FTCK	128			kHz	
Maximum RX clock frequency	FRCK	128			kHz	
Minimum MR duration	t_{rs}				ns	Fig.8(a)
RXIP to RCK set-up time	t_{su}	0			ns	Fig.8(b)
RXIP to RCK hold time	t_h	90			ns	Fig.8(b)
BAK to DMACK set-up time	t_{su}	0			ns	Fig.8(b)
BAK to DMACK hold time	t_h	25			ns	Fig.8(b)
Delay DMA clock to $\overline{MRD}$	t_d		40	55	ns	Fig.8(c)
Delay DMA clock to $\overline{MWR}$	t_d		40	55	ns	Fig.8(c)
Delay RCK ↓ to $\overline{R_{INT}}$	t_d		50	110	ns	Fig.8(d)
Delay, TCK to $\overline{T_{INT}}$	t_d		60	90	ns	Fig.8(c)
Delay, TCK ↓ or RCK ↓ to BRQ	t_d		70	90	ns	Fig.8(c) & (d)
Delay, DMACK to AEN	t_d		40	55	ns	Fig.8(c)
Delay, DMACK to ASB	t_d		40	55	ns	Fig.8(c)
Delay, TCK to TX_{OP}	t_d		70	115	ns	Fig.8(c)
Delay, TCK to T_{OP2}	t_d		60	115	ns	Fig.8(c)
Hold, DMACK to $\overline{MRD}$	t_h		90	130	ns	Fig.8(d)
Hold, DMACK to $\overline{MWR}$	t_h		50	75	ns	Fig.8(d)
Hold, DMACK to BRQ	t_h		60		ns	Fig.8(d)
Hold, DMACK to AEN	t_h		30	55	ns	Fig.8(d)
Hold, DMACK to ASB	t_h		40	55	ns	Fig.8(d)
Data to WR set-up	t_{su}				ns	Fig.9(a)
WR to data hold	t_h				ns	Fig.9(a)
RD to data delay	t_d		50		ns	Fig.9(b)
RD to data hold	t_h				ns	Fig.9(b)
DMACK to data/address delay	t_d		60		ns	Fig.10

DS3139-1.0

SP1404BW, D3702

HIGH VOLTAGE INTERFACE CIRCUIT

The SP1404 is a bipolar integrated circuit comprising five individual digital current amplifier circuits. Each circuit accepts a logic input from TTL, CMOS or a similar source and drives a high-current load at the output. The outputs are capable of withstanding high negative voltages in the 'off' state, making the SP1404 particularly suited to telecommunications applications.

The D3702 is a version of the SP1404BW in 14 pin plastic package approved to BT specification.

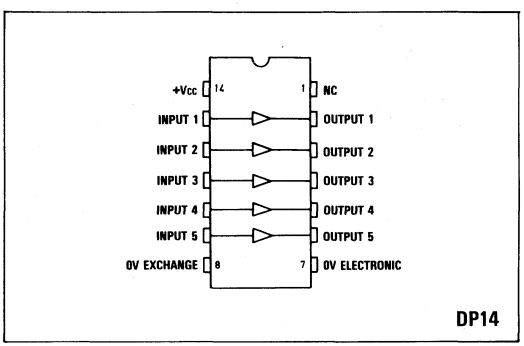


Fig.1 Pin connections (viewed from underside)

CIRCUIT DESCRIPTION (Fig.2)

The SP1404 operates as a power amplifier interfacing from a voltage-level sensitive input to a high-current output switch. The input threshold is TTL-compatible, with a low input current requirement enabling one standard TTL output to drive many interfaces. The low input current requirement also makes it possible to use series current-limiting resistors to protect the SP1404 inputs.

Each element of the device performs as inverting function, i.e. a low voltage level on the input causes a high current in the output. If the input is left open-circuit, the output will be off and the output current will be zero.

The isolation of the integrated circuit is biased to the more negative of the two earth points by diodes D1 and D2 so that differences of up to (V_{CC} - 1) volts can be tolerated between the 'noisy' exchange earth and the 'quiet' electronic earth.

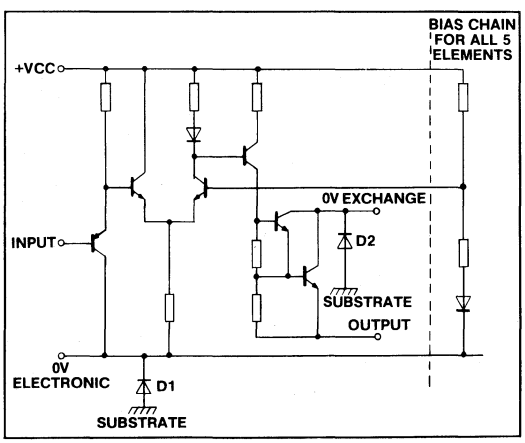


Fig.2 Circuit diagram of one element

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-55°C to +175°C
Chip operating temperature	+150°C
Ambient temperature (I_{OUT} = 50mA)	+85°C
Load current	80mA
Voltage between output and 'noisy earth'	-65V
V_{CC} to output voltage	75V
V_{CC} to electronic earth	7V
Input voltage	V_{CC} + 1V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Temperature range = 0°C to +70°C, V_{CC} = +5V ± 0.5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input current		-20		μA	V_{IN} = 0V
				μA	V_{IN} = V_{CC}
Output voltage			1.5	V	V_{IN} = 0.8V, I_{OUT} = 50mA
Output current (Off state)			100	μA	V_{IN} = 2V, V_{OUT} = -60V
Output current (On state)	50	80		mA	V_{IN} = 0.8V
V_{CC} supply current		30		mA	V_{CC} = 5V, all inputs low
Total power dissipation		450		mW	V_{CC} = 5V, all inputs low
					all outputs I_{OUT} = 50mA

Section 7
Application Notes

An HDB3-Coded PCM Link

This application note shows how the MV1442, MJ1444 and MJ1445 can be used in a 2048kbit/s, HDB3-coded PCM link. It describes the structure of the link, gives an application circuit using the devices and indicates how the circuit can be expanded to include the MV3506 series Codecs.

The 2048bit/s link is that described in CCITT recommendations G.703 and G.732. It is a digital trunk capable of carrying 30 speech channels plus associated signalling and synchronisation. The same link is used as a primary access for ISDN.

STRUCTURE OF THE 2048kBIT/s PCM LINK

The serial structure of the 2048kbit/s PCM link is shown in Fig.1. There are 8 bits in each Time Slot, 32 Time Slots in each Frame and 16 Frames in each Multiframe.

The serial data stream used on the line is HDB3 encoded. This ensures that the clock can be recovered and bit synchronisation established. Frame synchronisation is achieved by Time Slot 0 which contains an alternating signal on bit 2. To avoid accidental synchronisation, a frame synchronisation pattern is used on bits 3 to 8 when bit 2 is zero (see Table 1).

If multiframe synchronisation is required, it is established by four 0's in Time Slot 16 once every 16 Frames (see Fig.3). On the other 15 Frames, Time Slot 16 is used for signalling which avoids four 0's.

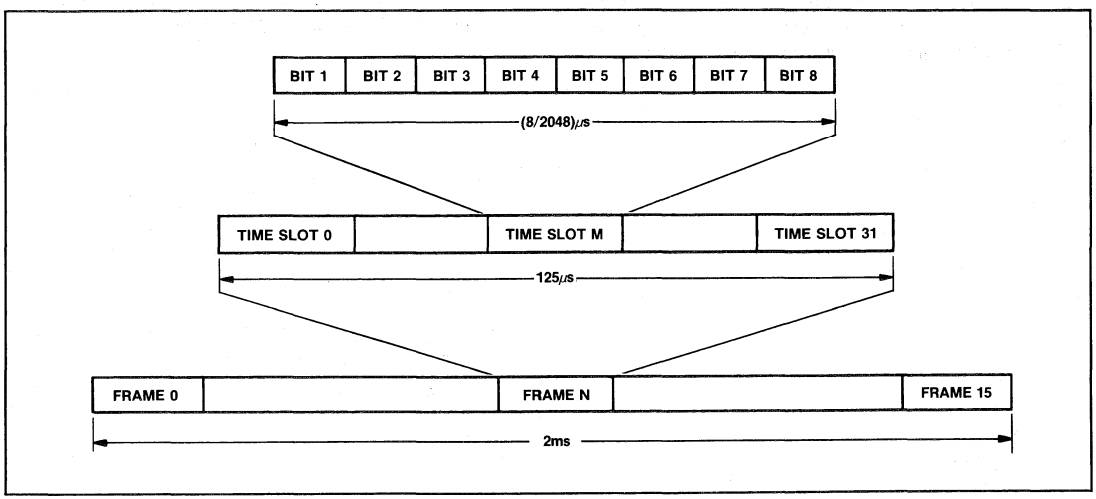


Fig.1 Serial format

	Bit Number							
	1	2	3	4	5	6	7	8
Time Slot 0 in Frame-Alignment Frames	Reserved for International use	0	0	1	1	0	1	1
Time Slot 0 in Non-Frame-Alignment Frames	Reserved for International use	1	Alarm indication to remote multiplexer	Reserved for National use				

Table 1 Bits in Time Slot 0

Frame 0 - Time Slot 16		Frame 1 - Time Slot 16			Frame 15 - Time Slot 16	
0000	XYXX	ABCD for Time Slot 1	ABCD for Time Slot 17		ABCD for Time Slot 15	ABCD for Time Slot 31

Table 2 Bits in Time Slot 16

THE 2048kBIT/s INTERFACE CIRCUIT

Fig.2 shows the interface circuit which is constructed from an MV1442, an MJ1444, and MJ1445 and discrete components at the line interface. The circuit can be used at either the master or the slave end of a phase-locked transmission link or with asynchronous directions of transmission.

Transmit Path

Signalling information for Time Slot 0 is sampled by the MJ1444 and output for multiplexing with PCM data to form the Transmit Data (TD) stream. The MV1442 samples the Transmit Data and outputs HDB3 steering pulses. The line transmit interface accepts the steering pulses, shapes them and couples them through the transmit transformer to generate the differential HDB3 line signal.

Bit and frame synchronisation are established by the Transmit Clock (TC) and Transmit Sync (TS) signals (see Fig.3). **NB** The Transmit Sync does not need to be generated every frame. The Transmit Clock drives the Clock input (pin 4) of the MJ1444 and the Encoder Clock input (pin 2) of the MV1442. The Transmit Sync drives the Channel Reset input (pin3) of the MJ1444.

Some care is required with the transmit transformer. The 5V connection to it must form a good AC ground and capacitive decoupling may be needed to ensure this. Transformer construction details are given in Table 3.

Receive Path

The differential line signal is sensed by the line receive interface which generates steering input pulses for the MV1442. These pulses are used by the MV1442 to generate the Receive Clock (RC) and are decoded according to the HDB3 rules to give the Receive Data (RD). The MJ1445 recognises the frame synchronisation signal on Time Slot 0 of the Received Data and outputs the signalling information.

The MJ1445 also outputs the Receive Sync (RS) signal which bears a similar relationship to Receive Clock and Receive Data as on the Transmit Path (see Figs.3 and 4). **NB** The MJ1445 only outputs the RS signal on Frame-Alignment Frames.

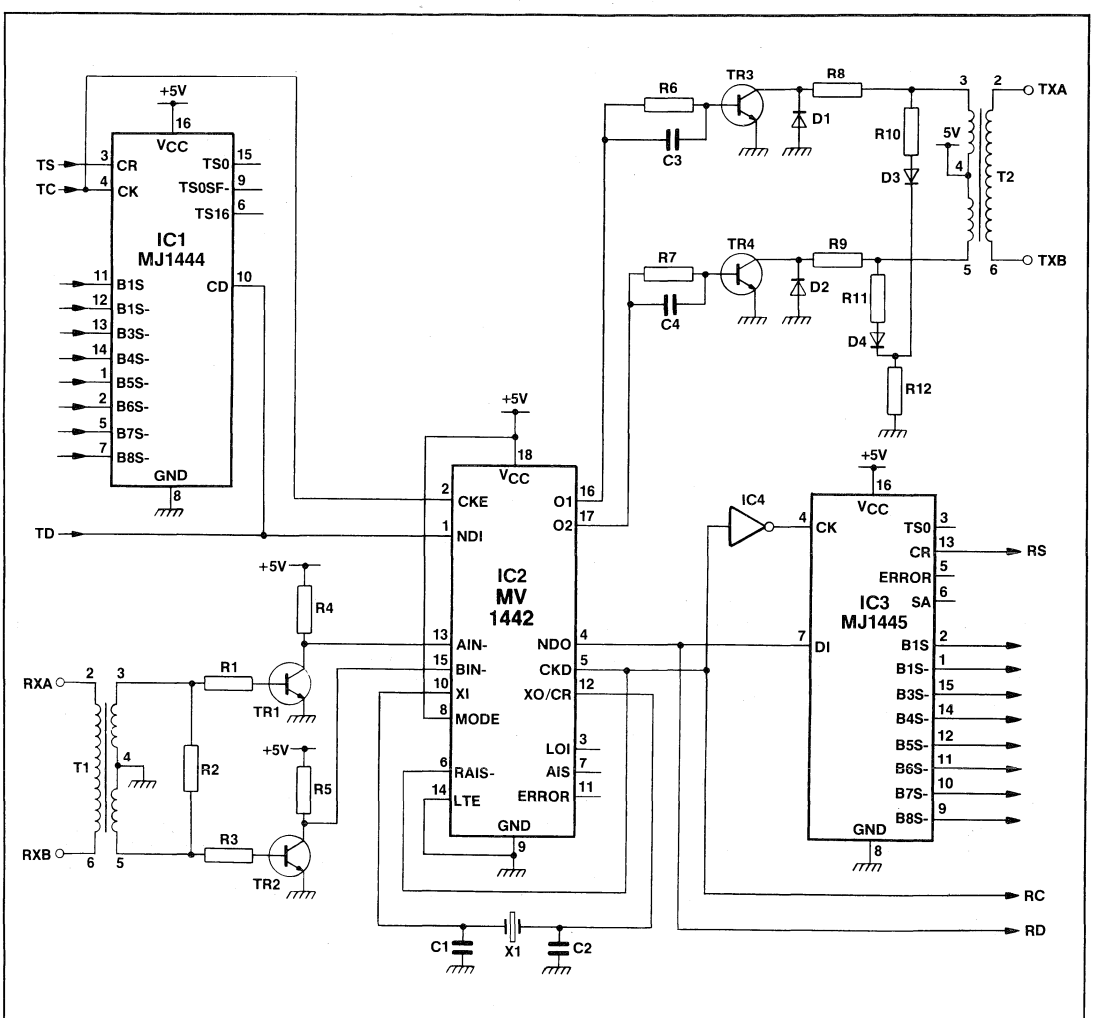


Fig.2 Interface circuit

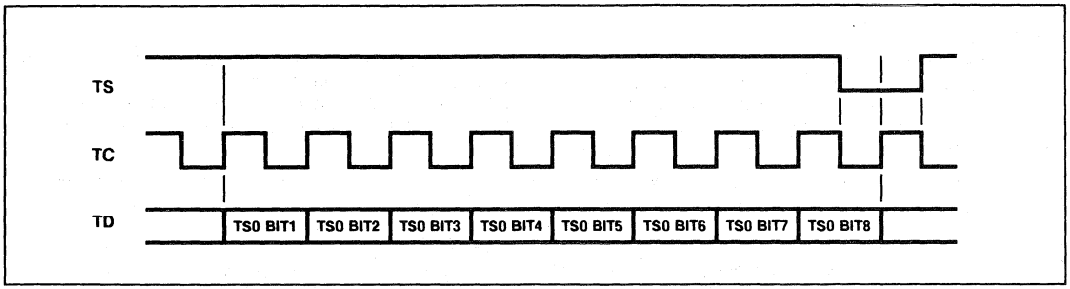


Fig. 3 Transmit signal alignment

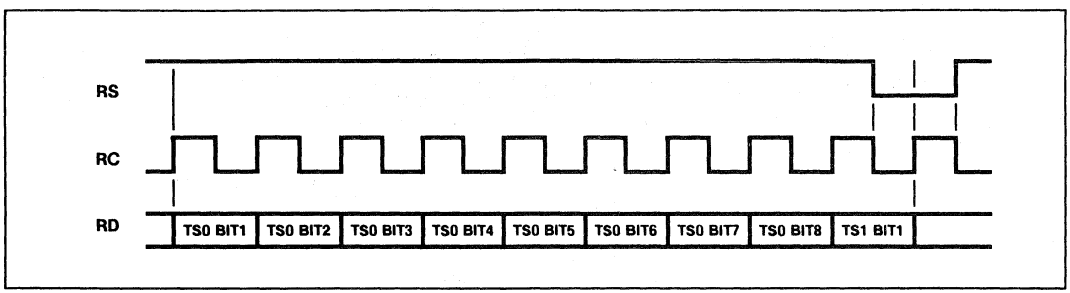


Fig. 4 Receive signal alignment (RS shown for Frame Alignment Frames)

Resistors	**Capacitors**	**Integrated Circuits**
R1 680Ω	C1 22pF	IC1 MJ1444
R2 390Ω	C2 22pF	IC2 MV1442
R3 680Ω	C3 220pF	IC3 MJ1445
R4 1kΩ	C4 220pF	IC4 CMOS inverter
R5 1kΩ	**Transistors**	**Transformer components**
R6 1kΩ	TR1-4 2N2369A	T1 and T2 (each):
R7 1kΩ	**Diodes**	1-off RMS Ferrite pot core assembly
R8 68Ω	D1-4 BAW62	e.g.
R9 68Ω	**Crystal**	1-off B650805-C0000-R030 core
R10 120Ω	X1 16.384MHz	2-off B65806-B2001-X000 clamp
R11 120Ω		1-off B65806-B1001-D001 bobbin
R12 680Ω		For winding details, see text below

Table 3. Interface circuit components list

Transformer winding instructions (contact factory for further details)

1. 40 SWG wire: Start at pin 2
   Wind 36 turns
   End at pin 6
2. Insulating tape: Wind 1 turn
3. Screen: Connect to pin 1
4. Insulating tape: Wind 1 turn
5. 40 SWG wire: Start at pin 3
   Wind 36 turns
   Tap to pin 4
6. Insulating tape: Wind 1 turn
7. 40 SWG wire: Continue from pin 4
   Wind 36 turns
   End at pin 5

EXPANDING THE CIRCUIT

Figs.5 and 6 show how MV3506/7/8 Codecs can be added to the interface circuit. Each Codec receives a transmit and receive strobe which defines its Time Slot. The relationships between the strobes and the signals used by the interface circuit are shown in Fig.7.

The Codecs require their transmit and receive clocks and strobes to be phase-locked with their master clock. Information on this and on the generation of the strobes is contained in the Codec data sheets.

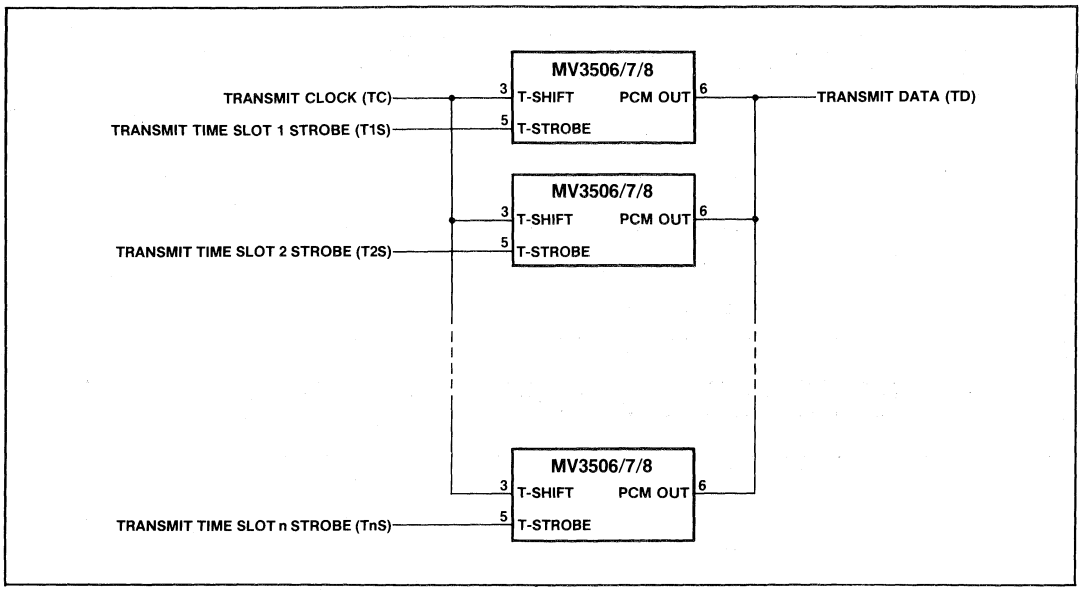


Fig.5 Transmit data from Codecs

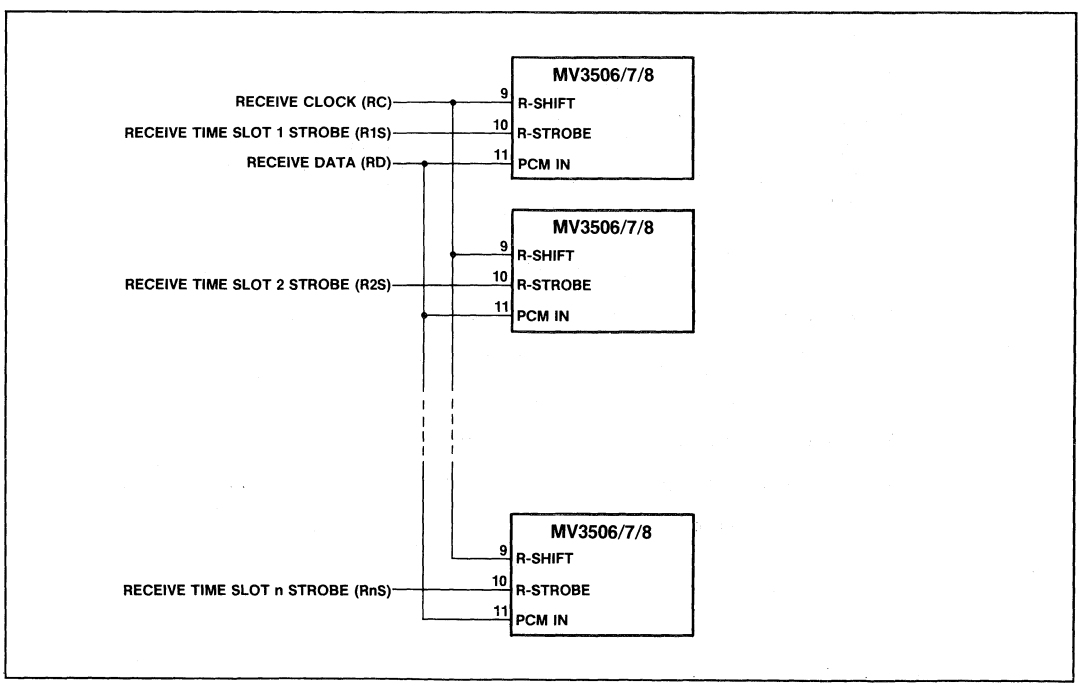


Fig.6 Receive data to Codecs

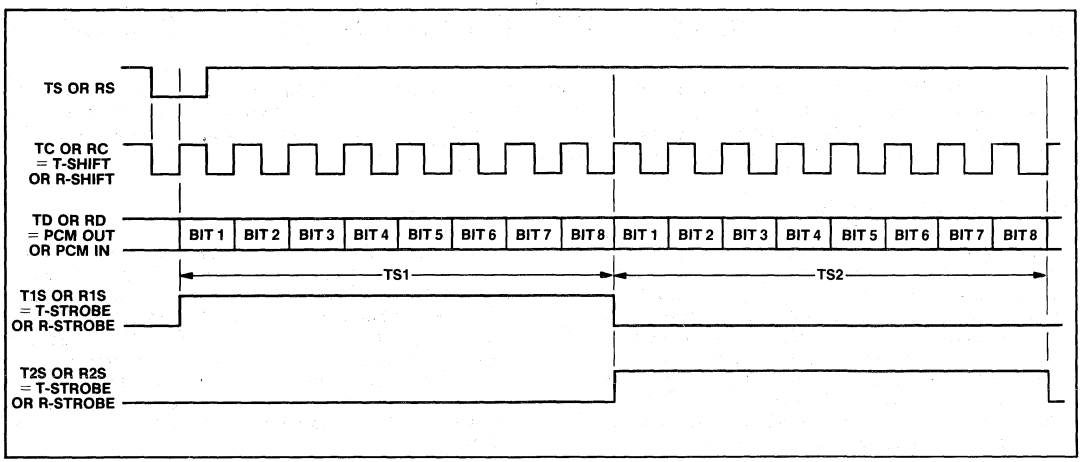


Fig.7 Signal alignment for MV3506/7/8 Codecs

MV1403 PCM Macrocell Evaluation Board AN93

This application note describes the PCBAN93 evaluation board (see page 2-49) for the MV1403 PCM Macrocell demonstrator chip. The board has been designed to allow evaluation of the individual macrocells and to demonstrate how the MV1403, along with external circuitry, may be used to implement a 2.048Mbit PCM link in accordance with CCITT Recommendations G.703, G.704 and G.732.

THE 2.048MBIT PCM LINK

This is a digital trunk capable of carrying 30 speech channels plus associated signalling, synchronisation and error checking. The serial structure of the 2.048Mbit PCM link is shown in Fig. 1. There are 8 bits in each timeslot, 32 timeslots in each frame and 16 frames in each multiframe.

The bits of a timeslot are numbered from 1 to 8, whilst the timeslots per frame and frames per multiframe are numbered from 0 to 31 and 0 to 15 respectively. The serial data stream is HDB3 encoded (CCITT Recommendation G.703), ensuring adequate clock recovery at the receiver.

Frame synchronisation is achieved by the receiver searching for and locking on to the Frame Alignment Signal (FAS), 0011011, present in bits 2 to 8 of timeslot zero during even numbered frames. Such frames are designated sync frames since they contain the FAS. Odd frames are designated non-sync frames. During timeslot zero of non-sync frames, bit 2 is set to '1' to ensure discrimination between sync and non-sync frames, bit 3 is used as a remote alarm bit and bits 4-8 are spare bits which may be used nationally.

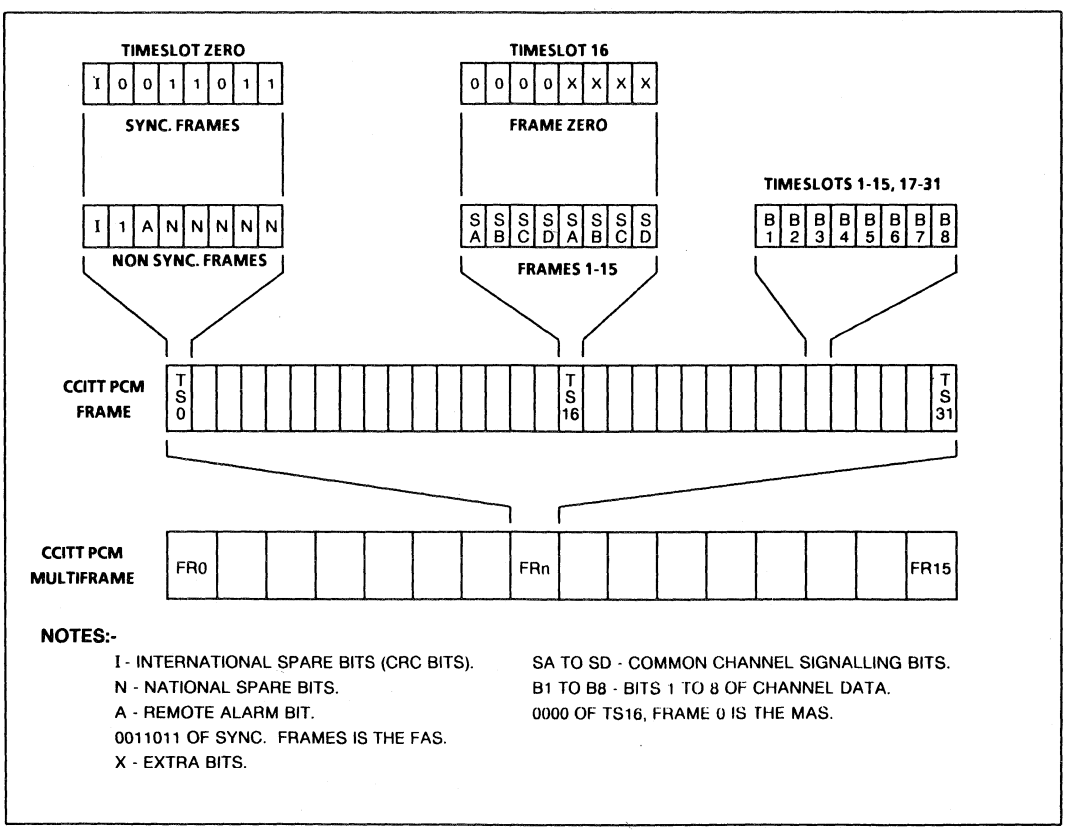


Fig.1 Serial Structure of the 2.048Mbit PCM Link.

Signalling data for the 30 voice channels is transmitted using common channel signalling in Timeslot 16. Multiframe alignment, if required, is achieved by the presence of four 0's, the Multiframe Alignment Signal (MAS), in bits 1 to 4 of timeslot 16 during frame 0. The remaining timeslot 16 in frames 1 to 15 may then be used for signalling by the 30 voice channels.

CCITT Recommendation G.704 describes a possible use for the International spare bits found in the bit 1 position of timeslot 0. Where there is a need to provide additional protection against simulation of the FAS or where there is a need for enhanced error monitoring, then the International spare bit may be used for a Cyclic Redundancy Check procedure. The CRC multiframe consists of two submultiframes, designated SMF I and SMF II, each containing 2048 bits, this being the CRC block size. The 16 frame CRC multiframe structure is not related to the possible use of a multiframe structure implemented within timeslot 16.

During sync frames, bit 1 of timeslot zero contains CRC bits obtained from the previous SMF. There are 4 CRC bits in each SMF, designated C1 to C4. During non-sync frames, bit 1 contains the 6-bit CRC Multiframe Alignment Signal (001011) in frames 1,3,5,7,9 and 11 and 2 CRC error bits (E-bits) in frames 13 and 15, used to indicate the reception of errored submultiframes.

THE MV1403

The MV1403 contains 8 PCM macrocells plus additional circuitry such as the transmission multiplexer and mode selectors to enable it to function as the basis of a 2.048Mbit PCM link or to allow operation of the individual macrocells to be proven. The 8 PCM macrocells are:

- Timeslot Zero Transmitter - TXTSZ
- Timeslot 16 Transmitter - TXTS16
- CRC Generator - CRCGEN
- HDB3 Encoder - HDB3EC
- HDB3 Decoder - HDB3DC
- Timeslot Zero Receiver - RXTSZ
- Timeslot 16 Receiver - RXTS16
- CRC Checker - CRCCHK

Detailed information about the MV1403 demonstrator chip and the individual macrocells can be found in the relevant data sheets, although a brief description of the macrocells is included below.

TIMESLOT ZERO TRANSMITTER

The Timeslot Zero Transmitter macrocell generates the Frame Alignment Signal in accordance with CCITT Recommendation G.704. This is multiplexed together with the other data to be transmitted during timeslot zero and injected on to the PCM highway at the relevant time. In order to do this it requires two timing inputs, a 2.048MHz clock and an active high 8 bit long pulse masking timeslot zero, to enable frame alignment. The latter of these is known as the Frame Sync input, FRS. The data to be transmitted during bits 3 to 8 of non-sync frames is loaded via parallel data inputs, and there is a further input for data to be transmitted during bit 1. The Timeslot Zero Transmitter also produces a timing waveform as output, TZS (Timeslot Zero Sync frame), which is used by other macrocells to determine whether sync frame or non-sync frame data is about to be transmitted.

TIMESLOT 16 TRANSMITTER

The Timeslot 16 Transmitter receives continuous signalling data at 64kbits and converts this into 8-bit packets of data which it transmits at 2.048Mbits during timeslot 16 of successive frames. It again requires a 2.048MHz clock and Frame Sync inputs, and from these it derives its TS16 timing output, which is similar to FRS but masks Timeslot 16.

CRC GENERATOR

The CRC Generator macrocell has two basic modes of operation: CRC mode and non-CRC mode. It has two main external inputs, D1S and D1N, which access the data to be transmitted during bit 1 of timeslot zero for sync and non-sync frames respectively. When in non-CRC mode, the D1S/D1N data is available at the Q output depending upon whether a sync frame or non-sync frame is about to be transmitted, as specified by the TZS input.

When in CRC mode, the CRC generator macrocell has two major functions. One part of the macrocell samples the data being output by the transmission multiplexer during successive submultiframes and from this it derives the CRC word to be output as bit 1 data to the Timeslot Zero Transmitter during the next submultiframe. The second part of the macrocell saves the previously obtained CRC word and outputs this, along with the CRC Multiframe Alignment Signal and D1S/D1N data (for the E-bits of frames 13 and 15 respectively) in accordance with CCITT Recommendation G. 704. This is used as an input to the Timeslot Zero Transmitter. It again relies upon the timing input TZS to do this.

HDB3 ENCODER

The HDB3 Encoder macrocell converts the NRZ data being output from the transmission multiplexer into HDB3 pseudo-ternary format in accordance with CCITT Recommendation G.703, Annex A.

HDB3 DECODER

The HDB3 Decoder macrocell decodes the pseudo-ternary HDB3 inputs to NRZ form. It provides a logical 'OR' of the two inputs as an output to be used by a clock regenerator if required. It also provides two alarm outputs, one for Loss of Input (LIA) and another for a Double Violation on the incoming signal (DV).

TIMESLOT ZERO RECEIVER

The main function of the Timeslot Zero Receiver is to search for and lock on to the Frame Alignment Signal present in the incoming data. The synchronisation/loss of synchronisation process is conducted in accordance with the synchronisation strategy described in CCITT Recommendation G.732. The macrocell produces two timing outputs to the other macrocells, TSZ and TZS. The TSZ (Timeslot Zero) output is similar to the Frame Sync input of the transmitter. The TZS (Timeslot Zero Sync-frame) output is used to determine whether a sync or non-sync frame is about to be received.

The national spare bits from timeslot zero non-sync frames are available as parallel data outputs. The bit 1 data from timeslot zero is also available as outputs Q1S and Q1N. These are obtained according to the CRC mode input, and two timing inputs, FRS13 and FRS15, to enable the two E-bits of a CRC multiframe to be extracted.

In addition, the Timeslot Zero Receiver provides three alarm outputs. The first, ER, denotes that a single erroneous FAS has been received. The second, Sync Alarm (SA), denotes that the receiver is out of synchronisation and the last is the Remote Alarm Indication (RAI), indicating that a remote alarm has been received from the transmitter.

TIMESLOT 16 RECEIVER

The Timeslot 16 Receiver macrocell synchronises to the 2.048Mbit PCM data stream and extracts signalling data during Timeslot 16. This data is stored and then output as a continuous stream at 64kbits.

CRC CHECKER

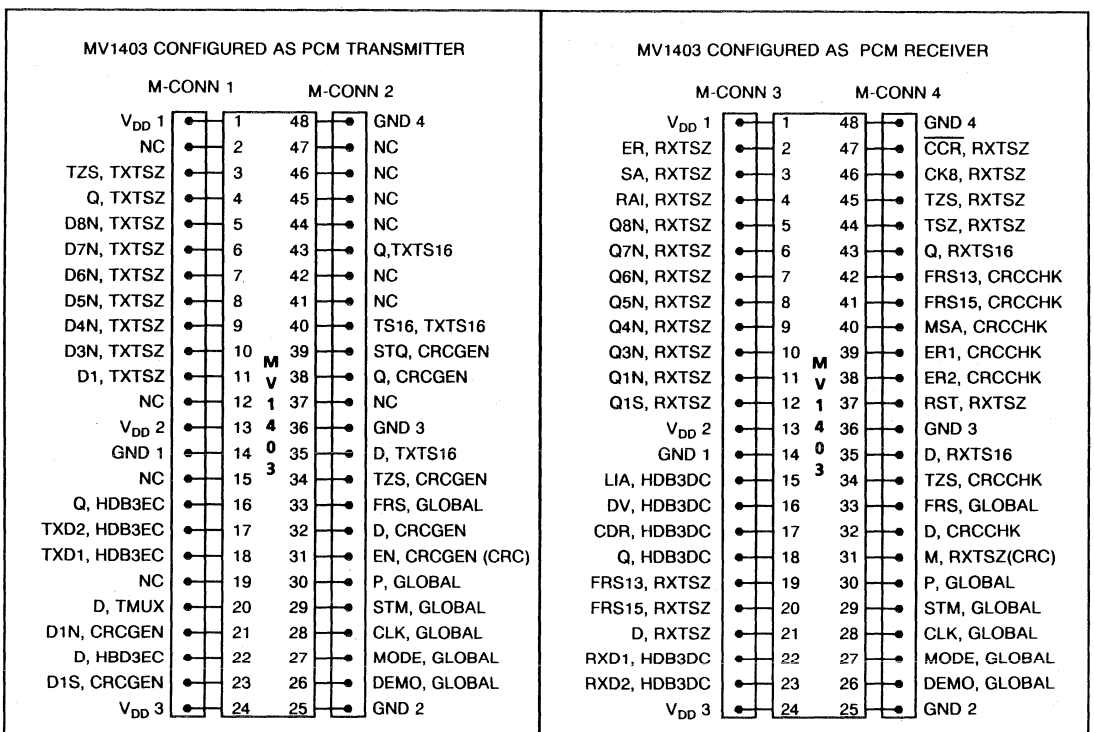
The CRC Checker macrocell has two major functions. One part searches for and locks on to the CRC Multiframe Alignment Signal present in the bit 1, timeslot zero position of non-sync frames. When in sync, the CRC bits are then extracted from bit 1 of sync frames. The second part generates a new CRC word in accordance with CCITT Recommendation G.704 from the incoming data stream and compares this with the CRC bits received in the next submultiframe. The CRC Checker provides three alarm and two timing outputs. The two timing outputs, FRS13 and FRS15, are high during bit 1, timeslot zero of frames 13 and 15 respectively. The Timeslot Zero Receiver uses this information to extract the E-bits of a CRC multiframe.

The three alarm outputs are ER1, ER2 and MSA. The ER1 and ER2 alarms are used to denote that a CRC error has occurred in submultiframe 1 or 2 respectively. The Multiframe Sync Alarm (MSA) indicates that the CRC Checker is out of multiframe alignment.

THE EVALUATION BOARD

MV1403 MODES OF OPERATION

Operation of the MV1403 is controlled by 4 device control inputs: STM, MODE, DEMO and CRC. The STM input is used to put the device in Scan Test Mode and should be tied to ground for normal operation. MODE is used to select whether the device is to be used as either a transmitter or receiver. The MV1403 contains all the macrocells to perform both transmitter and receiver operations but the pin count of the package restricts this to either one function or the other. When MODE is high the device acts as a receiver. The DEMO input selects whether the device is to be used as a system with all the macrocells connected together internally or whether the macrocells are to be accessed individually. When DEMO is high, the device functions as a system. The final control input is CRC. This selects whether or not the device is to be used in CRC generator/checker mode. When CRC is high then CRC generation/checking is enabled.



NOTES: NC - No valid connection in this mode of operation. These pins should be left unconnected.
D, TMUX - This is the speech data input to the transmission multiplexer, which is only used when DEMO is high.

Fig. 2: Macrocell Connector Pinouts.

EVALUATION BOARD OVERVIEW

Due to the package limitations previously discussed, the evaluation board contains two MV1403 devices to provide a useful demonstration, one configured as a transmitter, the other as a receiver. As such the board will demonstrate a 2.048Mbit PCM link in a single direction, although two boards may be connected together to form a bidirectional link. In addition to this, the two control inputs DEMO and CRC are externally selectable by DIL switches.

The other device of importance to be found on the board is an XR-T5683 line interface circuit. This device has three major functions: in the transmit direction it converts the TTL level pseudo-ternary data being output from the PCM transmitter into true ternary data to be output down a transmission line. In the receive direction it converts the ternary data from the transmission line back into TTL level pseudo-ternary data to be input to the PCM receiver and lastly performs clock recovery from the incoming data. These processes are performed in accordance with CCITT Recommendation G.703.

Although both transmit and receive directions are present in the XR-T5683, the two functions are completely segregated internally with separate power supplies for the two directions. The board is thus split into two halves, one being the PCM transmitter, the other the PCM receiver. The only common parts are the XR-T5683 interface circuit and the power supply. The board only requires a single +5 Volt supply and will draw approximately 600mA.

To enable access to the individual macrocells, a pair of 0.1 inch pitch 24 way PCB headers are connected to each of the two MV1403s (M-CONN 1-4). The pin layouts of these connectors are shown in Fig. 2 but are only valid when the DEMO mode input is low. When DEMO is high, some of the input pins will no longer have any function since they will be connected internally to the outputs of other macrocells.

The remainder of the evaluation board consists of additional circuitry such as a clock generator to enable the board to function as a useful demonstrator, with as much flexibility as possible. The HDB3 inputs/outputs are accessed via BNC connectors for 75 Ohm unbalanced operation whilst other connections such as an external clock are made via 0.1 inch pitch PCB headers. The position of all connectors, switches and other major components is shown in Fig. 7.

TRANSMITTER CIRCUIT

A full circuit diagram of the transmitter half of the evaluation board, excluding macrocell connectors, is given in Fig. 3. The operation of the transmitter is selectable via two DIL switches (half of SW1-4) to set DEMO (labelled DEMO MODE) and CRC (CRC EN). A further 8 DIL switches (SW5-12) are used to set the user data inputs D1S, D1N and D3N to D8N which are to be inserted into the spare bits of timeslot zero. No external pull-up resistors are required on these pins since all input pins of the MV1403 have internal 100kOhm pull-up resistors.

To enable flexible operation, the transmitter circuit has an on board 2.048MHz clock generator centred around the 74LS321 crystal controlled oscillator circuit. Alternatively, an external 2.048MHz clock may be used, the internal/external clock option being selected by a further DIL switch (INT CLK) driving tristate buffers. Both the external clock input and the clock output along with other connections are accessed via the 0.1 inch pitch PCB connector, TX-CONN.

As well as being used as an input to the PCM transmitter and line interface circuit, the clock is also input to an 8-bit counter, the 74LS590. This counter and associated decoder circuitry are used to derive the FRS signal, an 8-period high-going periodic pulse used to mask timeslot zero. An external FRS input is also available, the option being selected by a final DIL switch (INT FRS).

A final timing output, high during bit 1 of timeslot zero, is also decoded from the counter. This may be used to synchronise codecs requiring a single period pulse at the start of timeslot zero. This output is only valid when the on-board FRS is selected.

The two serial data inputs, one for the 2.048Mbit speech data, the other for the 64Kbit signalling data, may also be accessed by the same connector, as well as by the macrocell connector. An inverter is required between the clock signal driving the MV1403 and that driving the transmitter half of the XR-T5683 (the line interface circuit). This clock inversion is necessary since the XR-T5683 requires that its inputs be active during the high half cycle of clock, whereas the pseudo-ternary outputs of the MV1403 are active during the low half cycle of clock.

LINE INTERFACE CIRCUIT

A full circuit diagram of the line interface portion of the evaluation board is included in Fig. 4. This circuit is built around the XR-T5683 line interface circuit. As mentioned previously, this device consists of separate transmit and receive sections.

The transmitter half of this device accepts the incoming pulses, shapes them in accordance with the pulse mask specified in CCITT Recommendation G. 703 and couples them through the transmit transformer, T1, to generate the differential HDB3 line signal. Depending upon the position of wire link 1, the differential voltage produced by the transformer is used to drive either an unbalanced 75 Ohm co-axial output or a balanced 120 Ohm twisted-pair output (P-CONN1). Different feed resistor values (39 Ohm for 2.37V into 75 Ohm, 30 Ohm for 3.0V into 120 Ohm) are also required to produce the correct peak pulse voltage, as specified in CCITT Recommendation G.703. The winding instructions of both the transmit and receive transformers are given at the end of this application note.

On the receive side, either the 75 Ohm unbalanced input or the 120 Ohm balanced input (P-CONN2) is connected across the primary of the receive transformer, depending upon the position of wire link 2. The voltage thus produced on the centre tapped secondary of the receive transformer is fed into the XR-T5683. This converts the received ternary HDB3 pulses back into pseudo-ternary TTL level data to be output to the PCM receiver circuitry. The remainder of the circuitry is associated with the clock recovery circuit of the XR-T5683. This consists of the tuned circuit connected between pins 4 and 6 of the XR-T5683 and decoupling between pin 6 and ground. The clock recovery circuit of the XR-T5683 is not self resonant. The received data pulses are used to set the tuned circuit oscillating, after which the circuit will continue to ring for a number of cycles if no data pulses are subsequently received. The XR-T5683 converts these oscillations in to a TTL level clock and outputs this signal to the remainder of the receiver circuitry.

RECEIVER CIRCUIT

A full circuit diagram of the receiver circuitry excluding macrocell connectors is included in Fig. 5. As with the transmitter, the operation of the receiver is selectable via two DIL switches (half of SW13-16) used to set DEMO (DEMO MODE) and CRC. In addition, a momentary action push switch (SW17, RX RESET) is included to reset the Timeslot Zero Receiver if required.

The timeslot zero spare bit outputs, Q1S, Q1N and Q3N to Q8N are buffered by the 74LS541 and are then input to a ULN2803 darlington driver. The open collector outputs of the ULN2803 are then used to drive 8 LEDs to display the data being received in the spare bits. The 8 alarm outputs are fed into the error latch sub-circuit, the diagram of this being shown in Fig. 6. The outputs from this circuit are fed into a second ULN2803 to drive a further 8 LEDs, giving a visible indication of any alarms.

The error latch sub-circuit has a control input, LATCH-EN, to enable latching of the alarms. This input is selected by a DIL switch (ER-LATCH, Fig. 5)). When LATCH-EN is high a single period alarm will be latched and as such will be visible on the LEDs. When LATCH-EN is low, all alarms will just be buffered and not affected in any other way. A momentary action push switch (SW18, ERROR LATCH RESET) can be used to reset any latched alarms.

The circuitry around the 74LS74 (Fig. 5.) is used to derive the bit 1, timeslot zero timing output from the timeslot zero output of the PCM receiver. The inverted timeslot zero output is used to preset the D-type latch, the output from which is then used to set the S-R latch, thus disabling further presets. On the next positive clock edge a logic '0' is clocked in to the D-type latch, thus giving a single period high going pulse. The low going edge of timeslot zero is then used to reset the S-R latch to enable the next preset. This output may be used to synchronise Codecs requiring a single period Frame Sync input.

This bit 1, timeslot zero output, along with TSZ, the 2.048MHz receiver clock, the 2.048Mbit data output and the 64Kbit timeslot 16 data output are all accessed via a 6-way 0.1 inch pitch PCB header, RX-CONN.

Transformer Components (Fig. 4)
T1 and T2 (each)

1 - off RM5 Ferrite pot core pair e.g Philips type 4322-022-59900 (similar to old type LA1577).

1 - off RM5 6 pin bobbin.

2 - off RM5 clamp.

For winding details, see winding instructions opposite.

Transformer Winding Instructions

1. 35/36 SWG wire: Start at pin 3, wind 22 turns, tap to pin 4.
2. Insulating Tape: Wind 1 turn.
3. 35/36 SWG wire: Continue from pin 4, wind 22 turns, end at pin 5.
4. Insulating Tape: Wind 1 turn.
5. 35/36 SWG wire: Start at pin 2, wind 22 turns, end at pin 6.

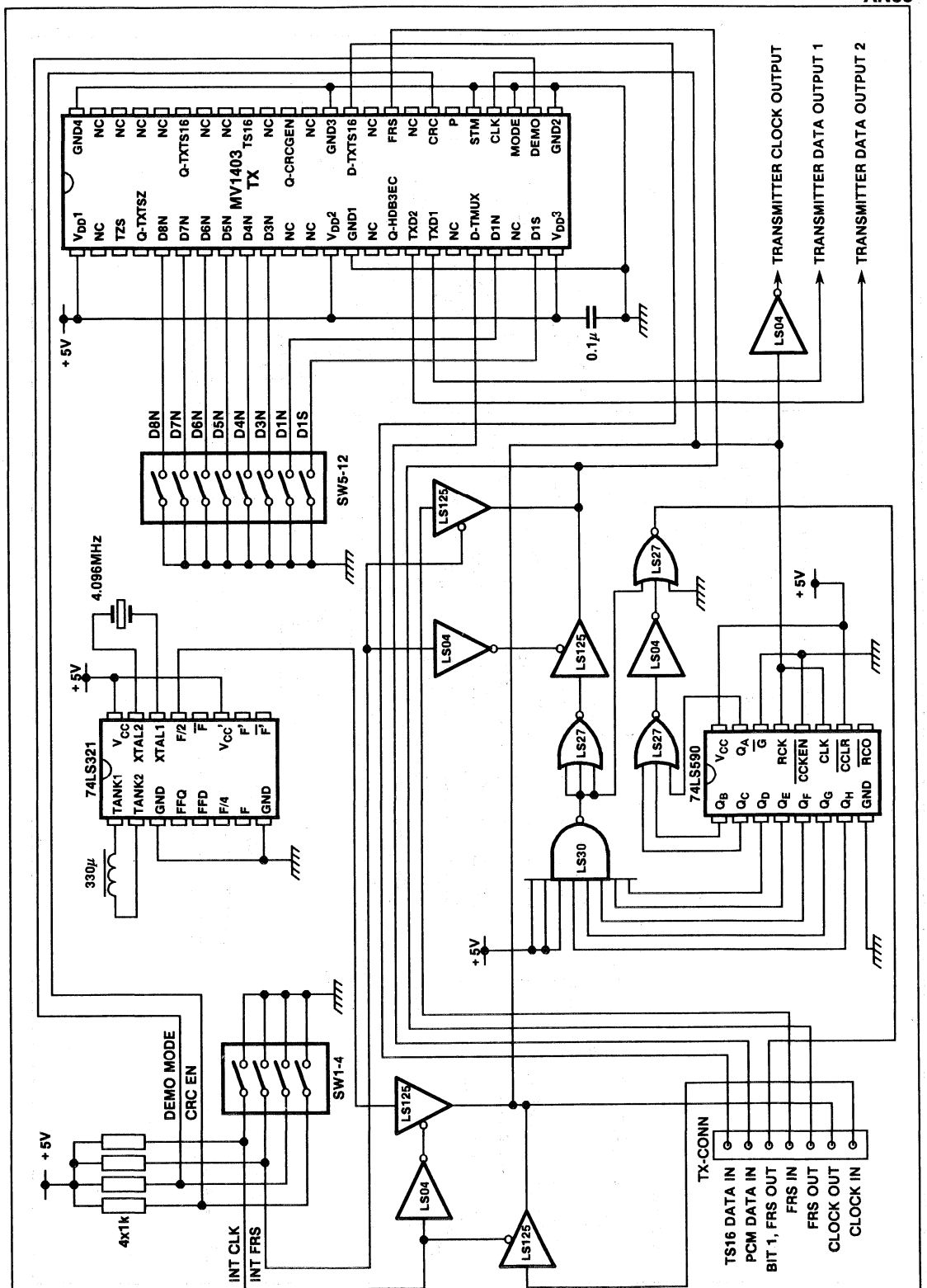


Fig.3 PCM Transmitter circuit diagram

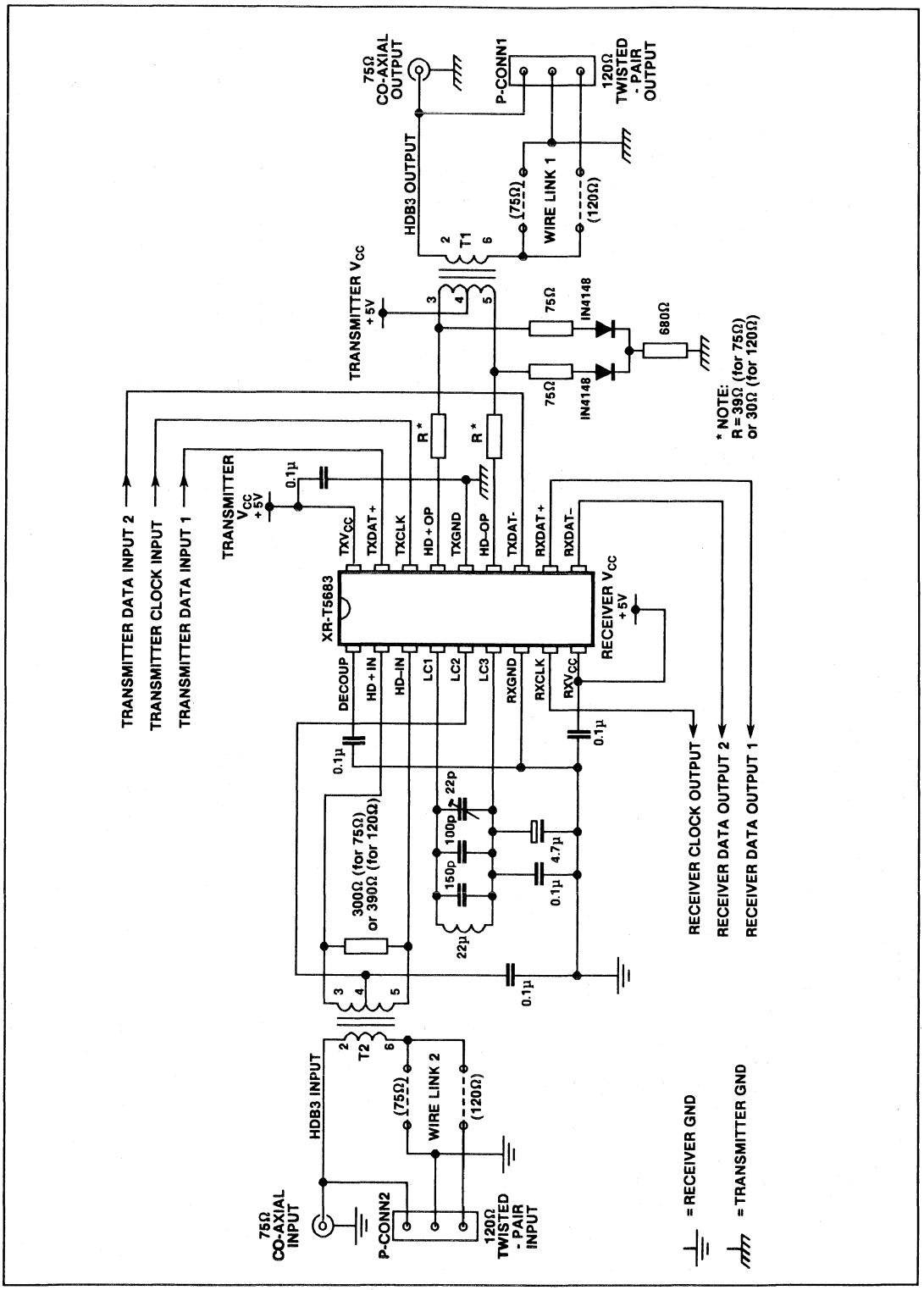


Fig.4 PCM line interface circuit diagram

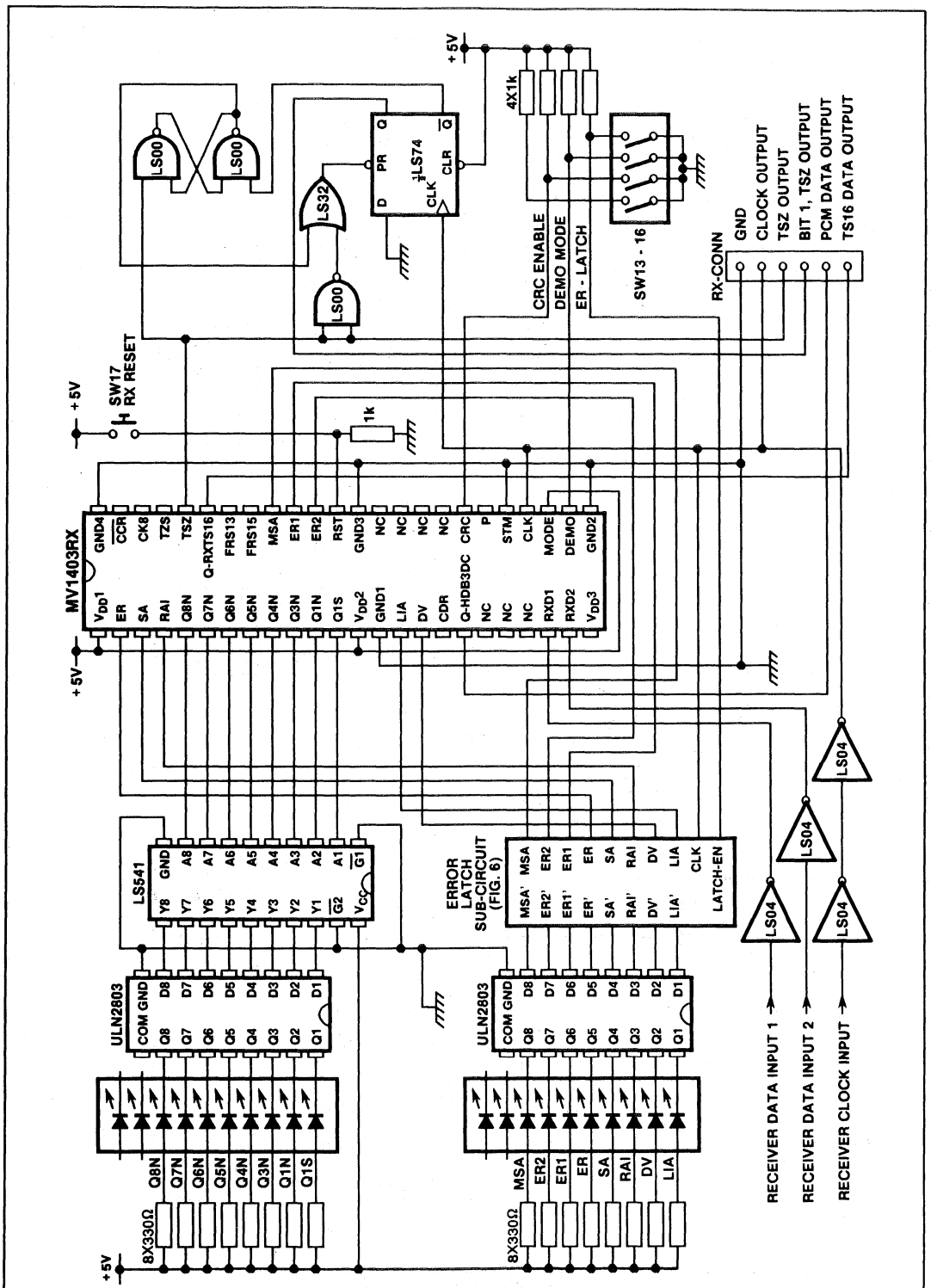


Fig.5 PCM Receiver circuit diagram

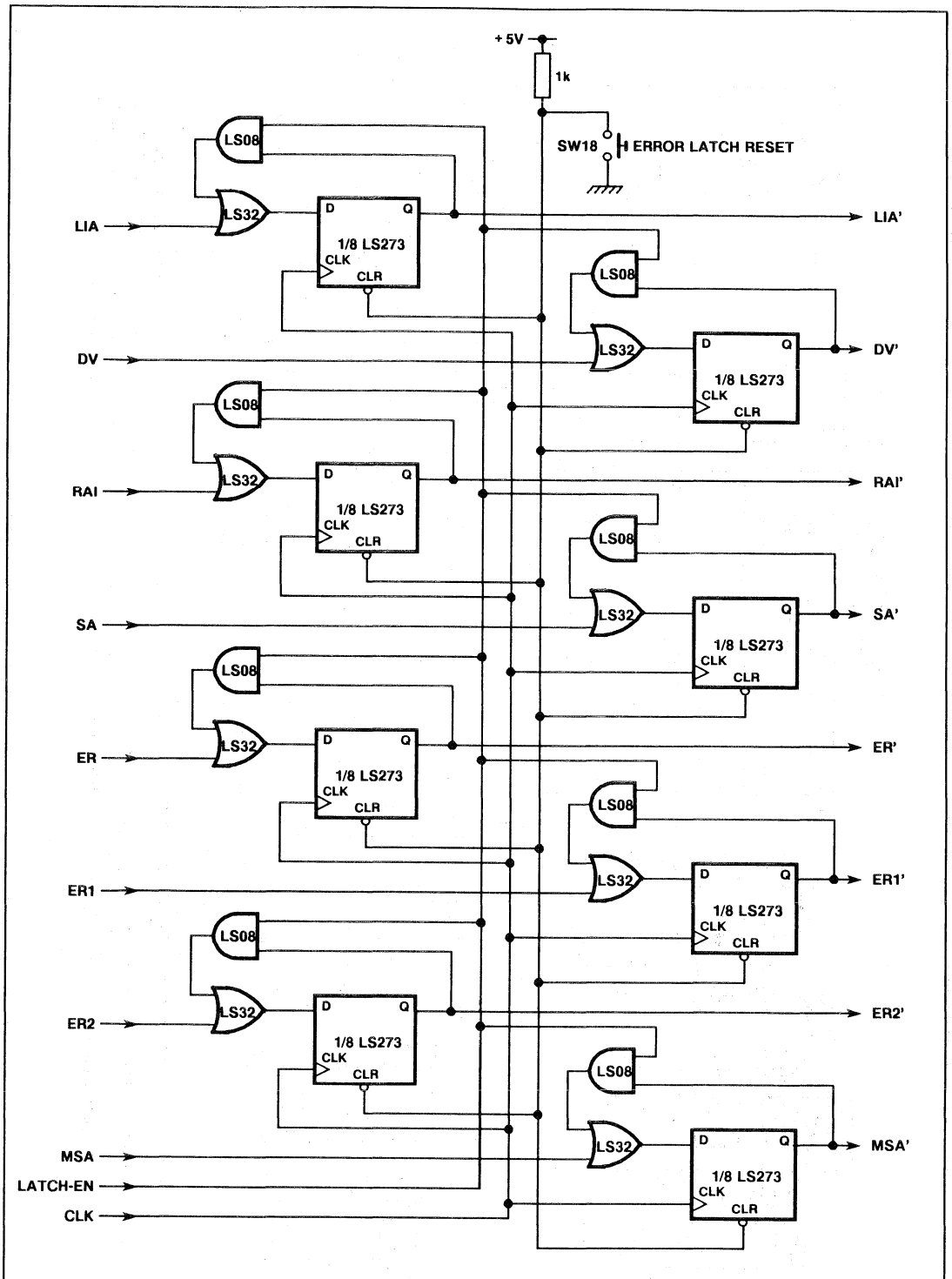
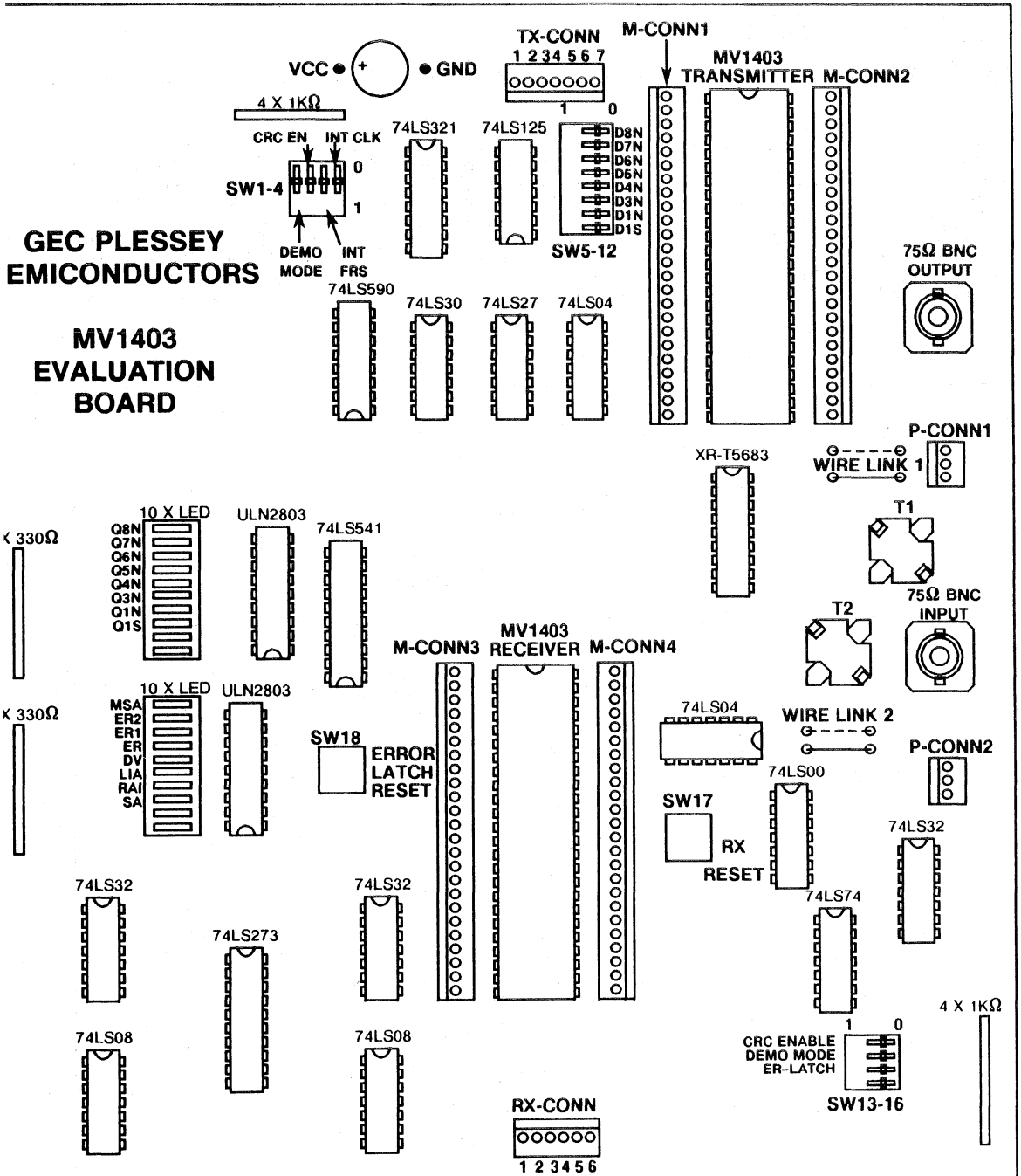


Fig. 6 Error Latch Sub-circuit.



TX-CONN PINOUT

1	CLK I/P	5	BIT1, FRS
2	CLK O/P	6	PCM DATA I/P
3	FRS O/P	7	TS16 DATA I/P
4	FRS I/P		

RX-CONN PINOUT

1	TS16 DATA O/P	4	TSZ O/P
2	PCM DATA O/P	5	CLK O/P
3	BIT1, TSZ	6	GND

Fig. 7 Evaluation board layout - main components.

SL373/SL376
Subscriber Line Interface Circuits

AN82

The GEC Plessey Semiconductors SL373 and SL376 are both Subscriber Line Interface Circuits (SLICs) designed to interface a subscriber line to a Public Switched Telephone Network or that of a PABX. Each device allows all the AC and DC conditions to be programmed according to the required application. The individual data sheets for each device give information on functionality and electrical parameters and are included in Section 3 of this handbook.

This Application Note is intended to complement the SL373 and SL376 data sheets, to give further application information and circuit details and to highlight the difference between the two SLICs. Finally, it may also prove useful to refer to the GEC Plessey Semiconductors MV3010 Subscriber Line Audio Circuit (PSLAC) data (see pages 3-135 to 3-173). This is a complementary device that supports a complete line card design, in conjunction with a SLIC.

CONTENTS

INTRODUCTION

When used in a system, both the SL373 and SL376 SLICs provide the designer with a number of operating modes for system flexibility. This section discuses these modes and highlights the nature of the two devices.

Firstly, both SLICs provide an Active and a Standby Mode with normal LA/LB (i.e. Tip/Ring) or reversed polarity. For normal polarity, the LA pin is positive and for reverse it is negative. Apart from DC line polarity, the normal and reverse Active Modes are identical. This is also true of the normal and reverse polarity Standby Modes.

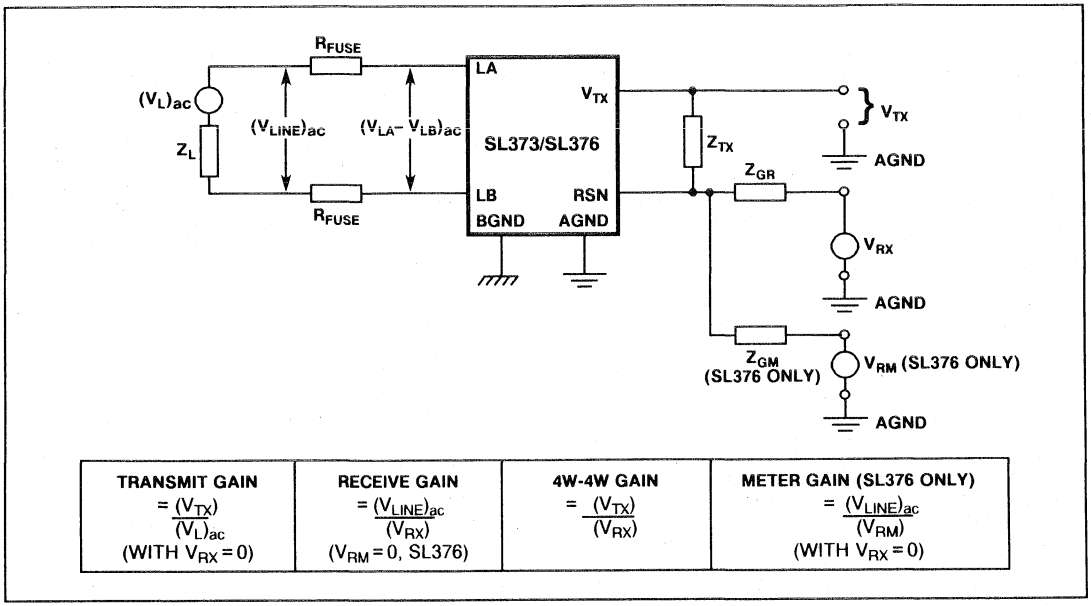
For most of the time, the served subscriber that is connected to the SLIC, will be On-Hook. Both of the SLICs provide a low power Standby Mode of operation keeping power consumption/dissipation by the SLIC to a minimum. It is intended that this Standby mode will only be used during On-Hook conditions. Note that the implementation of Standby is different for the two SLICs. Additional power saving is available by use of the SL376, which turns off the Voltage Regulator during Standby Mode. However, the Regulator is designed to limit power dissipation by the device by matching the required 2 wire DC voltage to the supplied regulator voltage. The difference between the battery and regulator voltages will be larger at lower line resistances, i.e. Off-Hook. If the SL376 thus remains in Standby Mode when the subscriber has gone Off-Hook, then a significant amount of power dissipation may occur because the Regulator (in Standby) is inoperative. This will not normally be a problem, since under all normal conditions the system will change the SLIC operating mode to Active, turning on the Voltage Regulator. It is therefore important that the system ensures the SL376 does not remain in Standby mode for Off-Hook status, excepting a short period before this condition is first recognised. Note that since the SL373 Voltage Regulator is always operative, then the above constraint does not apply and that the SL376 Standby power dissipation will for most times be greater than the SL373.

Once Off-Hook has been detected, then the SLIC should be put into Active Mode. This brings to light a second difference between the two SLICs. That is, the SL373 is a constant current feed device at low line resistance, whilst the SL376 is a resistive feed function. Both devices, however, have a constant voltage region (between pins LA and LB) at high line resistance. Setting up the parameters relating to Standby and Active Modes is fully described in the respective Data Sheets, with further information given in the Hardware Programming of SLIC Parameters section of this Applications Note.

Both SLICs contain a Ring Relay Driver. The nature of the driver is different for each SLIC, as described in the related Data Sheet. The SLIC can be placed in Ringing mode via the Digital Interface, activating the Ring Relay Driver and setting the SLIC to determine Ring Trip. For this mode, DC and AC ringing supply voltages are external to the SLIC, which may be Balanced or Unbalanced in nature, as described in the Ring Trip Circuits section.

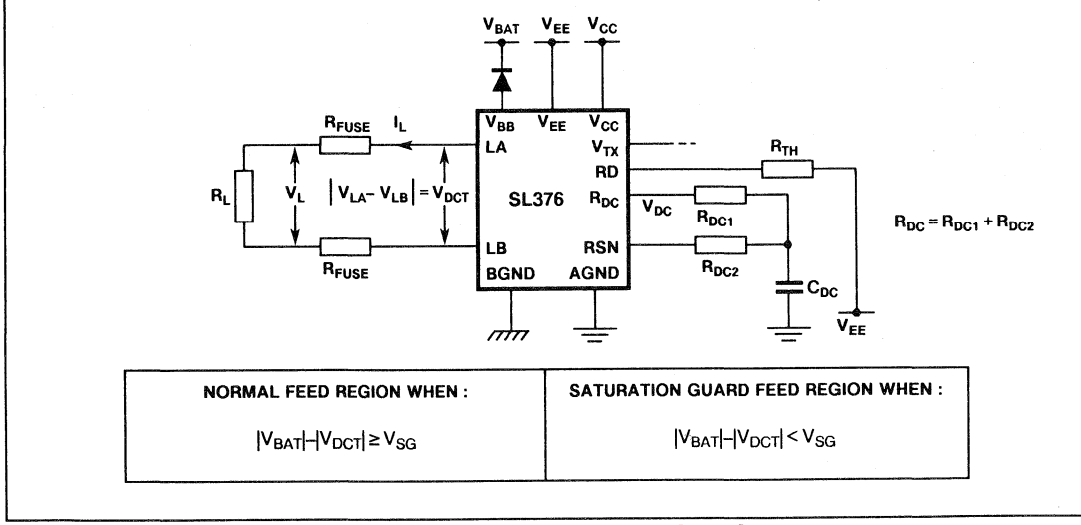
Other modes of operation are possible with each SLIC allowing the Line Card to be set to determine Ground Start conditions in Disconnect A Standby B Mode. This disconnects the A Leg from the line whilst the B leg is in Standby. Additionally, both SLICs can be placed in Disconnect Mode, which isolates the LA and LB pins from the Line (high impedance). Finally, the SL373 has one additional mode whereby a second relay can be activated, for example, to facillitate Test Access.

All the modes and SLIC functions as mentioned are fully described in the separate data sheets of the SL373 and SL376. For reference purposes, Figs. 1 and 2 provide a ready guide for the parameters used on these data sheets and in this document. Also, to assist circuit design, all of the major circuit equations to determine operating parameters are summarised in Table 1.



TRANSMIT GAIN	RECEIVE GAIN	4W-4W GAIN	METER GAIN (SL376 ONLY)
$= \frac{(V_{TX})}{(V_L)_{ac}}$ (WITH $V_{RX} = 0$)	$= \frac{(V_{LINE})_{ac}}{(V_{RX})}$ ($V_{RM} = 0$, SL376)	$= \frac{(V_{TX})}{(V_{RX})}$	$= \frac{(V_{LINE})_{ac}}{(V_{RM})}$ (WITH $V_{RX} = 0$)

Fig.1 AC parameters and components for SL373/SL376.



NORMAL FEED REGION WHEN :	SATURATION GUARD FEED REGION WHEN :
$\lvert V_{BAT}\rvert - \lvert V_{DCT}\rvert \geq V_{SG}$	$\lvert V_{BAT}\rvert - \lvert V_{DCT}\rvert < V_{SG}$

Fig.2 DC parameters and components for SL373/SL376

HARDWARE PROGRAMMING OF SLIC PARAMETERS

The SL373 and SL376 Data Sheets describe the internal circuitry for controlling the SLIC operating characteristics. The relationships for calculating the component values that determine these are summarised in Table 1. To illustrate the hardware programming of these characteristics, this section presents a typical example for each SLIC of a line card design requirement.

SL373 - DC	SL376 - DC
Active Mode : Normal Region $I_L = I_{FEED} = \frac{2500}{R_{DC}}$	Active Mode : Normal Region $R_{FEEDTOT} = 2R_{FUSE} + \frac{R_{DC}}{50}$
Active Mode : Saturation Guard Region $I_L = \frac{(\lvert V_{BAT}\rvert - V_{SG})}{R_L + 2R_{FUSE}}$	Active Mode : Saturation Guard Region $I_L = \frac{(\lvert V_{BAT}\rvert - V_{SG})}{R_L + 2R_{FUSE}}$
Standby Mode (Until Saturation Guard Region) $I_L = I_{LIM} = \frac{K_{LIM} \times 350}{R_{TH}} \sim \frac{600}{R_{TH}}$	Standby Mode (Until Saturation Guard Region) $I_L = I_{LIM} = \frac{K_{LIM} \times 350}{R_{TH}} \sim \frac{600}{R_{TH}}$
Active Mode Saturation Guard Threshold at:- $R_L = R_{LSG} = \frac{R_{DC}(\lvert V_{BAT}\rvert - V_{SG})}{2500} - 2R_{FUSE}$ such that $V_L = V_{LSG} = \lvert V_{BAT}\rvert - V_{SG} - \frac{2500 \times 2R_{FUSE}}{R_{DC}}$	Active Mode Saturation Guard Threshold at :- $R_L = R_{LSG} = \frac{R_{DC}(\lvert V_{BAT}\rvert - V_{SG})}{50(50 + V_{SG} - \lvert V_{BAT}\rvert)} - 2R_{FUSE}$ such that $I_L = I_{LSG} = \frac{50\,(\,50 + V_{SG} - \lvert V_{BAT}\rvert\,)}{R_{DC}}$
Off Hook Threshold at :- $I_L = I_{DET} = 350 \div R_{TH}$	Off Hook Threshold at :- $I_L = I_{DET} = 350 \div R_{TH}$
$V_{SG} = 15V$	$V_{SG} = 16.5V$
SL373 - AC	**SL376 - AC**
2 Wire Voltage Active Mode, Receive only $(V_{LINE})_{ac} = \frac{-V_{RX}\,\alpha\,(Z_L)\,Z_{TX}}{[\,\alpha\,(Z_L + 2R_{FUSE}) + Z_{TX}\,]\,Z_{GR}}$	2 Wire Voltage Active Mode, Receive only $(V_{LINE})_{ac} = \frac{-V_{RX}\,2\,\alpha\,(Z_L)\,Z_{TX}}{[\,\alpha\,(Z_L + 2R_{FUSE}) + 2Z_{TX}\,]\,Z_{GR}}$
$(V_{LA}-V_{LB})_{ac} = \frac{-V_{RX}\,\alpha\,(Z_L + 2R_{FUSE})\,Z_{TX}}{[\,\alpha\,(Z_L + 2R_{FUSE}) + Z_{TX}\,]\,Z_{GR}}$	$(V_{LA}-V_{LB})_{ac} = \frac{-V_{RX}\,2\,\alpha\,(Z_L + 2R_{FUSE})\,Z_{TX}}{[\,\alpha\,(Z_L + 2R_{FUSE}) + 2Z_{TX}\,]\,Z_{GR}}$
4 Wire Voltage Active Mode $V_{TX} = \frac{[(V_L)_{ac}\,Z_{GR} - \alpha\,(Z_L + 2R_{FUSE})\,V_{RX})]\,Z_{TX}}{[\,\alpha(Z_L + 2R_{FUSE}) + Z_{TX}\,]\,Z_{GR}}$	4 Wire Voltage Active Mode $V_{TX} = \frac{[(V_L)_{ac}\,Z_{GR} - \alpha\,(Z_L + 2R_{FUSE})\,V_{RX}\,]\,Z_{TX}}{[\,\alpha\,(Z_L + 2R_{FUSE}) + 2Z_{TX}\,]\,Z_{GR}}$

Table 1 SL373/SL376 characteristics.

SL373 APPLICATION

This example requires a 2-wire impedance of 600Ω ($Z_L = 600$) and a Receive Gain of 0dB ($Z_L = 600\Omega$) with a loop current of 40 mA (Active). For Standby Mode, the requirement of an Off-Hook threshold at ≈11.0 mA sets a standby loop current of $I_{LIM} \approx 18.75$ mA. The Application Circuit for the SLIC is shown in Fig. 3, and the components Z_{TX}, Z_{GR}, R_{DC} and R_{TH} determine the parameters of the required performance. For this example the resultant component values will be $Z_{TX} = 640k\Omega$, $Z_{GR} = 300k\Omega$, (note 20Ω fuse resistors) $R_{DC} = 2 \times 31.25k\Omega$ and $R_{TH} = 32k\Omega$. The Transmit Gain at $Z_L = 0\Omega$ will then be –0.527dB (×0.941) and the Receive Gain at $Z_L = \infty$ is +6.58dB (×2.14).

The graphs of Figs. 4 to 7 show variation of the SLIC parameters with line resistance. Fig. 4 gives both Active and Standby loop currents as well as indicating the position of the Off-Hook threshold. Note that with the chosen component values, the Saturation Guard becomes active at $R_L \geq 835\Omega$ ($V_{BAT} = -50V$, $R_{FUSE} = 20\Omega$).

Fig. 4 also shows that at line resistance above the Off-Hook threshold, then the Saturation Guard characteristic is true for both Active and Standby Modes. Thus the line resistance at which Off-Hook becomes valid can be obtained from the expression for the Saturation Guard characteristic, in conjunction with that for I_{DET}. We can now determine that:-

$$R_L(\text{off-hook}) = \frac{(|V_{BAT}| - V_{SG})}{I_{DET}} - 2R_{FUSE}$$

$$= 3160\Omega \text{ with } V_{BAT} = -50V \text{ and } R_{FUSE} = 20\Omega.$$

Variation of Transmit Gain with Z_L is shown in Fig. 5 (resistance only). This is evident by setting V_{RX} to zero in the expression for V_{TX} and we obtain:-

$$\frac{V_{TX}}{(V_L)_{ac}} = \frac{Z_{TX}}{\alpha(Z_L + 2R_{FUSE}) + Z_{TX}} = \frac{640}{(680 + Z_L)}$$

in this example. Note that the gain from $(V_{LA}\text{-}V_{LB})_{ac}$ to V_{TX} is constant and is obtained from the expression for V_{TX} at $Z_L = 0\Omega$ and $2R_{FUSE} = 0\Omega$, so that the gain is 0dB.

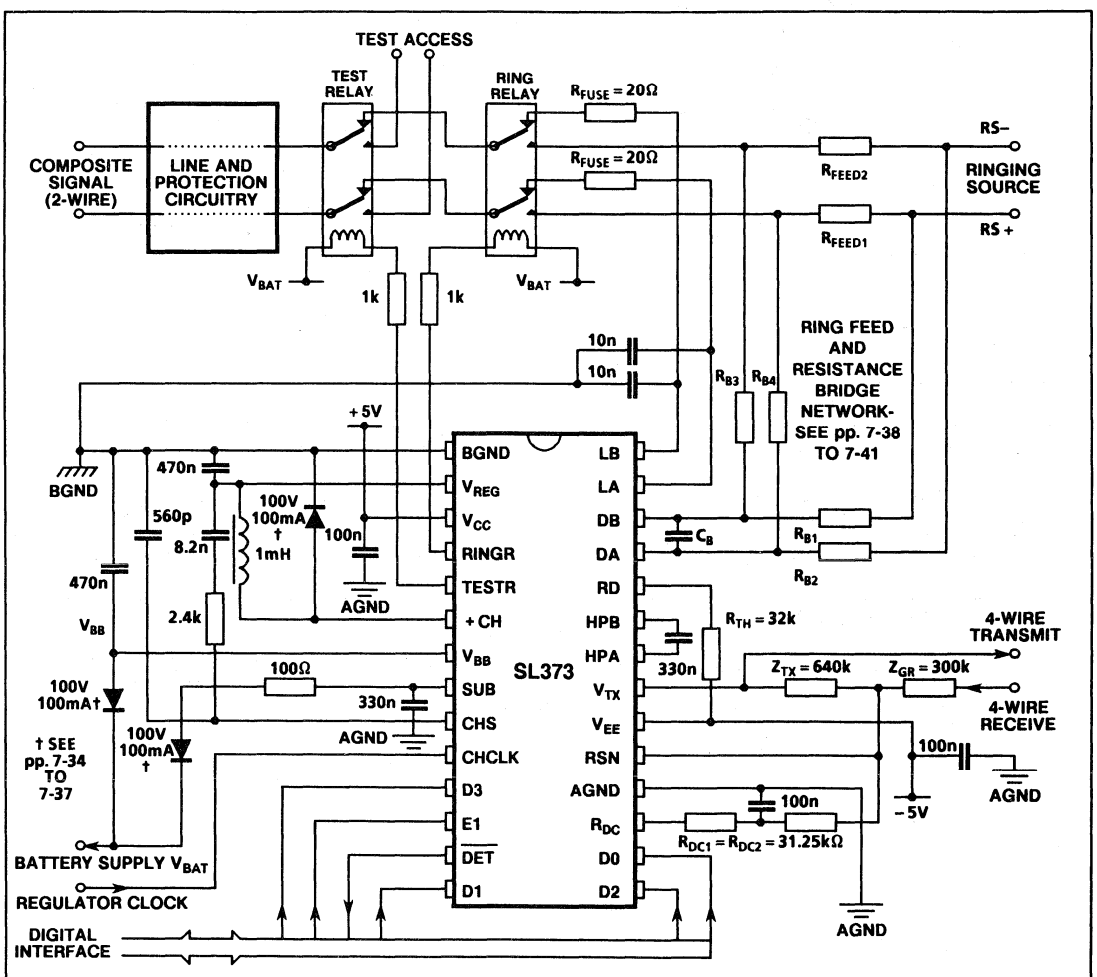


Fig. 3 Basic application circuit SL373 (see also Fig. 38)

In the receive direction, the gain also depends on Z_L in the manner shown in figure 6 (resistive only). This parameter variation can be obtained from the expression for $(V_{LINE})_{ac}$:

$$\frac{(V_{LINE})_{ac}}{V_{RX}} = \frac{-64(Z_L)}{30(Z_L+680)}$$

The Receive Gain will be $-\infty$dB (zero) at $Z_L = 0\Omega$. At $Z_L = \infty\Omega$, the gain goes to 6.58dB (×2.13), whilst at all times the phase of the signal will be inverted.

Finally, the last AC signal to consider is the 4-wire to 4-wire gain. This is obtained from the V_{TX} expression with $(V_L)_{ac}$ set to zero. Fig. 7 shows the relevant variation of gain which follows the expression:

$$\frac{V_{TX}}{V_{RX}} = \frac{-64(Z_L+40)}{30(Z_L+680)}$$

Thus at $Z_L = 0$ the 4w-4w gain is –0.125 (–18.03dB) and at $Z_L = \infty$ it will be 2.13 (6.58dB).

When considering the SLIC Gain settings, note that the Transmit Gain ($(V_{LINE})_{ac}$ to the V_{TX} output) obtained is a consequence of the 2-wire impedance, chosen by setting Z_{TX}. Including fuse resistors increases the value of Z_{TX} by $\alpha 2R_{FUSE}$ at the desired termination impedance (600k + 40k for 600Ω). The Receive Gain is now set by Z_{GR}, from the V_{RX} input to $(V_{LINE})_{ac}$. Since there is attenuation to this point across the fuse resistors, then to set the gain to $(V_{LINE})_{ac}$ the gain to $(V_{LA}–V_{LB})_{ac}$ is increased by a factor of $(Z_L + 2R_{FUSE}) \div Z_L$ to compensate; Z_L the termination impedance. Thus, setting the receive gain to $(V_{LINE})_{ac}$ means that $2R_{FUSE}$ does not affect Z_{GR}, which is scaled with the termination impedance to set the gain accordingly. That is, for this example, Z_{GR} needs to be 300kΩ (600Ω termination, $600 \times 1k \div 300k = 2.0$ for 6dB), and only the attenuation of the line is now considered to determine receive gain to the telephone.

Only the resistive part of the line impedance is considered in Figs. 5, 6 and 7. In practice, the nature of the line is complex and this affects the gain variations with line impedance also. Both Z_{TX} and Z_{GR} will thus need to be made complex also.

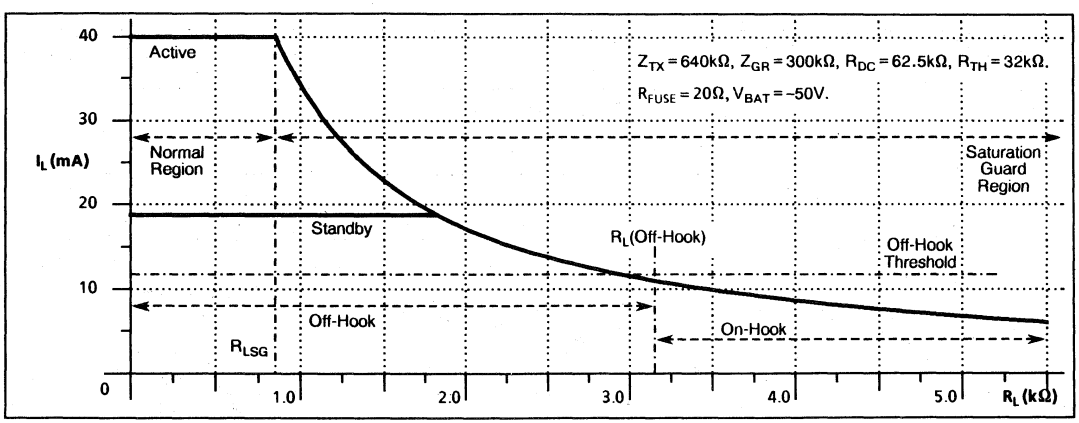


Fig. 4 DC Feed Line current vs R_L, SL373.

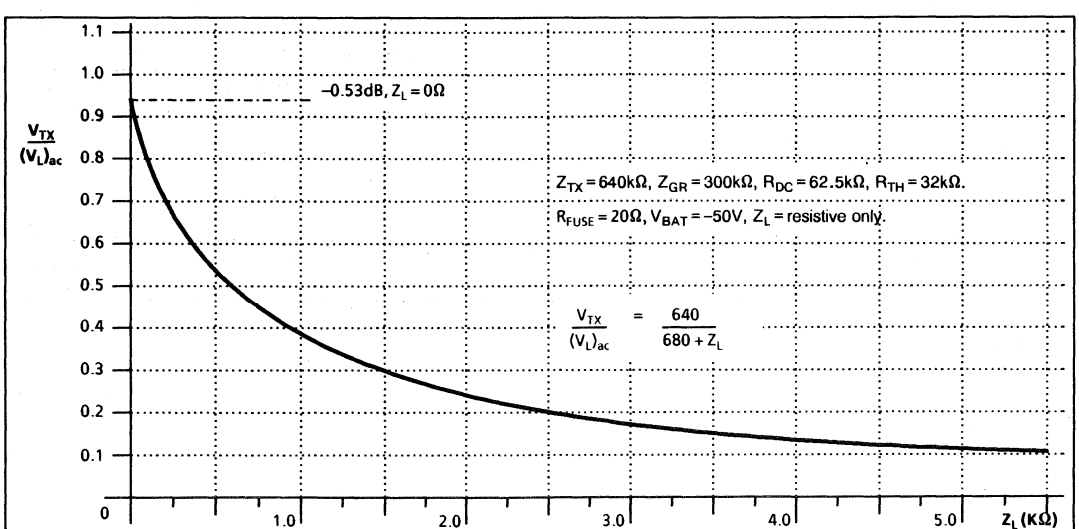


Fig. 5 Transmit Gain vs Z_L, SL373.

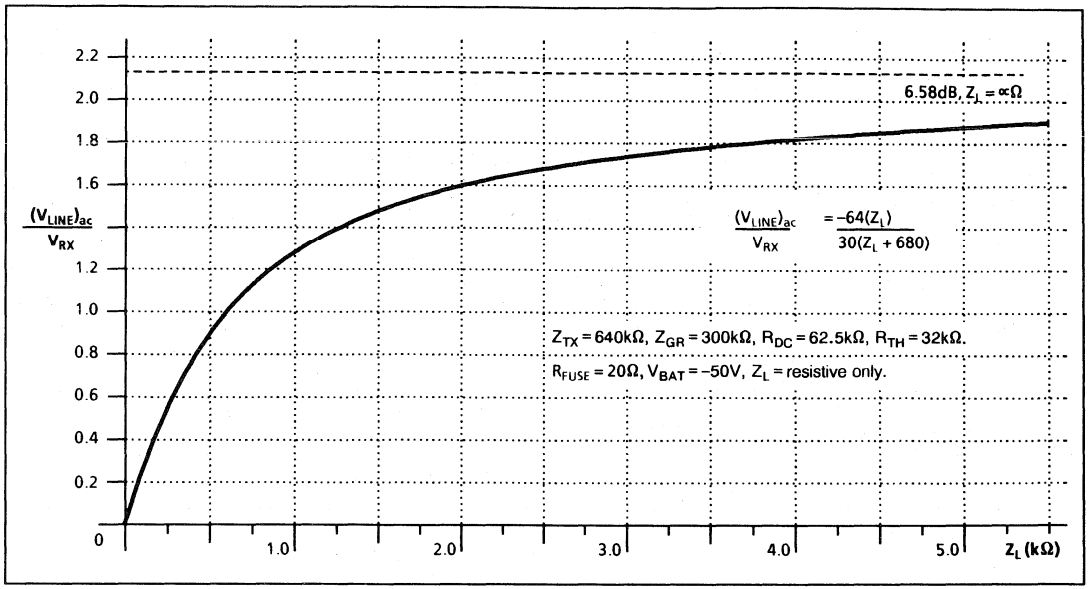


Fig. 6 Receive Gain vs Z_L, SL373.

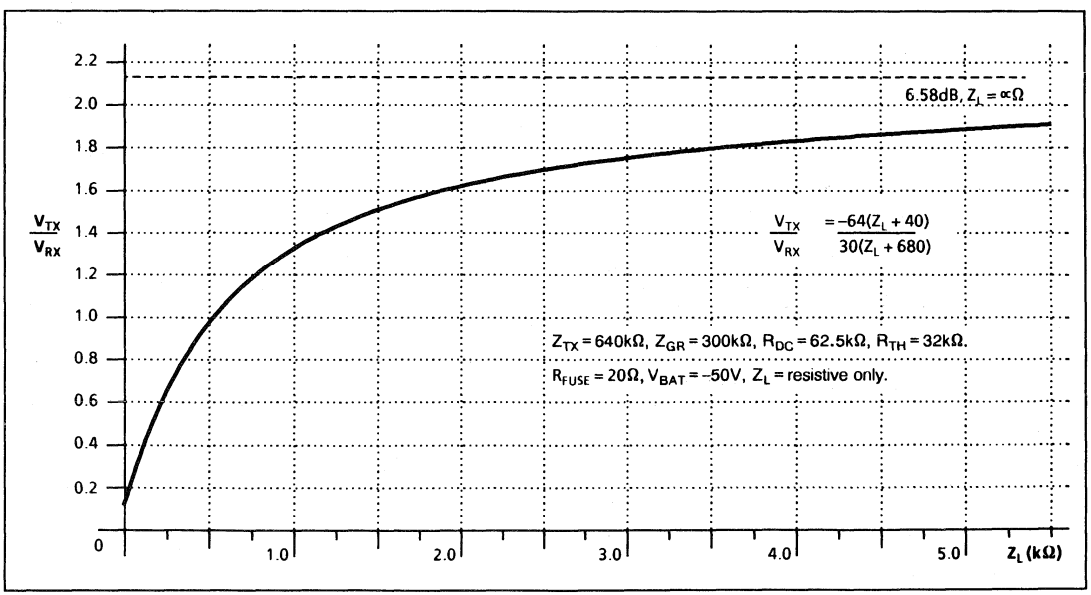


Fig. 7 4W-4W Gain vs Z_L, SL373.

SL376 APPLICATION

For the SL376, the following example is considered. The 2 wire impedance is 600Ω and Receive Gain is 0dB ($Z_L = 600\Omega$) with a total DC feed resistance of 800Ω. For Standby mode, the requirement of an Off-Hook threshold at ≈6.25mA sets a standby loop current of $I_{LIM} \approx 10.7$mA. The Application Circuit, which is similar to that of the SL373, is shown in figure 8 with parameters controlled by Z_{TX}, Z_{GR}, R_{DC} & R_{TH}. To meet the stated requirements, the component values need to be $Z_{TX} = 320k\Omega$, $Z_{GR} = 300k\Omega$, $R_{DC} = 38k\Omega$ ($R_{FUSE} = 20\Omega$) and $R_{TH} = 56k\Omega$. The Transmit Gain at $Z_L = 0\Omega$ will then be –6.55dB (×0.47) and the receive gain at $Z_L = \propto\Omega$ is +6dB with inverse phase.

Figs. 9 to 12 show the variation of the SLIC parameters with line resistance, in the same way as in the SL373 example. Both the Active and Standby currents are given in Fig. 9, together with an indication of the Off-Hook threshold. Note that the Saturation Guard becomes active at $R_{LSG} = 1435.3\Omega$ ($V_{BAT} = -48V$, $R_{FUSE} = 20\Omega$). The line resistance at which Off-Hook becomes valid can again be obtained from the Saturation Guard characteristic, which will be true for both Active and Standby modes as for the SL373. Thus we obtain:-

$$R_L(\text{Off-Hook}) = \frac{(|V_{BAT}| - V_{SG})}{I_{DET}} - 2R_{FUSE}$$

which gives a value of 5000Ω with $V_{BAT} = -48V$ and $R_{FUSE} = 20\Omega$.

Both the Transmit Gain and Receive Gain also vary with Z_L. Figure 10 shows the variation of Transmit Gain (Resistive only) which will follow the expression:-

$$\frac{V_{TX}}{(V_L)_{ac}} = \frac{Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + 2Z_{TX}]} = \frac{320}{Z_L + 680}$$

in this case, obtained from the expression for V_{TX} with $V_{RX} = 0$. It can be seen that the gain from $(V_{LA}\text{-}V_{LB})_{ac}$ to V_{TX} is of course constant, and is obtained from the same expression at $Z_L = 0$, and $R_{FUSE} = 0\Omega$, which gives –6dB exactly.

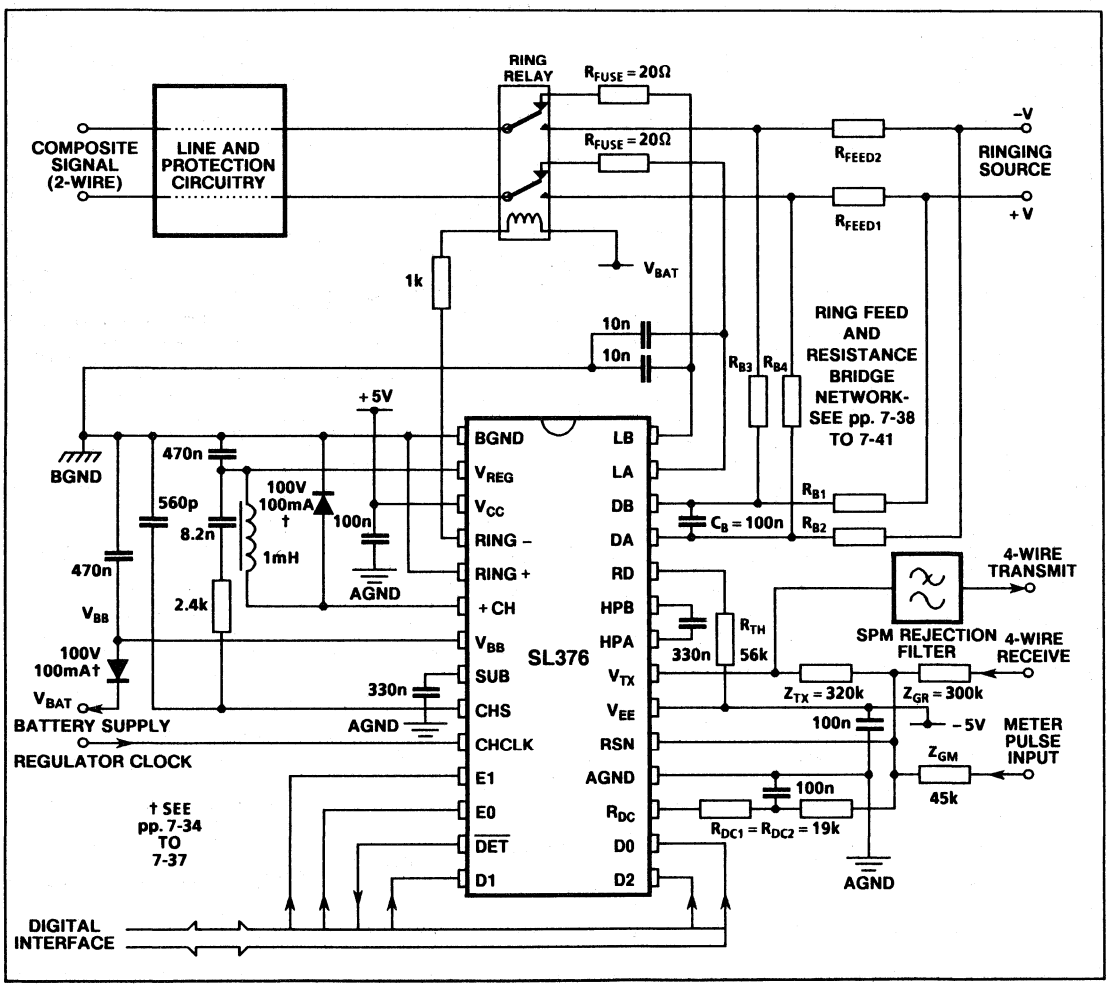


Fig. 8 Basic application circuit, SL376 (see also Fig. 42)

Fig. 11 shows the Receive Gain dependency on Z_L (Resistive only), which is obtained directly from the expression for $(V_{LINE})_{ac}$:-

$$\frac{(V_{LINE})_{ac}}{V_{RX}} = \frac{-64(Z_L)}{30(Z_L+680)}$$

Thus we obtain a value of $-\propto$dB (zero) at $Z_L = 0$ and +6.58dB (×2.13) at $Z_L = \propto\Omega$. The phase of the signal is at all times inverted.

Finally, the 4W-4W Gain also varies with line impedance, and is determined by the relationship for V_{TX} with $(V_L)_{ac} = 0$. In this case it will give an expression of:-

$$\frac{V_{TX}}{V_{RX}} = -\frac{32(Z_L+40)}{30(Z_L+680)}$$

Thus it will vary as in Fig. 12 so that at $Z_L = 0\Omega$ the gain will be –24dB (×0.063) and at $Z_L = \propto\Omega$ it is 0.56dB (×1.067), whilst at all times inverted in phase.

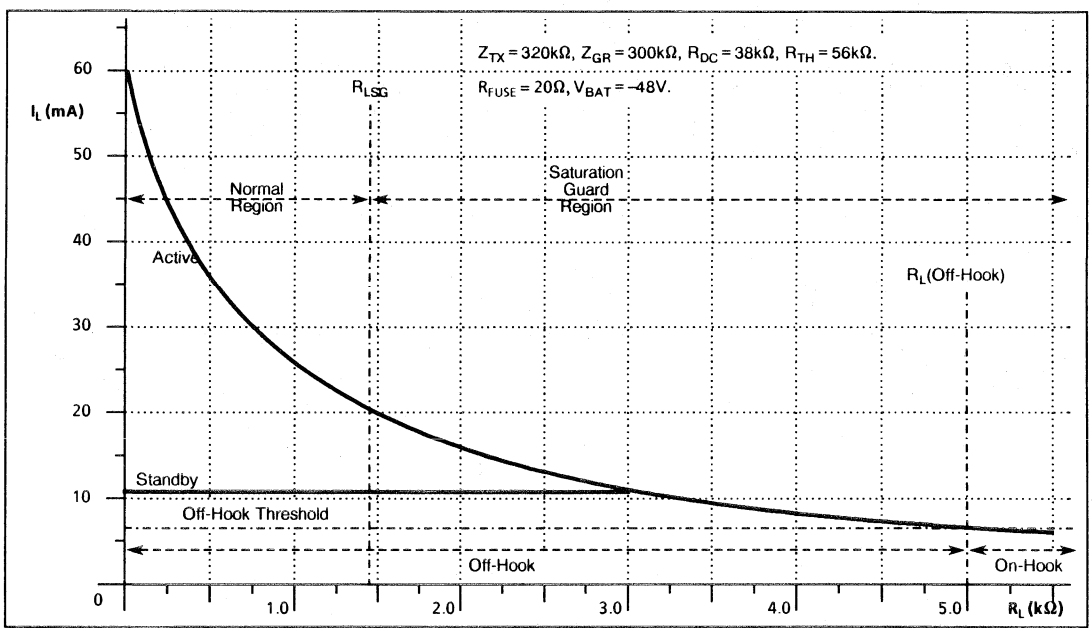


Fig. 9 DC Feed Line current vs R_L, SL376

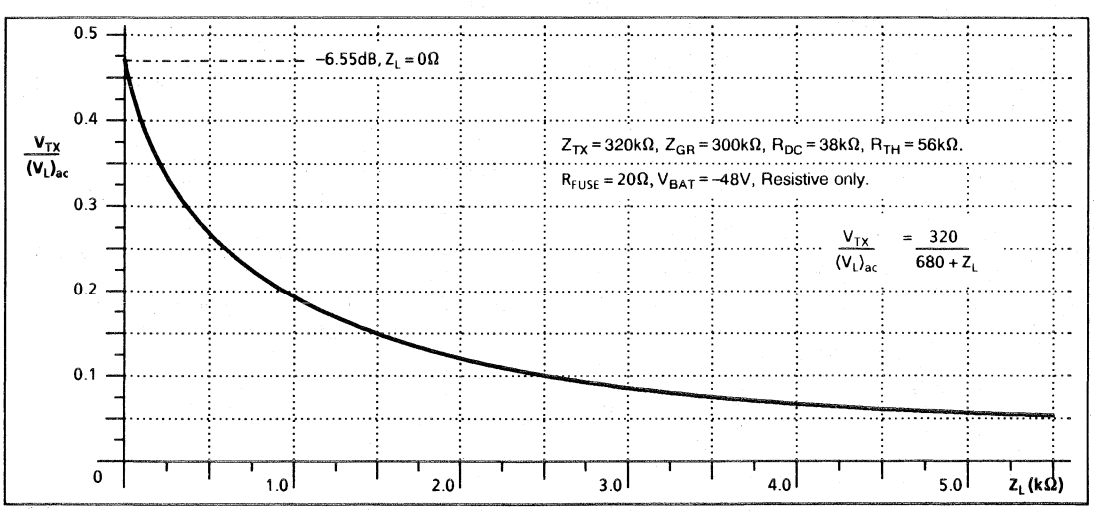


Fig. 10 Transmit Gain vs Z_L, SL376

When considering the SLIC Gain settings, note that the Transmit Gain ($(V_{LINE})_{ac}$ to the V_{TX} output) obtained is a consequence of the 2-wire impedance, chosen by setting Z_{TX}. Including fuse resistors increases the value of Z_{TX} by αR_{FUSE} at the desired termination impedance (300kΩ + 20kΩ for 600Ω). The Receive Gain is now set by Z_{GR}, from the V_{RX} input to $(V_{LINE})_{ac}$. Since there is attenuation to this point across the fuse resistors, then to set the gain to $(V_{LINE})_{ac}$ the gain to $(V_{LA}-V_{LB})_{ac}$ is increased by a factor of $(Z_L + 2R_{FUSE}) + Z_L$ to compensate; Z_L the termination impedance. Thus, setting the receive gain to $(V_{LINE})_{ac}$ means that $2R_{FUSE}$ does not affect Z_{GR}, which is scaled with the termination impedance to set the gain accordingly. That is, for this example, Z_{GR} needs to be 300kΩ (600Ω termination, 600 × 1kΩ ÷ 300kΩ = 2.0 for 6dB), and only the attenuation of the line is now considered to determine receive gain to the telephone.

Only the resistive part of the line impedance is considered in Figs. 10, 11 and 12.. In practice, the nature of the line is complex and this affects the gain variations with line impedance also. Both Z_{TX} and Z_{GR} will thus need to be made complex also.

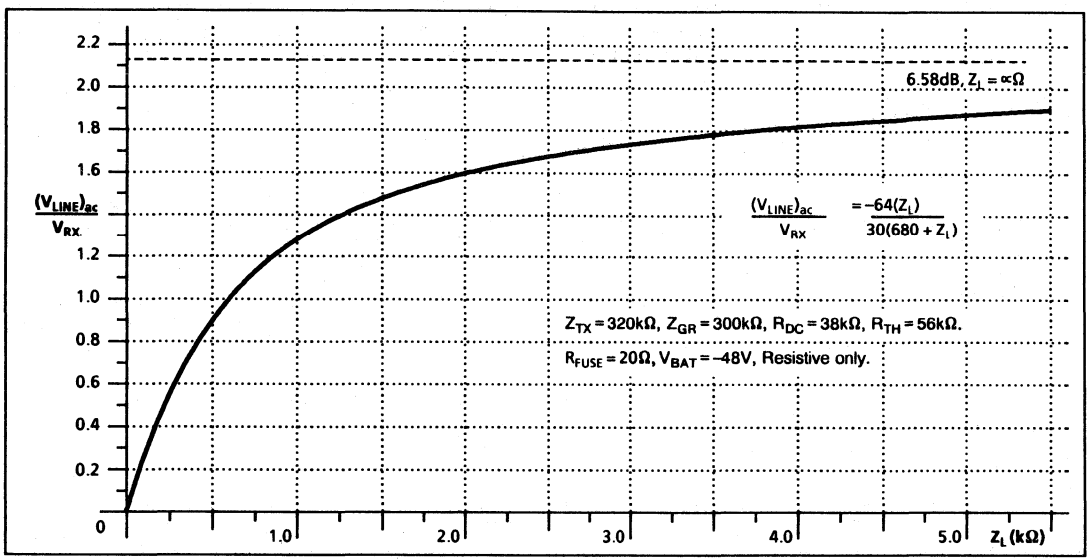


Fig. 11 Receive Gain vs Z_L, SL376

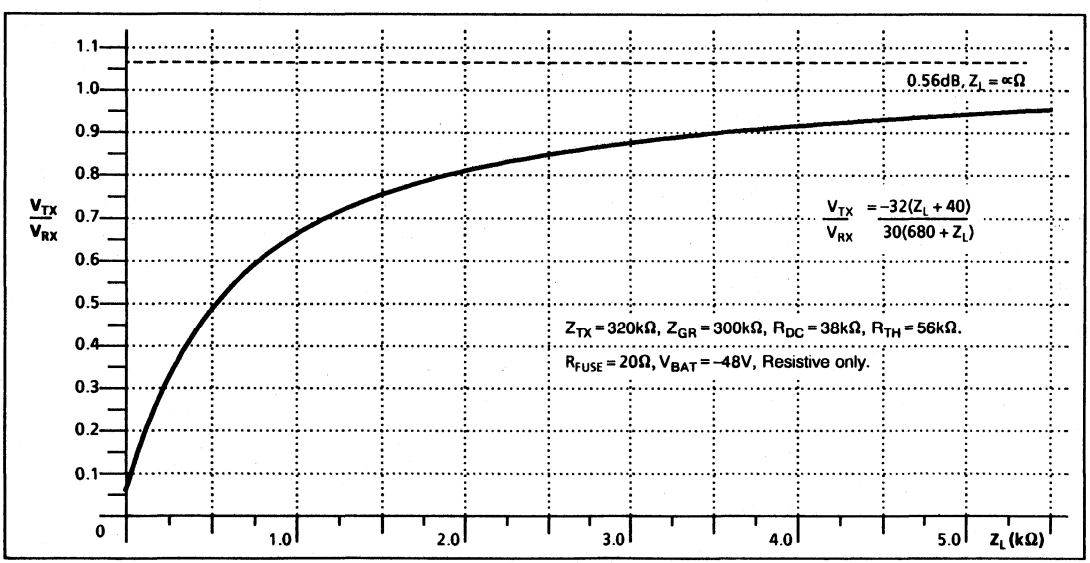


Fig. 12 4W-4W Gain vs Z_L, SL376

SLIC DC FEED CHARACTERISTIC

This section describes how the DC feed characteristic of a SLIC can be drawn very accurately and quickly. The graphs of Figs. 4 and 9 show the feed characteristic of each SLIC, for the examples considered, in I_L vs R_L format. Both graphs can be redrawn as V_L vs I_L, as in Figs. 13 and 14. This demonstrates the linear relationships that exist in each case. Additionally, both graphs show how they can be drawn easily once the component values of R_{DC} and R_{FUSE} are known in conjunction with a given battery voltage. Fig. 13 is for the SL373, whilst Fig. 14 is for the SL376.

For the SL373, the constant current region is set by R_{DC}, which determines the vertical line of the Normal feed region. The slope of the Saturation Guard region is determined partly by the value of the fuse resistors, and descends from the open circuit line voltage, which is nominally ($|V_{BAT}|-V_{SG}$) volts. Both lines meet at a point which is referred to as the Saturation Guard Threshold $|V_{BAT}|-|V_{DCT}| = V_{SG}$ i.e. $V_{LSG}/I_{LSG}/R_{LSG}$. To find where on the graph a given R_L will be, a straight line passing through the origin can be drawn, in addition to the characteristic, with a slope of R_L. Where this line crosses the graph, I_L and V_L will be known.

The SL376 will have a similar characteristic as the SL373 with only the Normal feed region being different. This will be a line of slope $R_{FEEDTOT}$ beginning from a point $50 \div R_{FEEDTOT}$ for $V = 0$, and if extended would intercept the apparent battery voltage i.e. 50V. The Saturation Guard region is drawn as for the SL373 and $V_{LSG}/I_{LSG}/R_{LSG}$ have the same meaning. V_L and I_L for a given R_L can be determined in the same way.

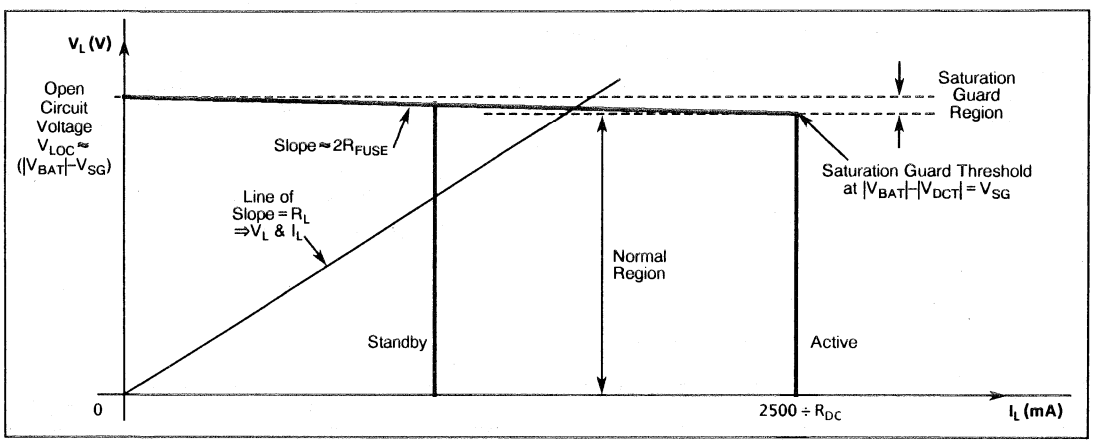


Fig. 13 General DC Feed characteristic V_L vs I_L, SL373

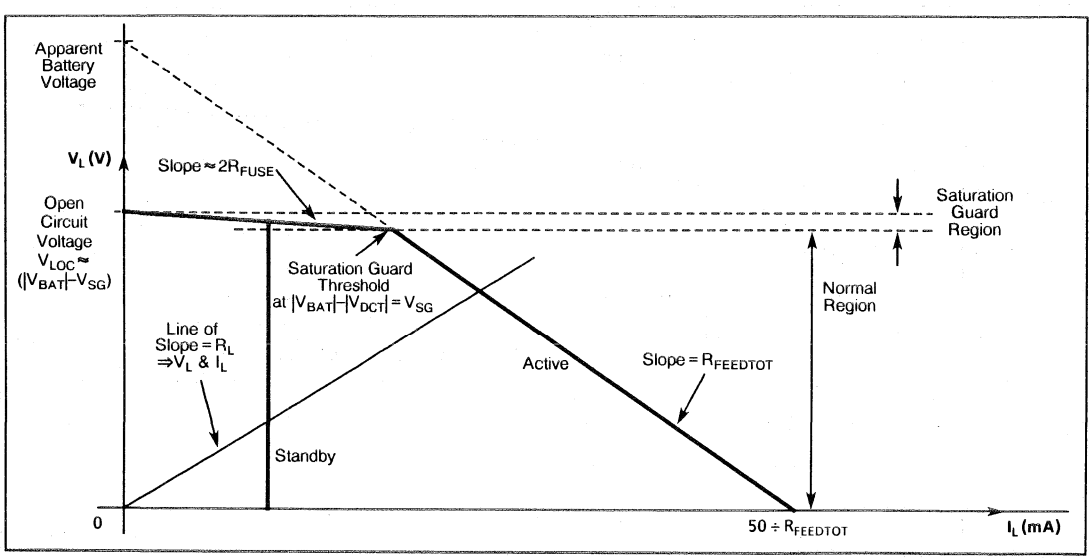


Fig. 14 General DC Feed characteristic V_L vs I_L, SL376

SLIC AC CHARACTERISTICS

In order to determine the AC characteristics of either SLIC, the Application Circuits of Figs. 3 and 8 can be redrawn as the simplified models of Figs. 15 to 18.

The SL373 Transmit direction is modelled as in Fig. 15. This shows a voltage, V_{TEL}, generated at the telephone with Z_{TEL} source impedance, and a resultant voltage of V_{TX} equivalent to the SLIC VTX pin output. In the Receive direction, the model is redrawn as that of Fig. 16. The input this time is a current generator of $(\alpha V_{RX}) \div (Z_{GR})$ with a resultant output of V_{TEL} at the telephone end.

The equivalent models for the SL376 are shown in Figs. 17 and 18, differing only in parameter values. Note that V_{TEL} represents either the input voltage at the telephone (receive direction) or the output voltage generated at the telephone (transmit direction), and that in this case Z_L represents the effect of the transmission line and telephone source impedance.

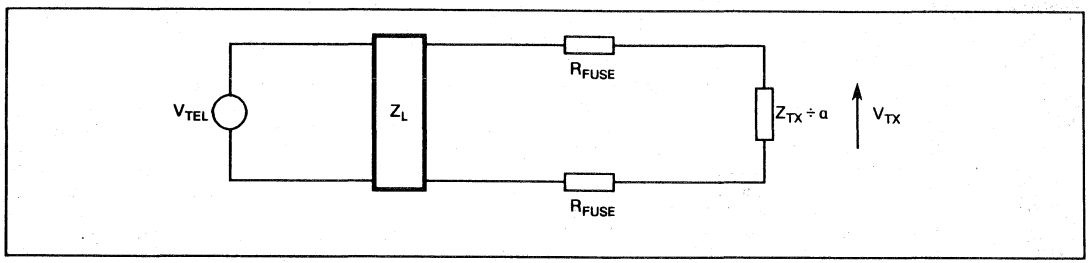


Fig. 15 Transmit circuit model, SL373.

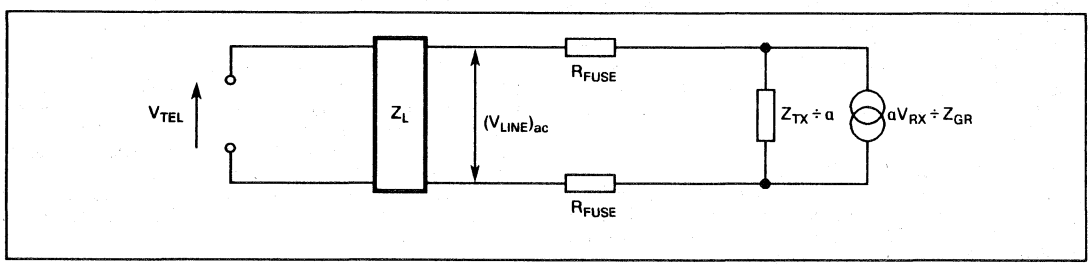


Fig. 16 Receive circuit model, SL373.

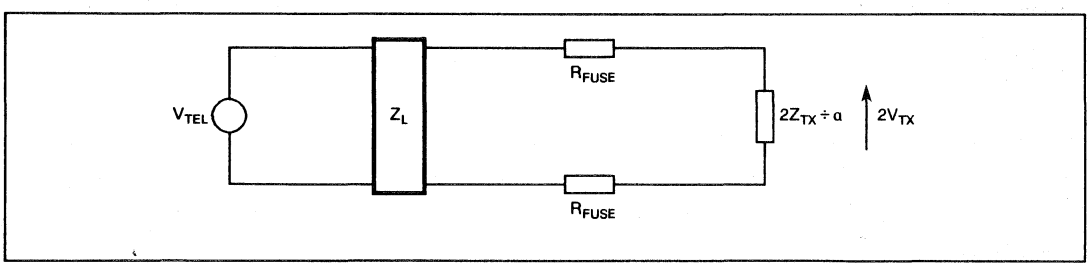


Fig. 17 Transmit circuit model, SL376.

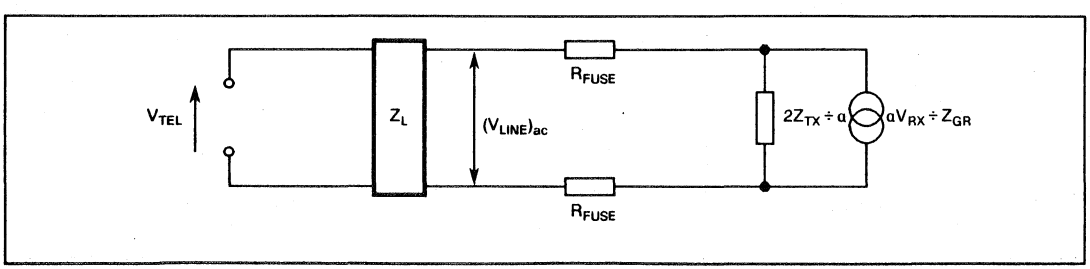


Fig. 18 Receive circuit model, SL376.

LINE CARD CONSIDERATIONS

GENERAL

Because the output voltage of the SLIC at the V_{TX} pin is a superposition of the voltage on the line (AC) and the receive input signal, the SLIC does not separate the directions of transmission. Several circuit possibilities to achieve this function external to the SLIC can be used, depending in the final Line Card solution required.

The most complete and versatile solution is to use the MV3010 Plessey Subscriber Line Audio Circuit (PSLAC). This is a DSP device including high quality D-A and A-D interfaces with a choice of PCM interface signal format (data rate, A-Law/μ-Law/Linear companding) for connection to the system backplane. Central to the features of the MV3010 is an automatically adaptive Cancellation Filter (9 tap FIR + 1 tap IIR) which is capable of adapting to changing line conditions of the Subscriber Interface to maintain high Trans-Hybrid Balance (and thus transmission signals separation). In addition, further digital filters on this device allow modification of both Transmit/Receive Gains and Frequency Response. All of the MV3010 functions are dynamically programmable via the device Digital Interface which can be connected to a microprocessor. Further details on both the MV3010 and microprocessor interface can be obtained by reference to the MV3010 Data Sheet and Application Notes AN42, AN84, AN102, AN103, AN104 and AN111. Some simple SLIC/PSLAC interfaces are discussed below.

In certain circumstances where the superior performance of the MV3010 is not required, the choice may be to use a standard COMBO or other discrete circuitry in conjunction with the SLIC. This circuitry must of course be capable of providing the necessary Trans-Hybrid Balance and A-D/D-A performance. Suggestions as to how this might be achieved are outlined later in this section.

SLIC/PSLAC INTERFACE - SL373

Both the analog (AC) and digital side of the SLIC/PSLAC interface need to be considered separately. Fig. 19 shows how the SL373 SLIC can be connected to the MV3010 SLAC to cater for AC signals. Note that the critical area of this interface is the voltage at the V_{IN} pin. If the DC offset level is too high this prevents adaption of the MV3010 C Filter in addition to reducing the dynamic range of the AC signal. The DC offset of the 4-wire transmit output of the SL376/SL373 is specified to be fully compatible with the MV3010. If a different circuit to that of the SLIC is used, then the driving source must present a low output impedance and DC offset compatible with the MV3010 input requirements (see MV3010 data Sheet, page 3-135).

When considering Meter Pulse Signalling, the injection of high frequency pulses at the 4-wire input to the SLIC, will also give rise to a signal at the 4-wire output. This additional signal to that in the voice band is capable of overloading the SL373 dynamic range. For this reason, the specifically designed SL376 Metering SLIC (MSLIC) should be used instead.

SLIC/PSLAC & METERING INTERFACE - SL376

Fig. 20 shows how the SLIC/PSLAC interface is reconfigured for use with the SL376. Note that the dynamic range at the 2-wire port of the SL376 is twice that of the SL373, but that the 4-wire output dynamic range is the same. Now, since the output impedance and offset voltage of the SL376 are also sufficiently low, then the direct SLIC/PSLAC connection can be maintained (the MV3010 has a low pass filter at the analog input, which excludes frequencies above ~4KHz). The additional network Z_{GM} (determines Metering gain) is thus the only change to the interface (this is discussed further later in this section).

Normally, Z_{TX} is chosen to set the termination impedance of the line, and the ratio of Z_{GR}/Z_{TX} sets the Receive Gain within the voice band. To determine Receive Gain at metering frequencies for the metering input, this is done in the same way as for Z_{GR}. However, the nominal Receive Gain of the SL376 ($Z_L = \alpha$) is ≈ -3.6dB at metering frequencies (this is very dependent on board layout near RSN, and on 2-Wire line decoupling) and must be taken into account when choosing Z_{GM}. Thus we derive the following:

$$\frac{(V_{LINE})_{ac}}{V_{RM}} = G_M = -\frac{2\alpha(Z_L)Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + 2Z_{TX}]Z_{GM}} \times 0.66$$

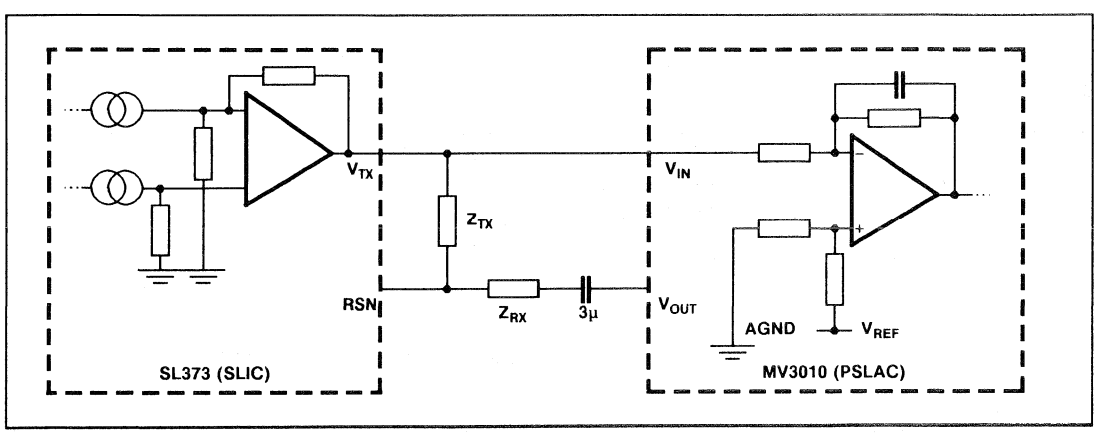


Fig. 19 Simple SLIC/PSLAC interface, SL373.

For the application example considered in the Hardware Programming section, we have $Z_{TX} = 320k\Omega$ $Z_{GR} = 300k\Omega$, $R_{FUSE} = 20\Omega$ and $\alpha = 1000$. Thus for a 1V RMS Meter Pulse Source, then for 2.2V RMS on the line at $Z_L = 200\Omega$, $G_M = \times 2.2$ and $Z_{GM} = 43.64k\Omega$. Fig. 21 shows the variation of Meter Pulse Gain with Z_L (Resistive only). This gives $G_M = 0$ at $Z_L = 0$ and $G_M = 9.68$ at $Z_L = \propto \Omega$.

As mentioned earlier, the dynamic range of the SL376 output matches that of the MV3010 input, such that direct connection is possible. Thus, since the SL376 interface circuitry is designed to prevent overload of the 2-wire port (V_{LA}–$V_{LB} \leq 6Vp\text{-}p$), the MV3010 input will not suffer overload conditions. The internal filtering of the MV3010 is capable of removing the high frequency meter pulses which fall outside of the psophometric weighting of the filters. However some degradation of transmission performance

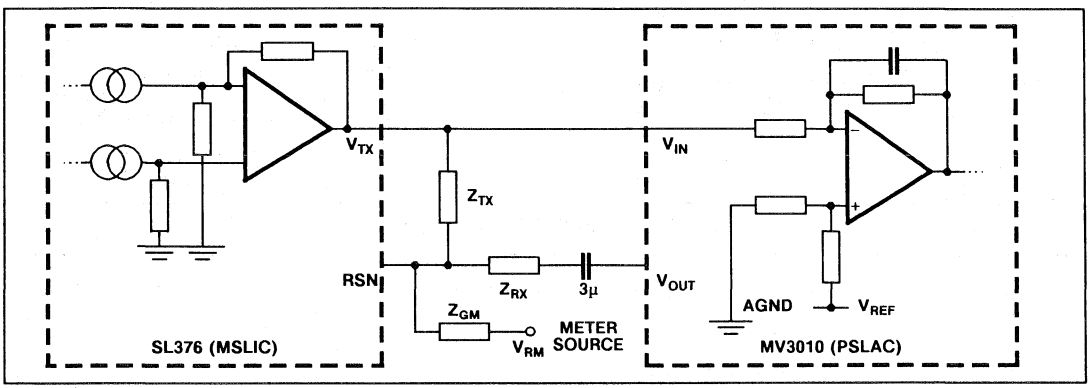


Fig. 20 Simple SLIC/PSLAC interface, SL376

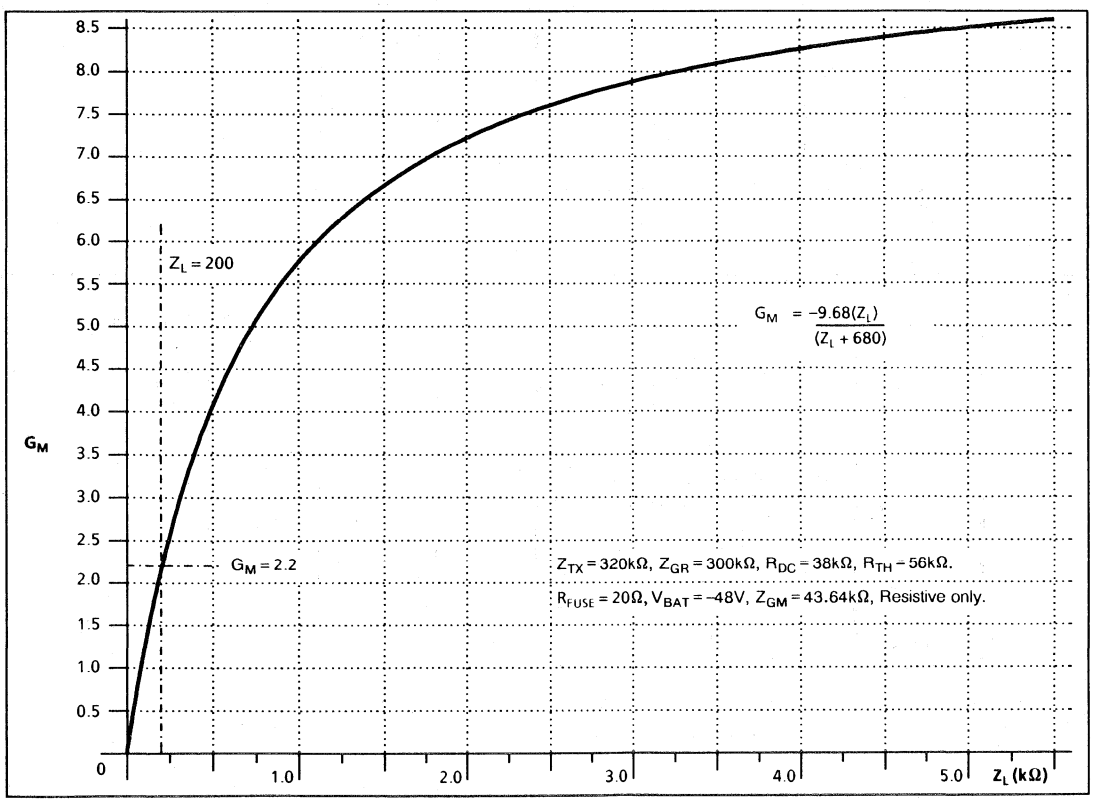


Fig. 21 Metering gain, G_M vs Z_L, SL376

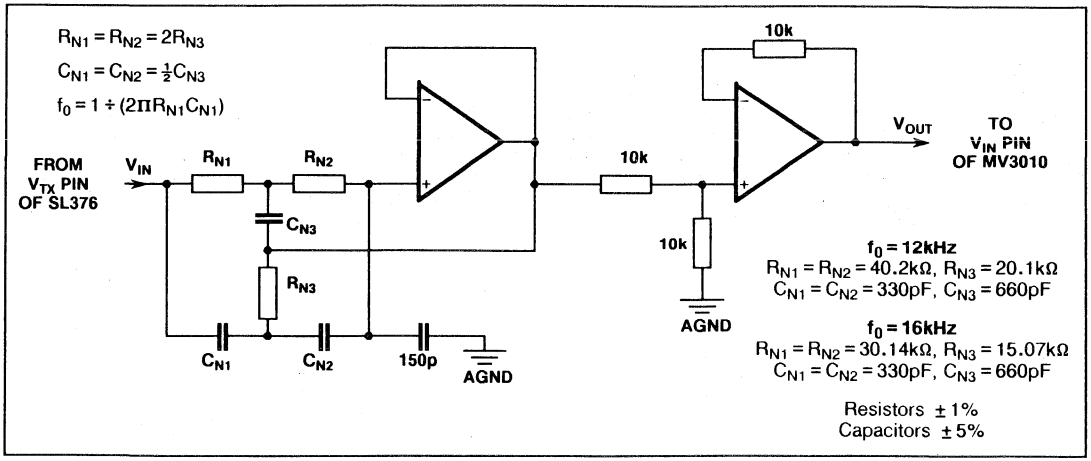


Fig. 22 Alternative SL376/PSLAC analog interface

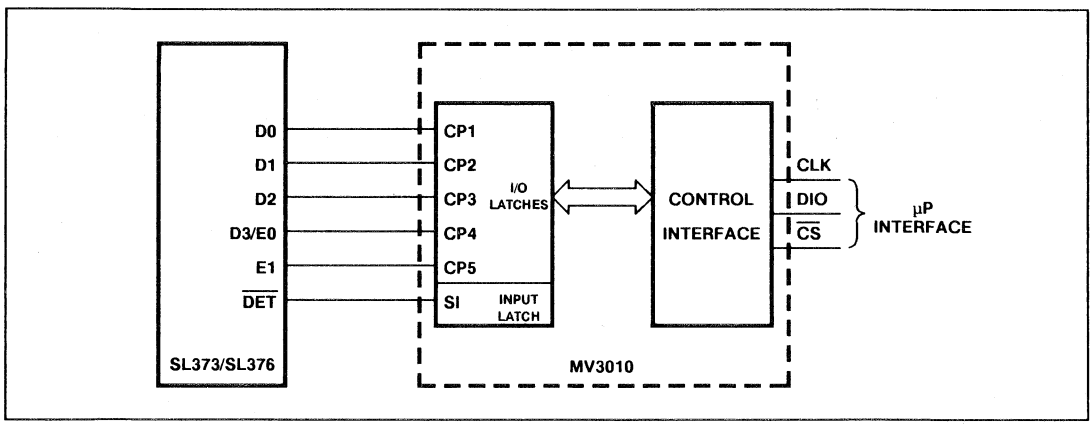


Fig. 23 Simple SLIC/PSLAC digital interface, SL373/SL376

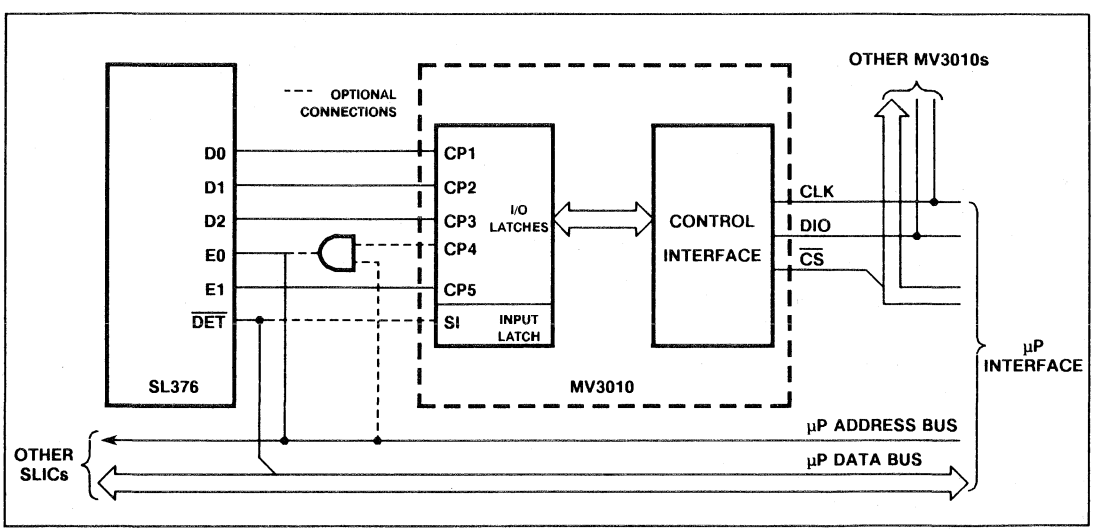


Fig. 24 Alternative SLIC/PSLAC digital interface, SL376

may occur, especially if the meter frequency coincides with a peak in the skirt of the MV3010 filters. This may typically add an in-band alias of no more than ~20-30mV equivalent at the MV3010 digital output, depending on the gain settings involved. The 6dB loss in voice frequencies intrinsic to the SL376 can be recovered by use of the MV3010 digital gain stage, which may be up to +13dB whilst maintaining CCITT G.714 requirements, or up to +18dB with some degradation of performance.

If more gain is required between SL376 and MV3010, then some form of meter pulse filtering will be required. Fig. 22 shows one possible technique for a simple filter/gain stage. This circuit consists of a notch filter capable of at least 20dB rejection, and may be greater depending on component matching. The following stage can be used to add gain at voice frequencies, and the whole circuit can be used if interfacing to other types of COMBO device is required.

SL373/SL376 DIGITAL INTERFACE

The SL373 and SL376 digital inputs are non-latched TTL-compatible, and control the SLIC functions as described in the related Data Sheets. When interfacing these inputs to the MV3010, this device has latched outputs such that direct connection to the MV3010 can be used. Since the MV3010 does not have dedicated I/O pins, these may be connected in any order.

In addition, the $\overline{DET}$ output of the SLIC can be connected to the MV3010. The SLIC operating modes can then be controlled via the MV3010 I/O pins and the line status read via the SI (Status Input) pin. This gives the digital interface as shown in Fig. 23, with CP1, CP2, CP3 controlling SLIC modes, CP4 the Test Relay (SL373) or $\overline{DET}$ enable E0 (SL376), CP5 the SLIC detector setup and SI reads the line status. The Line Card is now fully controlled via the MV3010, with microprocessor/controller interface options to the MV3010 as described in Application Note AN42.

The circuit of Fig. 23 is suitable for both the SL373 and SL376. However, since the SL376 has a different digital input coding to that of the SL373, then an alternative SLIC/PSLAC interface can be used, as shown in Fig. 24. This allows the status of a number of subscribers on a line card to be determined simultaneously. Higher level processing of the system can then service any line as necessary, via the microprocessor/controller associated with that MV3010. In addition, if the E0/E1 pins are still connected to the MV3010 as before, then an individual SLIC can be controlled via the MV3010.

SLIC/COMBO OPTIONS

If conditions of the line are sufficiently well known and/or performance of the final line card solution not so determinate, then an alternative application circuit may be used. Fig. 25 shows how a standard COMBO device might be used in association with the SLIC.

The most important difference from the MV3010 application, is that the COMBO has no balance filter such that trans-hybrid balance must be achieved separately. The suggestion here is to use an Op Amp between SLIC and COMBO which can set transmit gain (via Z_{X2}/Z_{X1}), with an added balance network Z_{BR}. Z_{BR} is chosen to closely match the echo return of the SLIC such that the summation of V_{RX} and the return at V_{TX} attenuates V_{RX} at the Op Amp output. When using the SL376, the network Z_{BM} is further added to attenuate meter signalling at the COMBO V_{IN} in the same way.

To complete the solution, additional logic will be needed to control PCM timing of the COMBO and interface the circuit to the PCM Backplane. This logic will also need to provide a microprocessor/controller interface (or other digital control interface) to match the SLIC digital inputs/output to the system hardware. The precise nature of the logic will of course depend on the COMBO used and the final application solution required.

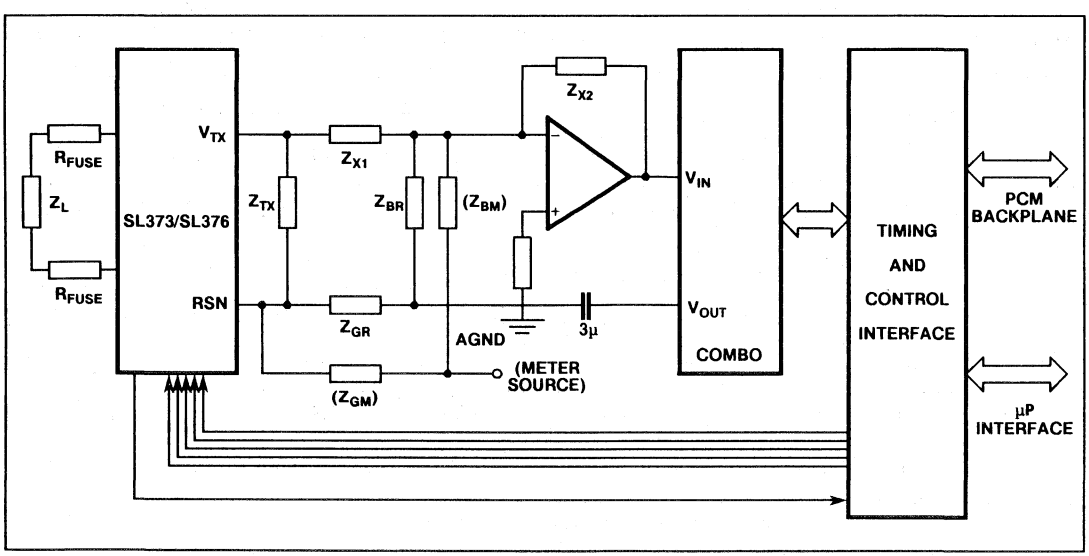


Fig. 25 SLIC/COMBO line card outline (SL376 options are shown in brackets)

THE SWITCHING REGULATOR

GENERAL

The SL373 (page 3-3) and SL376 (page 3-52) data sheets describe the operation of the Switching Regulator, which is nominally the same circuitry for both devices. This section describes the characteristics of the operation in more detail. One important point to note is that the Regulator is powered down in Standby mode in the case of the SL376, the consequences of which are discussed on page 7-42. The SL373 leaves the Regulator operational in Standby mode.

As stated in the SLIC data sheets, V_{REG} follows a voltage V_{REF} such that:-

$$V_{REF} = -(|V_{DCT}| + BIAS) \quad ...(1)$$

where $|V_{DCT}| = |V_{LA} - V_{LB}|$. V_{DCT} can be determined from the equations quoted in Table 1 (page 7-21). V_{DCT} depends on I_L and the total resistance from LA to LB. Thus for the DC feed modes of the SLIC, we can write approximate relationships for V_{REG} vs R_L as in Table 2 (obtained using equation 1). Precise values for V_{REG} are given in the Electrical Characteristics section of each device data sheet, for defined line impedance.

Fig. 26 indicates what the graph of V_{REG} vs R_L looks like with $R_{DC} = 62.5k\Omega$ and $R_{TH} = 32k\Omega$ whilst Fig. 27 is for the SL376 with $R_{DC} = 38k\Omega$ and $R_{TH} = 56k\Omega$.

REGULATOR COMPONENTS

The function of the components of the Regulator circuit are discussed in the SLIC Data Sheets. These components should be chosen carefully to meet a number of circuit criteria. Guidance on how to do this is given below, with reference to Figs. 28 and 29 showing the Regulator circuit of the SL373 and SL376 respectively.

Firstly, the 1mH inductor (L_1) should be capable of taking at least twice the line current without saturating (most probably iron core) and have a series resistance below 20Ω. If the inductor saturates, this could cause excessive current switching which may damage the SLIC. The low resistance reduces stored energy dissipation and hence regulator noise pickup. In addition, the self resonant frequency of the inductor should be sufficiently high ($\sim 10 \times f_{CHCLK}$) to suppress high frequency harmonics of the CHCLK frequency.

Both C_2 and D_1 should be low lead inductance components and all connections to V_{BB} and +CH should be as short as possible. C_1 must be of a material, e.g. polyester, that will not cause oscillation of the stabilisation network R_1/C_3 (thus avoiding subharmonics of CHCLK) and have a working voltage >70V with short leads to ensure CHCLK harmonics are correctly filtered.

All of D_1-D_3 should have a recovery time <10ns (preventing large transient currents when the switch closes) and rated >70V reverse voltage with $>2 \times I_L$ forward current. Note that R_2 for the SL376 is inside the device such that R_2 and D_3 are unnecessary.

When designing the PCB layout, note that very large voltage changes occur at +CH. Since this is a high impedance connection to the inductor, this component

SL373 - DC	SL376 - DC
$V_{LINE} = (V_{LA} - V_{LB}) = V_{DCT}$ $V_{REF} = -(\|V_{DCT}\| + BIAS)$ where $\|V_{DCT}\| = \|I_L(R_L + 2R_{FUSE})\|$	$V_{LINE} = (V_{LA} - V_{LB}) = V_{DCT}$ $V_{REF} = -(\|V_{DCT}\| + BIAS)$ where $\|V_{DCT}\| = \|I_L(R_L + 2R_{FUSE})\|$
ACTIVE MODE : Normal Region $V_{REG} \approx (0.9)(V_{LINE}) + 12.8$	ACTIVE MODE : Normal Region $V_{REG} \approx (0.9)(V_{LINE}) + 16.0$
ACTIVE MODE : Saturation Guard Region $V_{REG} \approx (0.9)(V_{LINE}) + 12.8$	ACTIVE MODE : Saturation Guard Region $V_{REG} \approx (0.9)(V_{LINE}) + 16.0$
STANDBY MODE : Until Saturation Guard Region $V_{REG} \approx (0.9)(V_{LINE}) + 12.8$	STANDBY MODE : Until Saturation Guard Region Regulator is powered down, $V_{REG} \approx V_{BB}$
STANDBY MODE : Saturation Guard Region $V_{REG} \approx (0.9)(V_{LINE}) + 12.8$	STANDBY MODE : Saturation Guard Region Regulator is powered down, $V_{REG} \approx V_{BB}$

Table 2 SL373/SL376 regulator characteristics (approximate)

must be close to the device. All sensitive circuit nodes (AGND/RSN), should be protected against pick up from this connection by a guard ring or ground plane of BGND surrounding these pins (separate from any AGND plane).

If there is more than one SLIC in the system, then the Switching Regulators can be synchronised to the same 256kHz clock to reduce voice band interference from intermodulation products and to synchronise the single frequency noise to the existing system clock frequency. Alternatively, the regulator of both the SL373 and SL376 will free-run in the absence of a clock signal.

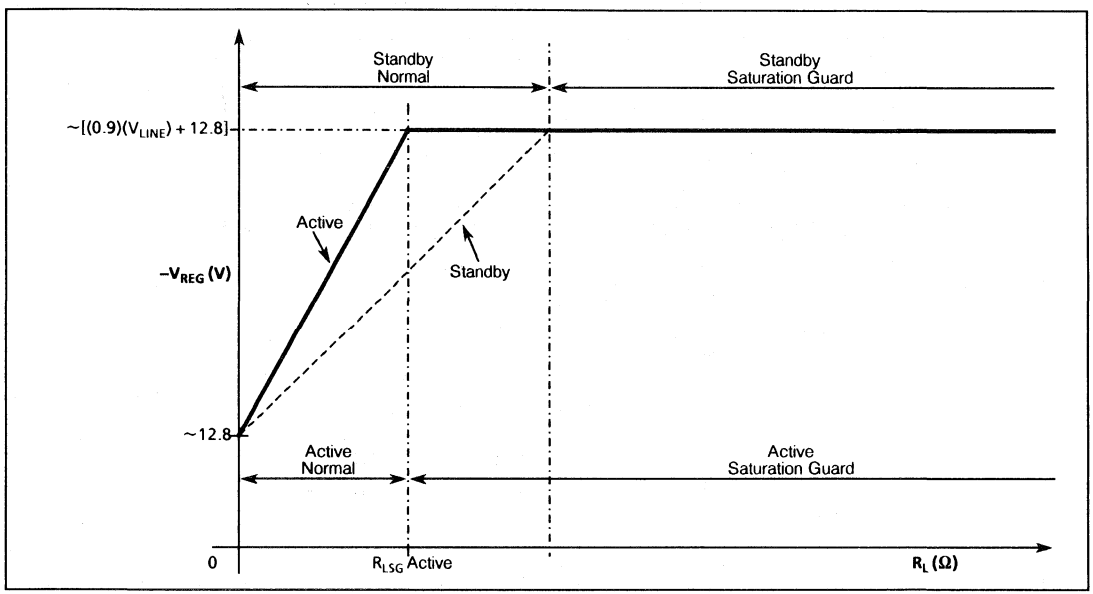


Fig. 26 V_{REG} vs R_L, SL373.

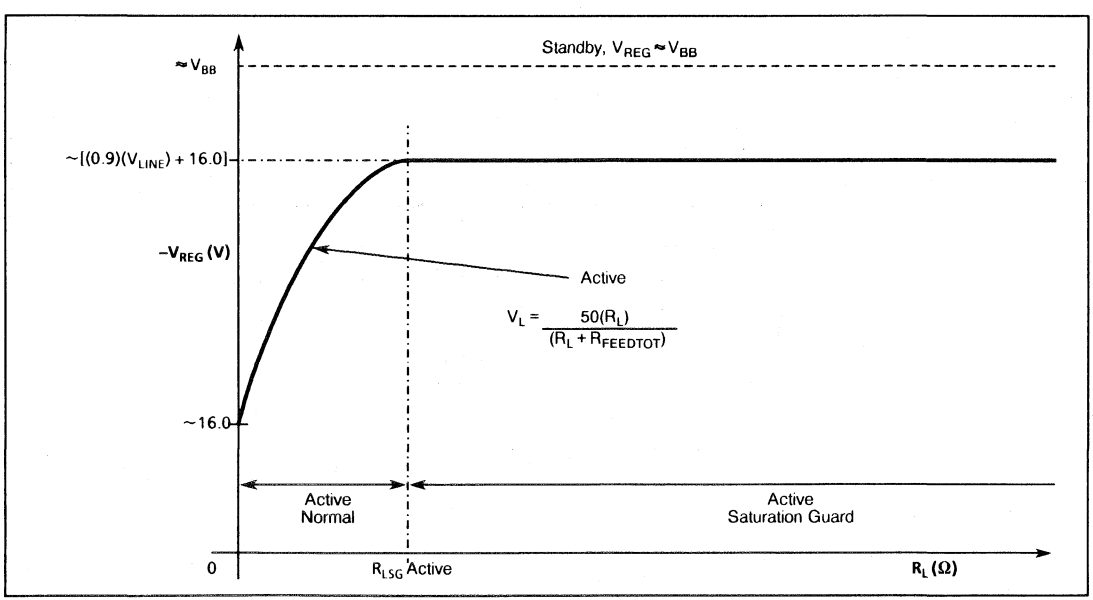


Fig. 27 V_{REG} vs R_L, SL376.

POWER DISSIPATION

Since the voltage V_{REG} is used to power the line amplifiers, then it can be seen from Figs. 26 and 27 how power savings result (on short lines) by inclusion of the voltage regulator circuit. The DC voltages associated with the SLIC are shown in Fig. 30 which shows how the regulator acts in practice.

We can get an illustration of the typical power savings that result by comparing the general case of Fig. 30 to that of the 'ideal' shown in Fig. 31.

Thus we consider the SL376 set for 48V battery and 800Ω feed and measure the current I_{BAT} as a function of line resistance (total LA pin - LB pin resistance). The resultant total power consumption is then shown by curve **B** of Fig. 32. This can be compared to the consumption for the circuit of Fig. 31 shown by curve **A**.

Lastly curve **C** of Fig. 32 shows estimated power dissipation within the SLIC. The difference between curves **B** and **C** of Fig. 32 then represents the external power dissipation, Fig. 30.

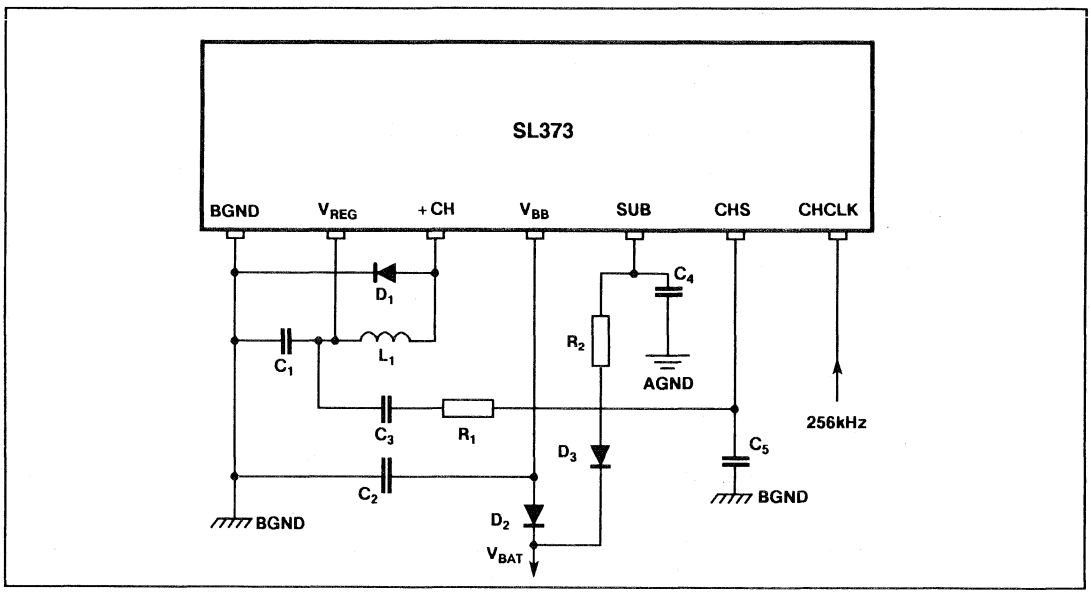


Fig.28 Voltage regulator circuit, SL373

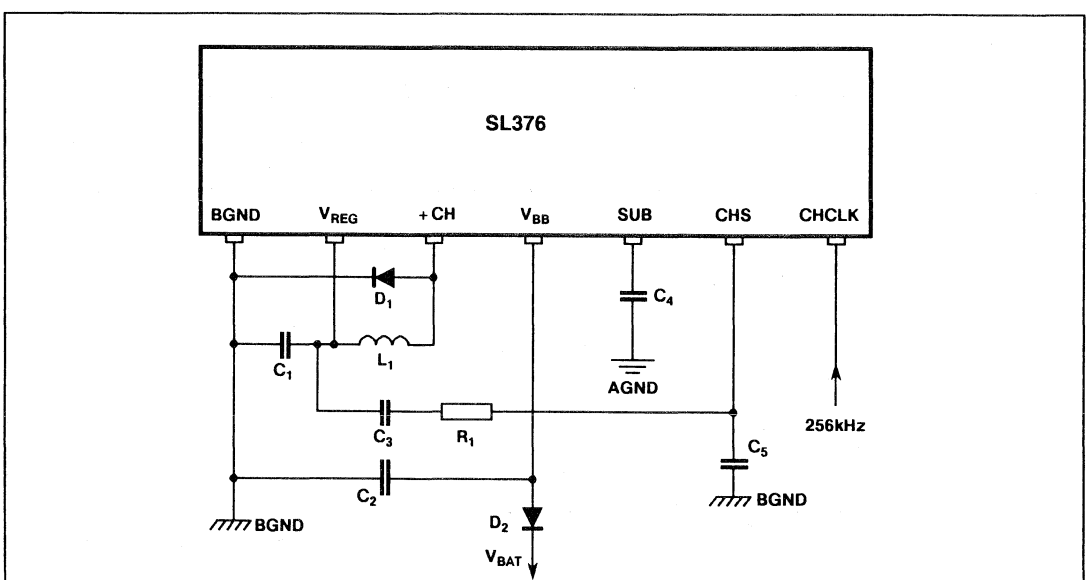


Fig.29 Voltage regulator circuit, SL376

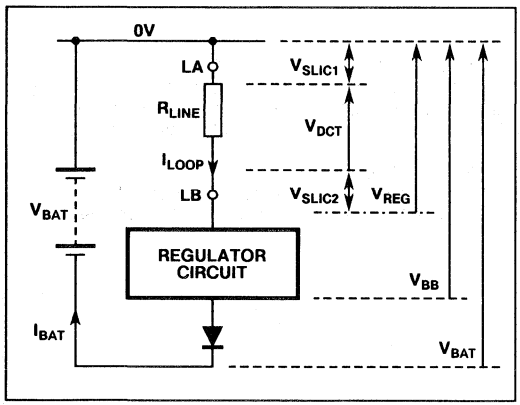


Fig. 30 DC feed voltages, general case

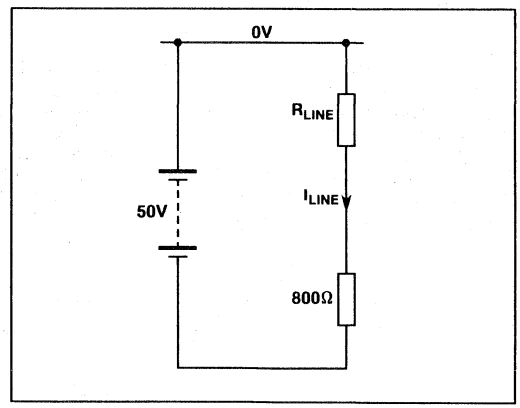


Fig. 31 'Ideal' resistive feed case

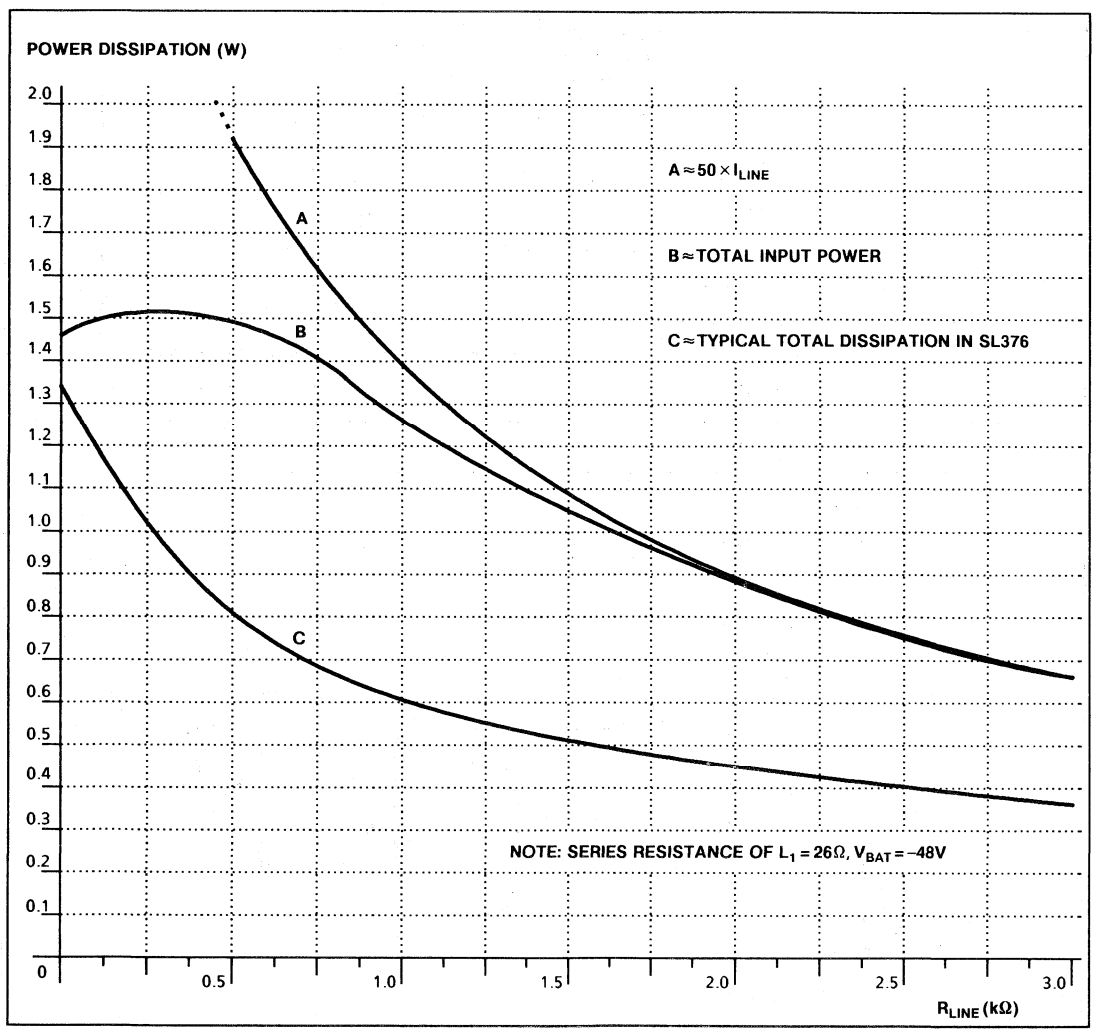


Fig. 32 Typical power dissipation (for SL376, 50V Batery, 800Ω feed)

RING TRIP CIRCUITS

GENERAL

Both SLICs can be used in Ringing Mode with the addition of an external relay which is energised by the on-chip Ring Relay Driver. This mode of operation is selected via the Digital Interface as described in the SLIC Data Sheets. When Ringing Mode is selected, the Ring Relay Driver is activated and the Ring Trip Comparator is selected for an output on $\overline{DET}$. Note that AC Ringing and DC Feed voltages are supplied separately via the Ring Relay to the line, connected as indicated in Fig. 33.

The SLIC ringing circuit can either be Balanced or Unbalanced in format. Connections of the feed and bridge resistors for each case are given in the following pages.

BALANCED RINGING - DC

In this case, the connections for Balanced Ringing are shown in Fig. 34. The feed resistors R_{FEED1} and R_{FEED2} are

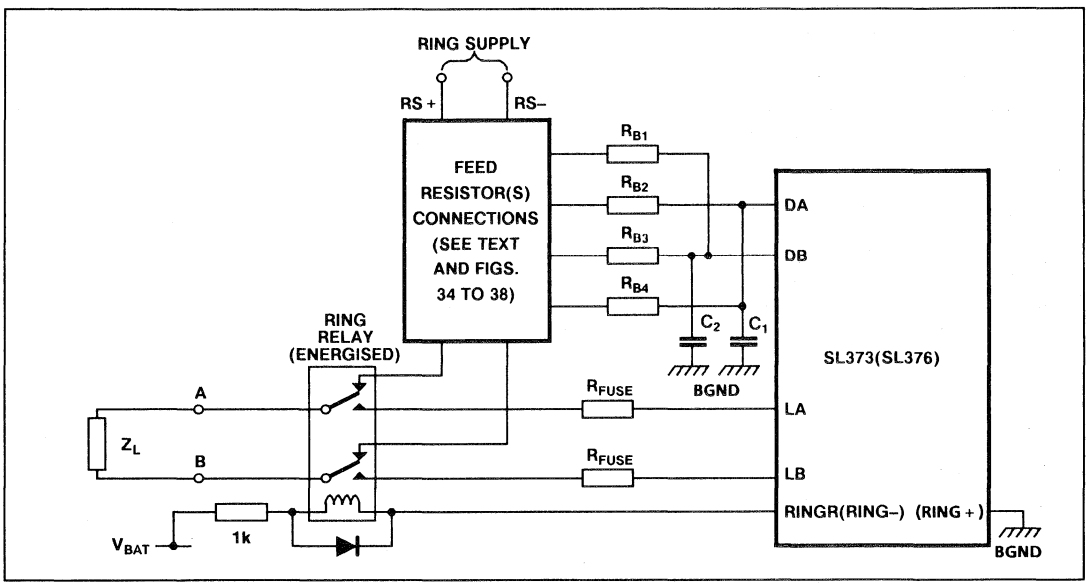


Fig. 33 General connections for ringing mode (SL376 differences shown in brackets)

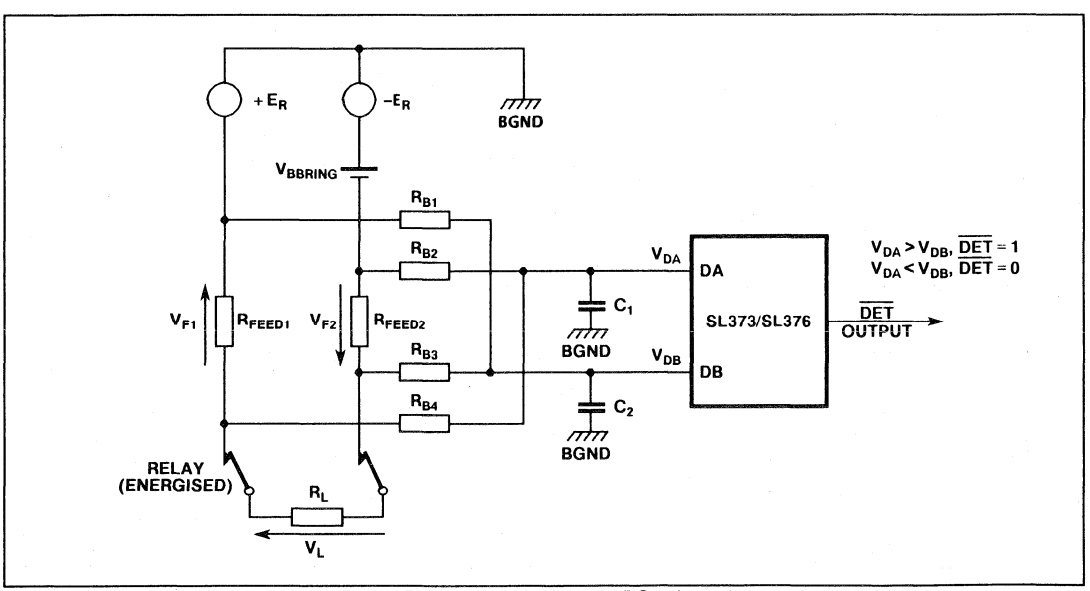


Fig. 34 Balanced ringing circuit (DC voltages) .

equal so that we can use $R_{FEED1} = R_{FEED2} = R_F$ and $V_{F1} = V_{F2} = V_F$. For the DC voltages at DA and DB, we can now write the following :

$$V_{DA} = \frac{(R_{B2})(V_F + V_L)}{(R_{B2} + R_{B4})} \quad ....(1)$$

$$V_{DB} = \frac{(R_{B3})(V_F + V_L)}{(R_{B1} + R_{B3})} + V_F \quad ....(2)$$

Assuming that the bridge resistors R_{B1}-R_{B4} are all $\geqslant R_F$, R_L (R_{B1}-R_{B4} ~few hundred kΩ), then:

$$V_F \approx \frac{V_{BBRING} R_F}{(R_L + 2R_F)} \quad ....(3)$$

$$V_L \approx \frac{V_{BBRING} R_L}{(R_L + 2R_F)} \quad ....(4)$$

At the Ring Trip threshold, $R_L = R_{LTH}$ is the line impedance at the threshold below which Ring Trip is indicated, with $V_L = V_{LTH}$ the associated line voltage. Also, $V_{DA} = V_{DB}$ must be valid at $R_L = R_{LTH}$. Equating eqn. (1) with (2) and using (3) and (4) to obtain V_{FTH} and V_{LTH} (i.e. voltages at threshold), we can solve for R_{LTH} so that:

$$R_{LTH} = \frac{(2R_{B3}R_{B4} + R_{B1}R_{B4} + R_{B2}R_{B3})R_F}{(R_{B1}R_{B2} - R_{B3}R_{B4})}$$

We can make $R_{B1} = R_{B2}$ and $R_{B3} = R_{B4}$ so that we can rewrite the above as:

$$R_{LTH} = \frac{2R_{B4}R_F}{(R_{B1} - R_{B4})} \quad ....(5)$$

with $R_{B4} < R_{B1}$ for the circuit to work. Note that since the DC feed resistance is just $2R_F$, we can rewrite (5) as :

$$R_{LTH} = \frac{R_{B4}(\text{Total Feed Resistance})}{(R_{B1} - R_{B4})} \quad ....(6)$$

BALANCED RINGING - AC

The capacitors C_1 and C_2 in Fig. 30 reduce the amplitude of the AC ringing voltage at DA and DB respectively. In the case of Balanced Ringing and dual feed resistors, we can consider the circuit for AC voltages as that shown in Fig. 35.

If we assume that $C_1 = C_2 = 0$, then we can write for the AC voltages at v_{DA} [$v_{DA(0)}$] and v_{DB} [$v_{DB(0)}$]:

$$v_{DA(0)} = \frac{[R_L(R_{B2} - R_{B4}) - 2R_{F1}R_{B4}]E_R}{(R_{B2} + R_{B4})(2R_{F1} + R_L)}$$

$$v_{DB(0)} = \frac{-[R_L(R_{B1} - R_{B3}) - 2R_{F1}R_{B3}]E_R}{(R_{B1} + R_{B3})(2R_{F1} + R_L)}$$

Including C_1 and C_2 in the circuit (i.e. $C1 \neq 0$, $C2 \neq 0$), we can write for the AC voltages at DA and DB:-

$$v_{DA} = \frac{R_{B2}}{(R_{B2} + R_{B4}) + j\omega C_1 R_{B2} R_{B4}} \left(\frac{(R_{F2} - R_{F1} + Z_L)}{(R_{F2} + R_{F1} + Z_L)} - \frac{R_{B4}}{R_{B2}} \right) E_R$$

$$v_{DB} = \frac{R_{B1}}{(R_{B1} + R_{B3}) + j\omega C_2 R_{B1} R_{B3}} \left(\frac{(R_{F1} - R_{F2} + Z_L]}{(R_{F1} + R_{F2} + Z_L)} - \frac{R_{B3}}{R_{B1}} \right) E_R$$

Thus we can determine that C_1 reduces $V_{DA(0)}$ by a factor :

$$\tau_1 = [1 + (\omega C_1 R_X)^2]^{-\frac{1}{2}} \quad ..(7)\ R_X = (R_{B2}R_{B4})(R_{B2} + R_{B4})$$

and that C_2 reduces $V_{DB(0)}$ by a factor :-

$$\tau_2 = [1 + (\omega C_2 R_Y)^2]^{-\frac{1}{2}} \quad ..(8)\ R_Y = (R_{B1}R_{B3})(R_{B1} + R_{B3})$$

For Balanced Ringing we have $R_{F1} = R_{F2}$, and we have chosen $R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$ so that $v_{DA} = v_{DB}$ and we can make $C_1 = C_2$. Alternatively, since the AC voltages at v_{DA} and v_{DB} are the same, C_1 and C_2 can be replaced by a single capacitor connected between DA and DB, wih a value of $C_1C_2 \div (C_1 + C_2)$.

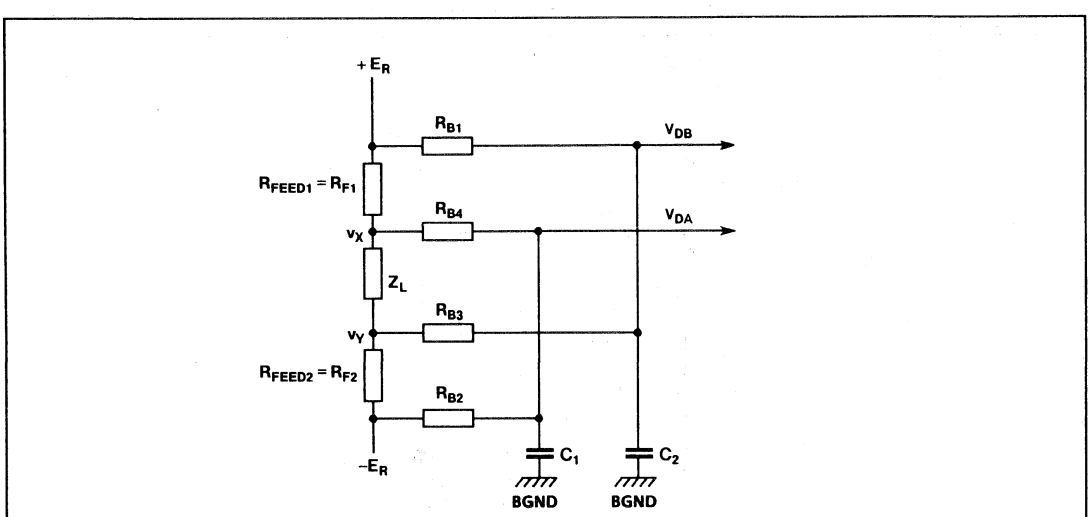


Fig. 35 Balanced ringing circuit (AC voltages)

UNBALANCED RINGING - DC

The circuit for Unbalanced Ringing can be considered as that of Fig. 36 for DC voltages. This is equivalent to the Balanced case with $R_{F2} = 0$ and an unbalanced AC source. Considering DC voltages only, we obtain the same result as equation (6) for Balanced Ringing, with a total feed resistance of R_{F1}, i.e:-

$$R_{LTH} = \frac{R_{B4}R_{F1}}{(R_{B1}-R_{B4})}$$

UNBALANCED RINGING - AC

As with the Balanced case, we can write for the AC voltages at the comparator inputs with $C_1 = C_2 = 0$:-

$$v_{DA(0)} = \frac{[R_{F1}(R_{B2} + R_{B4}) + R_{B4}R_L](-E_R)}{(R_{B2} + R_{B4})(R_{F1} + Z_L)}$$

$$v_{DB(0)} = \frac{(R_B)(-E_R)}{(R_{B1} + R_{B3})}$$

Again, if we include C_1 and C_2 ($\neq 0$), then we obtain :-

$$v_{DA} = \frac{R_{B2}}{(R_{B2} + R_{B4}) + j\omega C_1 R_{B2} R_{B4}} \left[\frac{(R_{F1})}{(R_{F1} + Z_L)} + \frac{R_{B4}}{R_{B2}}\right] - E_R$$

$$v_{DB} = \frac{R_{B1}(-E_R)}{(R_{B1} + R_{B3}) + j\omega C_2 R_{B1} R_{B3}}$$

We can again determine that C_1 reduces the ac voltage at DA by a factor τ_1, as in equation (7), and C_2 reduces the

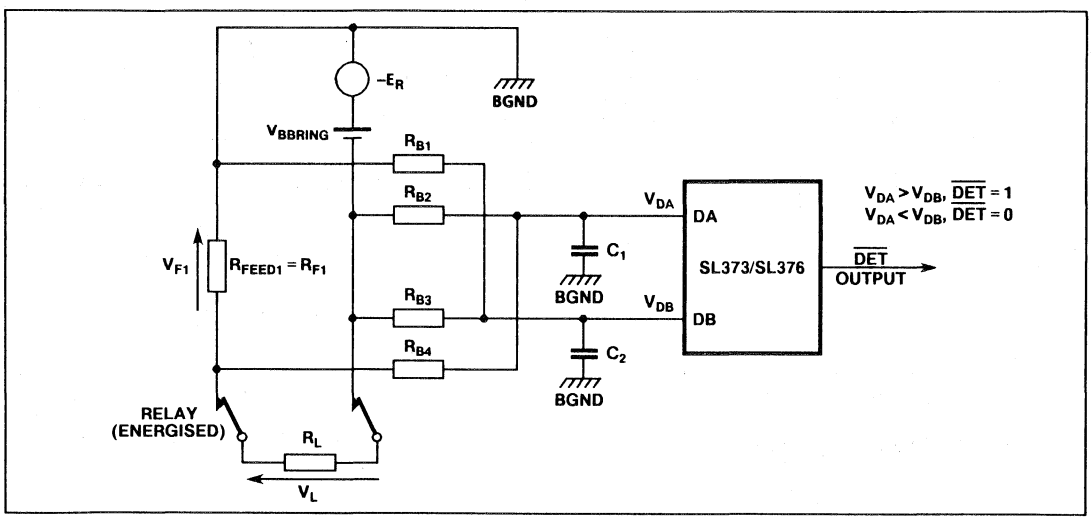


Fig. 36 Unbalanced ringing circuit (DC voltages)

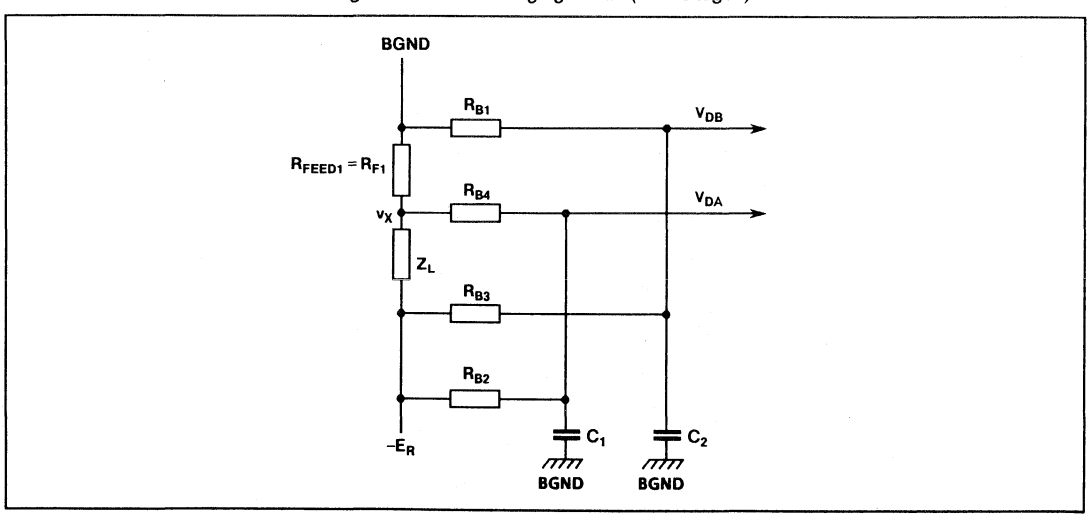


Fig. 37 Unbalanced ringing circuit (AC voltages)

AC voltage at DB by a factor τ_2, as in equation (8). Lastly, note that we can dispense with the capacitor C_2 if we reconfigure the circuit of Fig. 36 as that of Fig. 38, since there is now no AC at the DB pin.

CAPACITOR VALUES

Both C_1 and C_2 (C_1 only for Fig. 38) should be chosen to satisfy two criteria. The first is to reduce the amplitude of the ringing signal at DA and DB, thus preventing the voltages at these pins going outside the safe range for the SLIC (0-V_{BB}). Secondly, C_1 and C_2 reduce the possibility of the $\overline{DET}$ output toggling at line resistances near the Ring Trip threshold. The values of C_1 and C_2 are determined from (7) and (8). However, as the capacitor values increase, this increases the time taken to detect Ring Trip. Thus, to detect Ring Trip within a given time (100ms say), then the time constant of these capacitors must be kept within this limit. For Balanced Ringing, this gives a time t set by:

$$t = \frac{(R_{B1}R_{B4})(C_1C_2)}{(R_{B1}+R_{B3})(C_1+C_2)}$$

assuming $R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$ and for Unbalanced Ringing we get:

$$t = \frac{(R_{B1}R_{B4})(C_1)}{(R_{B1}+R_{B3})}$$

FEED RESISTORS

The Feed Resistors R_{F1} and R_{F2} (or just R_{F1}) provide the DC Feed for the ringing circuit, and as such, will dissipate power according to the value of the total feed resistance (R_F), Line Resistance (R_L) and Battery Voltage (V_{BBRING}). For an example consider $R_{FTOT} = 800\Omega$ with $V_{BBRING} = -48V$. With a line resistance of 600Ω, then a current of 34.3mA will flow in R_{FTOT}. The power dissipated is then 0.94W. Thus, for Balanced Ringing, each resistor will need to be rated at $\frac{1}{2}$W, or greater, and for Unbalanced Ringing R_{F1} will need to be rated at ≥1W.

Note that the power dissipation, P_D, follows the relationship:

$$P_D = \frac{V_{BBRING}^2}{(R_L+R_F)}$$

and $V_{BBRING} = V_{BAT}$ in most cases.

OVERVOLTAGE PROTECTION-RINGING CIRCUIT

Overvoltage protection for the Ringing Circuitry must be provided in a similar way as for the normal line connection (Ring Relay de-energised), as described on pages 7-42 and 7-43.

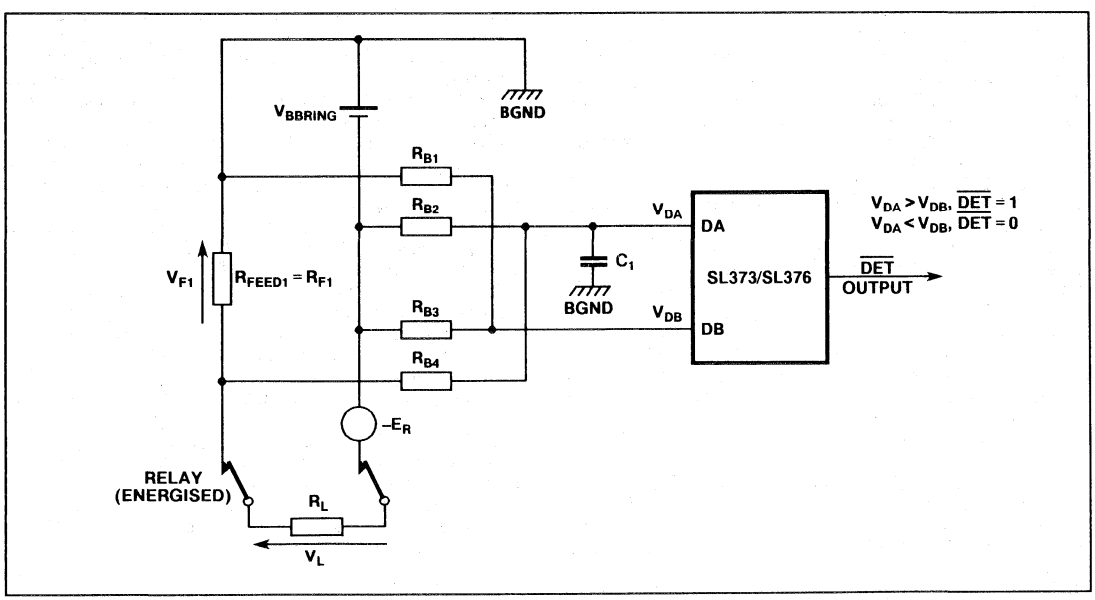


Fig. 38 : Alternative unbalanced ringing circuit (DC voltages)

APPLICATIONS GENERAL CONSIDERATIONS

SLIC OPERATING MODES

When used in a system, both the SL373 and SL376 SLICs provide the designer with a number of operating modes for system flexibility. This section describes how these modes are intended for use in a real system.

Firstly, both SLICs provide an Active and a Standby mode with normal LA/LB (i.e. Tip/Ring) or reversed polarity. For normal polarity, the LA pin is positive and for reverse it is negative. Apart from DC line polarity, the normal and reverse Active Modes are identical. This is also true of the normal and reverse polarity Standby Modes.

For most of the time, the served subscriber that is connected to the SLIC, will be On-Hook. Both of the SLICs provide a low power Standby Mode of operation keeping power consumption/dissipation by the SLIC to a minimum. It is intended that this Standby mode will only be used during On-Hook conditions. Note that the implementation of Standby is different for the two SLICs. Additional power saving is available by use of the SL376, which turns off the Voltage Regulator during Standby Mode. However, the Regulator is designed to limit power dissipation by the device by matching the required 2-wire DC voltage to the supplied regulator voltage. The difference between the regulator and battery voltages will be larger at lower line resistances, i.e. Off-Hook. If the SL376 thus remains in Standby Mode when the subscriber has gone Off-Hook, then a significant amount of power dissipation may occur because the Regulator (in Standby) is inoperative. This will not normally be a problem, since under all normal conditions the system will change the SLIC operating mode to Active, turning on the Voltage Regulator. It is therefore important that the system ensures the SL376 does not remain in Standby mode for Off-Hook status, excepting a short period before this condition is first recognised. Note that since the SL373 Voltage Regulator is always operative, then the above constraint does not apply and that the SL376 Standby power dissipation will for most times be greater than the SL373.

Once Off-Hook has been detected, then the SLIC should be put into Active Mode. This brings to light a second difference between the two SLICs. That is, the SL373 is a constant current feed device at low line resistance, whilst the SL376 is a resistive feed function. Both devices, however, have a constant voltage region (between pins LA and LB) at high line resistance. Setting up the parameters relating to Standby and Active Modes is fully described in the respective Data Sheets, with further information given in the Hardware Programming of SLIC Parameters section of this Applications Note. Note that some transmission parameters are degraded when the DC saturation guard region is entered and this may influence the choice of battery voltage for the system.

Both SLICs contain a Ring Relay Driver. The nature of the driver is different for each SLIC, as described in the related Data Sheet. The SLIC can be placed in Ringing mode via the Digital Interface, activating the Ring Relay Driver and setting the SLIC to determine Ring Trip. For this mode, DC and AC ringing supply voltages are external to the SLIC, which may be Balanced or Unbalanced in nature, as described in the Ring Trip Circuits section.

Other modes of operation are possible with each SLIC allowing the Line Card to be set to determine Ground Start conditions in Disconnect A Standby B Mode. This disconnects the A Leg from the line whilst the B leg is in Standby. Additionally, both SLICs can be placed in Disconnect Mode, which isolates the LA and LB pins from the Line (high impedance). Finally, the SL373 only has one additional mode whereby a second relay can be activated to facilitate Test Access. Connections for this are described later in this section.

OVERVOLTAGE PROTECTION

Neither the SL373 or SL376 is provided with on-chip overvoltage protection. This must be provided externally for all SLIC modes. In addition, any external Ring Supply circuits will need similar protection. Fig. 39 shows how such protection against lightning strikes and induced high voltage AC signals (e.g. mains) might be implemented.

The components P_1 and P_2 are primary protection devices which absorb the main energy of a lightning strike. They must be able to turn on at about 300V and absorb a few thousand amps (intermittent). However, since a lightning strike can produce very fast rising edges, some energy (possibly ~1500V/1.5A) can leak past P_1 and P_2, depending on the components used. In addition, induced AC below the P_1/P_2 turn-on voltage will also get past. For this reason, secondary protection must be provided by a combination of fuse/protection resistors ($R_{FUSE1/2}$,$R_{P1/2}$) and diodes to protect the SLIC LA and LB pins against damage.

The protection resistors ($R_{P1/2}$) must be able to absorb the remaining energy from lightning strikes. Any separate fuse resistors ($R_{FUSE1/2}$) must go open circuit in the event of a continuous induced AC (~ >1 Sec.), which might otherwise destroy the protection resistors. In addition, it is important that the fuse (& protection) resistors are matched to limit their degradation of Longitudinal Balance. Thus matching must be in the order of $(R_{FUSE1} + R_{P1}) = (R_{FUSE2} + R_{P2})(1.005)$ i.e. ½%. R_{F1} and R_{P1} (also R_{F2} and R_{P2}) may be combined so long as open circuit behaviour is not impaired, thus protecting the voltage limiting components (D_{P1}-D_{P5},S_1) at the LA/LB pins.

Protection of the SLIC LA/LB pins is provided by the voltage limiting components D_{P1}-D_{P5},S_1. Thus, the forward voltage of D_{P1}/D_{P2} protects LA/LB against voltages above BGND by the forward voltage drop, with a current handling capacity to match the remaining energy of a lightning strike. Diodes D_{P3}, D_{P4}, D_{P5} and the SCR (S_1) provide similar protection from voltages below BGND by an amount $(\geq |V_{BAT}|)$ $V_{DP3} + V_{S1} + V_{DP5}$ (or $V_{DP4} + V_{S1} + V_{DP5}$) where V_{DP3}/V_{DP4} are the forward voltages of D_{P3}/D_{P4}, V_{DP5} is the zener voltage and V_{S1} is the gate voltage of the SCR. S_1 provides reduction of power dissipation in D_{P5} at high currents and D_{P1}-D_{P4} may be combined with the use of a standard bridge rectifier (~3/5A).

In deciding the value of protection devices to use, reference can be made to surge specifications CCITT K17, FCC part 68 or REA Form 522a.

VOLTAGE SUPPLIES

The SLIC uses supplies of V_{CC}, V_{EE}, V_{BAT}, AGND and BGND, operating ranges of which are given in the associated data sheets. To help avoid possible SLIC

damage and ensure correct operation after applying power, it is recommended to connect the supplies in the following order: BGND/AGND, V_{BAT} then V_{CC}/V_{EE}.

Additionally, care should be taken in the rate of change in V_{BAT} upon application of this supply. This is because of the charging current to the capacitor at the substrate pin (C_4 Figs. 28/29) which may cause SLIC damage if the current is too great. The maximum rate of change of V_{BB} is specified in the relevant SLIC Data Sheet. If the voltage change of the circuit is too great, this may be limited by a small resistance in series with the V_{BAT} supply (≈10Ω) and a capacitance, ≈1μF, to ground. This resistance can be switched out of circuit after a given delay. The cause of this ∂V/∂t limit is the charge path for C_4, the substrate capacitor, via VBB and SUB.

TEST ACCESS

Access to the line for test purposes is achieved via an external Test Relay. For the SL373 this can be energised via the SLIC D3 digital input (=0V) and using the on-chip Test Relay Driver, whereas for the SL376, this must be done external to the SLIC. The SL373 data sheet shows how the Test Relay can be connected into the line (which is relevant for the SL376 excepting relay driver) providing Test Access to the line only (A/B). However, additional Test Access to both LA/LB pins and A/B can be provided by using the circuit of Fig. 40.

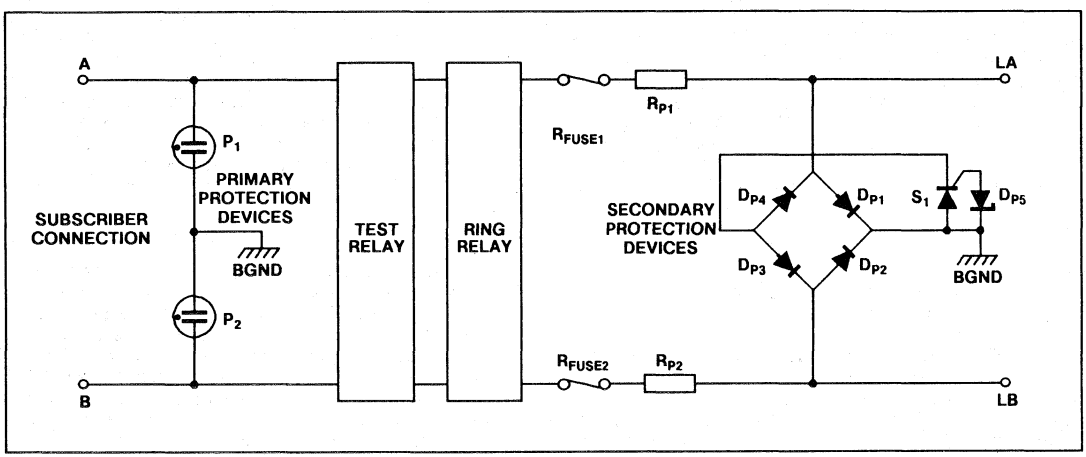


Fig. 39 Overvoltage protection

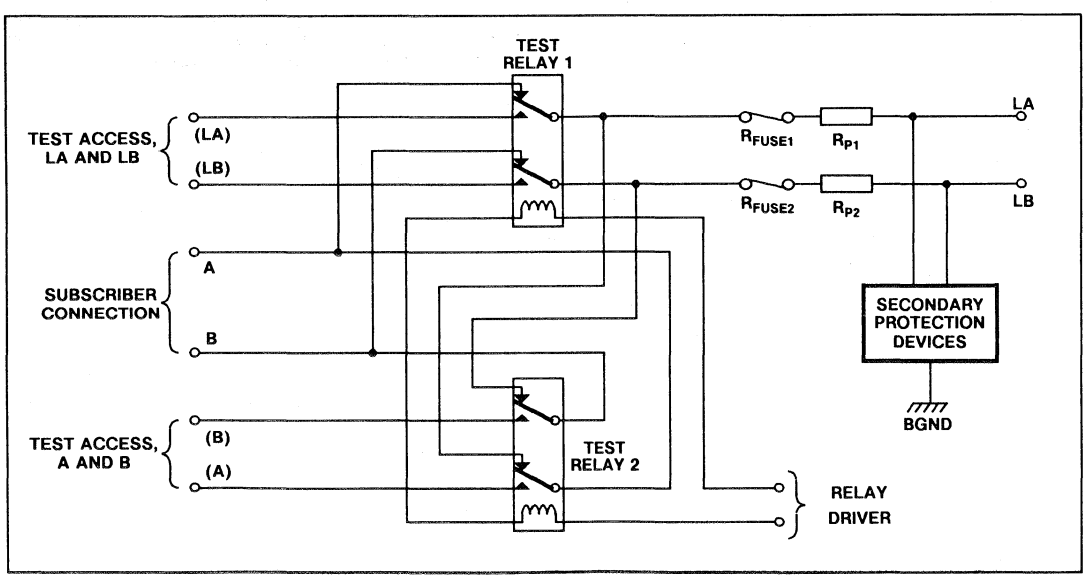


Fig. 40 Test access circuit

TEST RELAY DRIVER - SL373

This relay driver may be used in the manner described earlier in the TEST ACCESS section. However, there is no reason why this relay driver cannot perform some other function. For example, it may be used to allow the SLIC to access another subscriber line should its own be determined as faulty by the system hardware. Indeed, some designs may prefer to keep any test access separate from the SLIC so as to always be able to test the line, even if the SLIC may have suffered damage (e.g. from overvoltage) and the relay driver be inoperative.

AC/DC SEPARATION CAPACITOR

The value and quality of the AC/DC separation capacitor (C_{HP}, Figs. 41 and 42) can affect the stability of the DC control loop and have consequences on the transmission parameters, in several ways. This section discusses the issues regarding component choice.

Internal to the SLIC, the capacitor C_{HP} has 200kΩ resistors connecting each side of this component to the LA and LB legs (shown in the conceptual DC Power Feed Circuit Model of the SLIC Data Sheets), and can be considered as 400kΩ in series. The associated circuitry internal to the device contains a 90° phase shift. The roll-off in frequency required to maintain DC stability is set by the value of C_{HP} and the 200kΩ resistors. This roll-off in the DC control loop is set in conjunction with the roll-off in the R_{DC}/C_{DC} network at the Rdc pin (used to filter chopper noise from this output). If there is a frequency at which the roll-off of the R_{DC}/C_{DC} network exhibits significant phase shift, which then adds to the 90° from C_{HP}, with a net gain round the DC control loop from both networks >1, then a classic type of oscillator can result.

The circuits presented in this Application Note (Figs. 3, 8, 41 and 42) have been designed to ensure that the above problem does not occur. As a reasonable guide, keep the roll-off of the two networks involved separated by ~100Hz (e.g. the SL373 circuit of Fig. 3 uses ~1.2Hz for C_{HP} and ~100Hz for R_{DC}/C_{DC}). Thus, if C_{HP} is reduced in value, C_{DC} should be scaled accordingly. However, care should be taken in choosing this value, as a reduction in C_{DC} may have other consequences.

Firstly, reducing C_{HP} may cause a degradation in the SLIC frequency response. A value of 150nF will cause ~0.11dB variation, falling on the limit of the SLIC specification. Secondly, an increase in chopper noise may result due to the necessary scaled reduction in C_{DC}, as discussed earlier. Finally, on long lines/low battery voltages (i.e. saturation guard is active) a degradation of 4-wire-longitudinal balance may result. Although the DC control loop is unaffected, an internal mechanism can allow 4-wire signals to modulate the longitudinal balance point. This effect becomes more apparent with reductions in C_{HP} and an active saturation guard circuit.

In addition to considering the effects of changing the value of C_{HP}, care must be taken in deciding the quality of this component, particularly in surface mount applications. The internal 200kΩ resistors associated with C_{HP} also have an SCR type structure connected across the terminals. Thus, if any leakage current through C_{HP} (discharging the capacitor slightly), sufficient to cause ~0.5V across these resistors, then the associated SCRs may be triggered. The C_{HP} capacitor is now recharged to the full DC separation voltage, and the discharge process starts again- oscillations then result. To ensure that this situation does not occur, then C_{HP} should exhibit >100MΩ resistance at 63V. It is important to remember that the resistance is specified at high voltage, since this is what the capacitor must tolerate in this application.

PCB LAYOUT

In addition to the Switching Regulator considerations (as outlined earlier), care must be taken with the PCB layout with regard to the RSN and AGND pins of the SLIC. Since RSN is a high gain current input, it is sensitive to noise pickup. In addition, any noise at AGND may be injected into the transmission paths. For this reason, an AGND plane would be advisable, which must then be separate from BGND. It is also best to use BGND as a digital ground to avoid injection of switching transients.

APPLICATION CIRCUIT SUMMARY

Given in the following pages are complete Application Circuits for the SL373 and SL376 (Figs. 41 and 42) with component values in Tables 3 and 4, respectively.

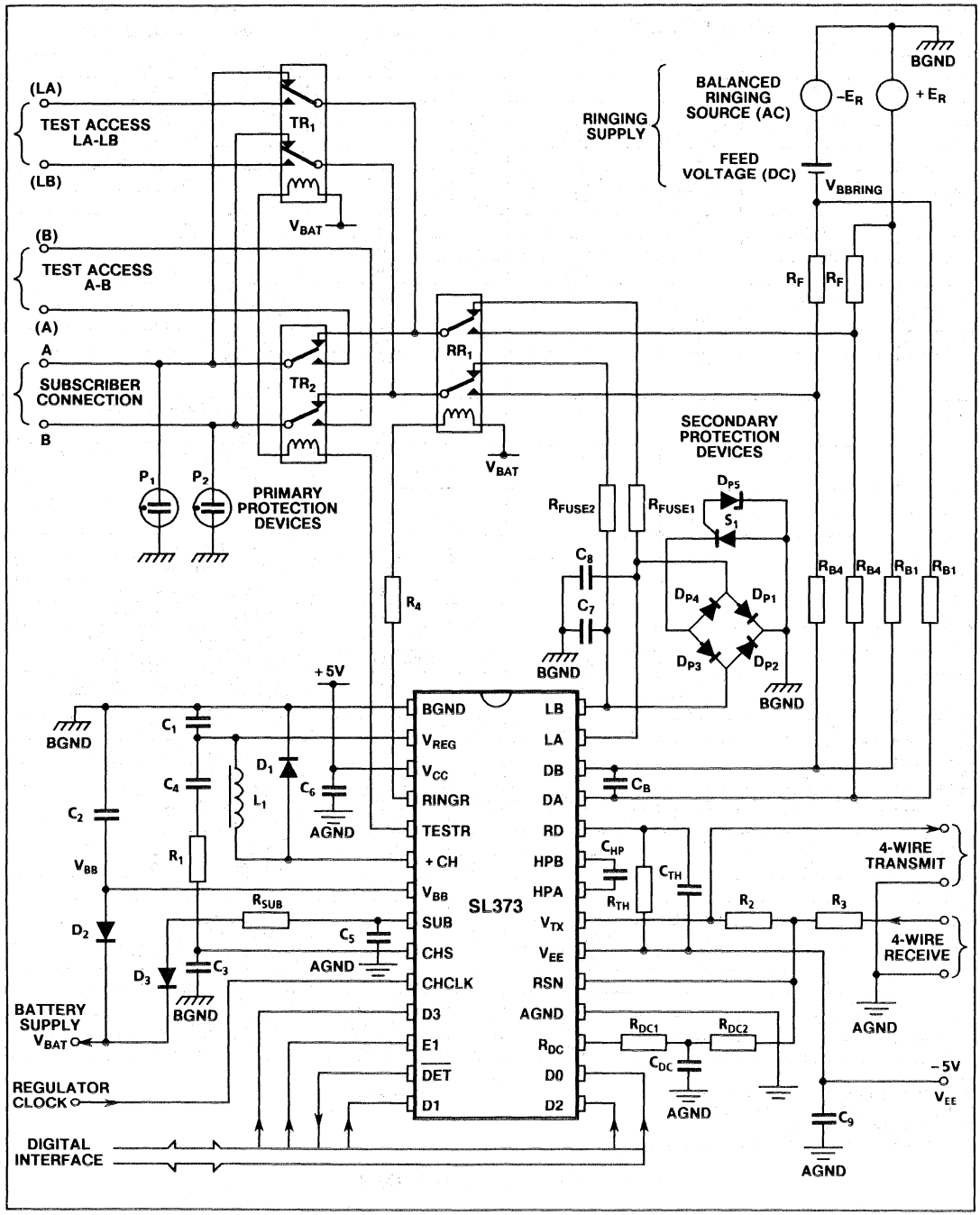


Fig.41 SL373 application circuit (see text, data sheet and Table 3 for details)

Name	Component Value			Unit	Rating	Component Description
	Min	Typ	Max			
C_1	-20%	470	+20%	nF	100V	Switching Regulator Capacitor
C_2	-20%	470	+20%	nF	100V	V_{BB} Pin Filter Capacitor
C_3	-10%	560	+10%	pF	100V	Chopper Stability Network Capacitor
C_4	-20%	8.2	+20%	nF	100V	Substrate Decoupling Capacitor
C_5	-20%	330	+20%	nF	100V	Chopper Stability Network Capacitor
C_6	-20%	100	+20%	nF	100V	V_{CC} Filter Capacitor
C_7	-5%	10	+5%	nF	800V	LB Filter Capacitor
C_8	-5%	10	+5%	nF	800V	LA Filter Capacitor
C_9	-20%	100	+20%	nF	100V	V_{EE} Filter Capacitor
C_B	-5%	100	+5%	nF	100V	Ring Trip AC Filter Capacitor
C_{DC}	-10%	100	+10%	nF	100V	R_{DC} Filter Capacitor
C_{HP}	-20%	330	+20%	nF	100V	AC/DC Separation Capacitor
C_{TH}	-20%	10	+20%	nF	50V	Off-Hook Filter Capacitor
D_1	-	100	-	V	100mA	Regulator Diode, 10ns recovery; e.g. 1N4148
D_2	-	100	-	V	100mA	$V_{LA}/V_{LB} < V_{BB}$ Protection, 10ns recovery; e.g. CV9637
D_3	-	100	-	V	100mA	C_5 Charging Diode, 10ns recovery; e.g. 1N4002
D_{P1}	-	1.0	-	V	5A	V_{LA} > BGND Protection Diode
D_{P2}	-	1.0	-	V	5A	V_{LB} > BGND Protection Diode
D_{P3}	-	1.0	-	V	5A	$V_{LB} < V_{BB}$ Protection Diode [3]
D_{P4}	-	1.0	-	V	5A	$V_{LA} < V_{BB}$ Protection Diode [3]
D_{P5}	-	62.0	-	V	1.3W	Zener Diode (Max I_R = 200mA)
L_1	-	1.0	-	mH	100mA	Switching Regulator Inductor
P_1	210		320	V	800V 5kA-10µs	Surge Arrester (for CCITT 8/20)
P_2	210		320	V	800V 5kA-10µs	Surge Arrester (for CCITT 8/20)
R_1	-2%	2.4	+2%	kΩ	0.25W [1]	Chopper Stability Network Resistor
R_2	Note 4	640	Note 4	kΩ	0.25W [1]	2 Wire Termination Resistor
R_3	Note 4	320	Note 4	kΩ	0.25W [1]	4 Wire Receive Gain Resistor
R_4	-5%	1.0	+5%	kΩ	1W [2]	Relay Coil Current Limit Resistor
R_{B4}	-5%	1.11	+5%	MΩ	0.125W [1]	Ring Trip Bridge Resistor
R_{B1}	-1% of $1.288 \times R_{B1}$	1.43	+1% of $1.288 \times R_{B1}$	MΩ	0.125W [1]	Ring Trip Bridge Resistor
R_{DC1}	-1%	31.25	+1%	kΩ	0.125W [1]	Active Mode Constant Current Resistor
R_{DC2}	-1%	31.25	+1%	kΩ	0.125W [1]	Active Mode Constant Current Resistor
R_F	-1%	510	+1%	Ω	0.5W	Ring Mode Feed Resistance = $2R_F$
R_{FUSE1}	-5%	20	+5%	Ω	1500V/1.5A	Fuse Resistor
R_{FUSE2}	$0.995 \times R_{FUSE1}$	R_{FUSE1}	$1.005 \times R_{FUSE1}$	Ω	1500V/1.5A	Fuse Resistor
R_{SUB}	-5%	100	+5%	Ω	0.25W	C_5 Charging Resistor
R_{TH}	-2%	32	+2%	kΩ	0.125W [1]	Off-Hook/Standby Resistor
RR_1	17.2		36.0	V	30W/50VA	DPDT Relay 1050Ω Coil
S_1		3.0		V	100.0mA	SCR, 13A I_T
TR_1	17.2		36.0	V	30W/50VA	DPDT Relay 1050Ω Coil
TR_2	17.2		36.0	V	30W/50VA	DPDT Relay 1050Ω Coil

NOTES
1. Suggested rating may be smaller if required; e.g. Surface Mount applications.
2. Rating depends on Relay used.
3. In association with D_{P5} and S_1.
4. Tolerance depends on gain accuracy required.

Table 3 Component values for Fig. 41

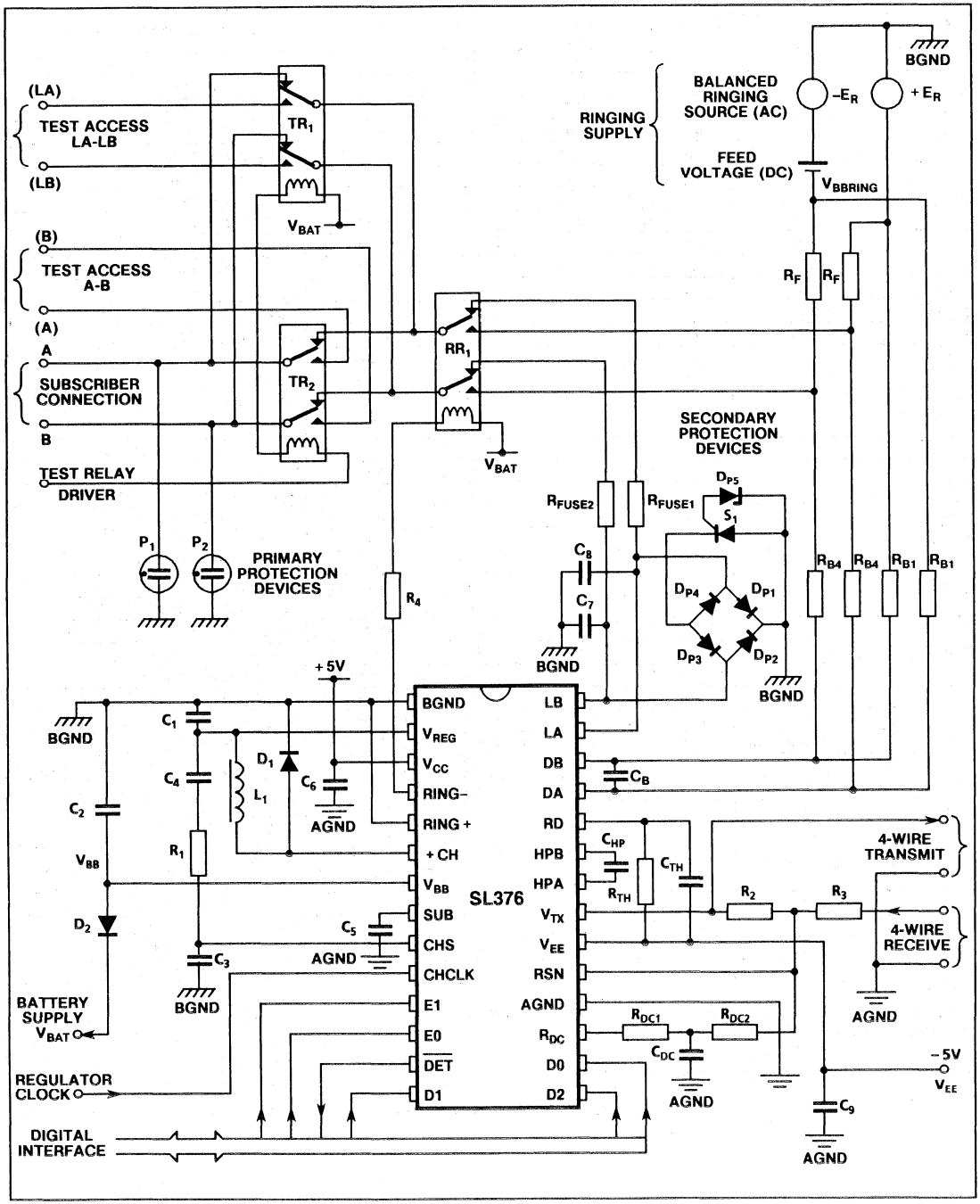


Fig.42 SL376 application circuit (see text, data sheet and Table 4 for details)

Name	Component Value			Unit	Rating	Component Description
	Min	Typ	Max			
C_1	-20%	470	+20%	nF	100V	Switching Regulator Capacitor
C_2	-20%	470	+20%	nF	100V	V_{BB} Pin Filter Capacitor
C_3	-10%	560	+10%	pF	100V	Chopper Stability Network Capacitor
C_4	-20%	8.2	+20%	nF	100V	Substrate Decoupling Capacitor
C_5	-20%	330	+20%	nF	100V	Chopper Stability Network Capacitor
C_6	-20%	100	+20%	nF	100V	V_{CC} Filter Capacitor
C_7	-5%	10	+5%	nF	800V	LB Filter Capacitor
C_8	-5%	10	+5%	nF	800V	LA Filter Capacitor
C_9	-20%	100	+20%	nF	100V	V_{EE} Filter Capacitor
C_B	-5%	100	+5%	nF	100V	Ring Trip AC Filter Capacitor
C_{DC}	-10%	100	+10%	nF	100V	R_{DC} Filter Capacitor
C_{HP}	-20%	330	+20%	nF	100V	AC/DC Separation Capacitor
C_{TH}	-20%	10	+20%	nF	50V	Off-Hook Filter Capacitor
D_1	-	100	-	V	100mA	Regulator Diode, $10n_S$ recovery; e.g. 1N4148
D_2	-	100	-	V	100mA	$V_{LA}/V_{LB} < V_{BB}$ Protection, $10n_S$ recovery; e.g. CV9637
D_{P1}	-	1.0	-	V	5A	$V_{LA} >$ BGND Protection Diode
D_{P2}	-	1.0	-	V	5A	$V_{LB} >$ BGND Protection Diode
D_{P3}	-	1.0	-	V	5A	$V_{LB} < V_{BB}$ Protection Diode [3]
D_{P4}	-	1.0	-	V	5A	$V_{LA} < V_{BB}$ Protection Diode [3]
D_{P5}	-	62.0	-	V	1.3W	Zener Diode (Max $I_R = 200mA$)
L_1	-	1.0	-	mH	100mA	Switching Regulator Inductor
P_1	210		320	V	800V 5kA-10µs	Surge Arrester (for CCITT 8/20)
P_2	210		320	V	800V 5kA-10µs	Surge Arrester (for CCITT 8/20)
R_1	-2%	2.4	+2%	kΩ	0.25W [1]	Chopper Stability Network Resistor
R_2	Note 4	320	Note 4	kΩ	0.25W [1]	2 Wire Termination Resistor
R_3	Note 4	320	Note 4	kΩ	0.25W [1]	4 Wire Receive Gain Resistor
R_4	-5%	1.0	+5%	kΩ	1W [2]	Relay Coil Current Limit Resistor
R_{B4}	-5%	1.11	+5%	MΩ	0.125W [1]	Ring Trip Bridge Resistor
R_{B1}	-1% of $1.288 \times R_{B1}$	1.43	+1% of $1.288 \times R_{B1}$	MΩ	0.125W [1]	Ring Trip Bridge Resistor
R_{DC1}	-1%	19	+1%	kΩ	0.125W [1]	Active Mode Constant Current Resistor
R_{DC2}	-1%	19	+1%	kΩ	0.125W [1]	Active Mode Constant Current Resistor
R_F	-1%	510	+1%	Ω	0.5W	Ring Mode Feed Resistance = $2R_F$
R_{FUSE1}	-5%	20	+5%	Ω	1500V/1.5A	Fuse Resistor
R_{FUSE2}	$0.995 \times R_{FUSE1}$	R_{FUSE1}	$1.005 \times R_{FUSE1}$	Ω	1500V/1.5A	Fuse Resistor
R_{TH}	-2%	56	+2%	kΩ	0.125W [1]	Off-Hook/Standby Resistor
RR_1	17.2		36.0	V	30W/50VA	DPDT Relay 1050Ω Coil
S_1		3.0		V	100.0mA	SCR, 13A I_T
TR_1	17.2		36.0	V	30W/50VA	DPDT Relay 1050Ω Coil
TR_2	17.2		36.0	V	30W/50VA	DPDT Relay 1050Ω Coil

NOTES
1. Suggested rating may be smaller if required; e.g. Surface Mount applications.
2. Rating depends on Relay used.
3. In association with D_{P5} and S_1.
4. Tolerance depends on gain accuracy required.

Table 4 Component values for Fig. 42

A Universal SLIC Evaluation Board

AN114

This Application Note describes the PCBAN114 board (see page 3-134) which can be used to evaluate any one of the range of GEC Plessey Semiconductors Subscriber Line Interface Circuits (SLICs). These include the SL373, SL374, SL376, SL7950 and SL7953. The design of the board allows it to be customised for the chosen SLIC device by selecting appropriate component values. The different types of relay connections used by the range of SLIC devices can be set using a DIL header plugged into an on-board socket in one of two orientations. The SLIC digital interface can be driven by an 8-way s.p.s.t. DIL switch or externally through the available connector. Lastly, the regulator circuit of the SLIC, operating at 256kHz, can be driven by an external clock of either 256kHz or 2048kHz by using an on-board divider circuit.

CONTENTS

HARDWARE DESCRIPTION

Fig. 1 shows a block diagram of the SLIC Evaluation Board, indicating the main areas of the circuit which are discussed in later sections. The components of the Overvoltage Protection, Ring Trip, Relays and Clock Select blocks are independent of SLIC type. Use of the Digital Options block allows a stand alone application (On-Board option) or control by an external test system (Off-Board option). Some components of the Regulator are used for certain SLIC types only and these are discussed separately. Finally, all power supply, 2-Wire and 4-Wire connections to the board are the same regardless of SLIC.

Choosing components of the 4-Wire block can be done to suit any requirement of a given PTT administration or other application. Since these vary widely, the board was designed to suit a basic 600Ω (i.e. resistive impedances) system and can easily be populated with appropriate component values, as discussed in later sections. Thus the PCB hole pattern was chosen to suit this requirement, keeping component density as high as possible for improved transmission characteristics. Also note that although following sections give components with set values for the DC and Detector block, these may be changed according to the relevant description in the appropriate device data sheet (i.e. for Ring Trip threshold, Off-Hook threshold, Standby current level, DC Feed conditions, 2Wire termination and Receive Gain).

To summarise, the design of of the PCB will cater for any of the GEC Plessey Semiconductors range of SLIC devices and is flexible enough to be used with any requirement of programmable parameters. The SLIC options discussed in later sections assume the following conditions:-

> 600Ω 2-Wire line and termination (–6dB Transmit Gain), 0dB Receive gain, 40mA or 800Ω DC Feed, Off Hook at ~ 11mA, Ring Trip at ≤ ~3470Ω line with 6.24 reduction in AC voltage at DA/DB.

The circuit diagram of the evaluation board is shown in Fig. 2 with the PCB layout and component listing in Figs. 3 and 4, respectively.

RELAY CONNECTION OPTIONS (SK1)

The various possible connections from each of the SLIC devices are restricted to those which utilise the V_{BAT} and BGND rails. Two relays are mounted on the board for both Ring Trip and Test Access provision. Each SLIC contains either one or two relay drivers, one of which is always used for ringing mode supply feed. If only one driver is available from a SLIC, provision is made to drive the other (Test) relay from a switch on the PCB (SW1 Figs. 2/3).

In order to change the relay interconnect for the chosen SLIC, an 8-way DIL socket is used as a means of setting each option. Fig. 2 shows the associated circuit with SK1, whilst Fig. 5 shows how SK1 is used together with the means of operating both Ring Trip and Test Relays.

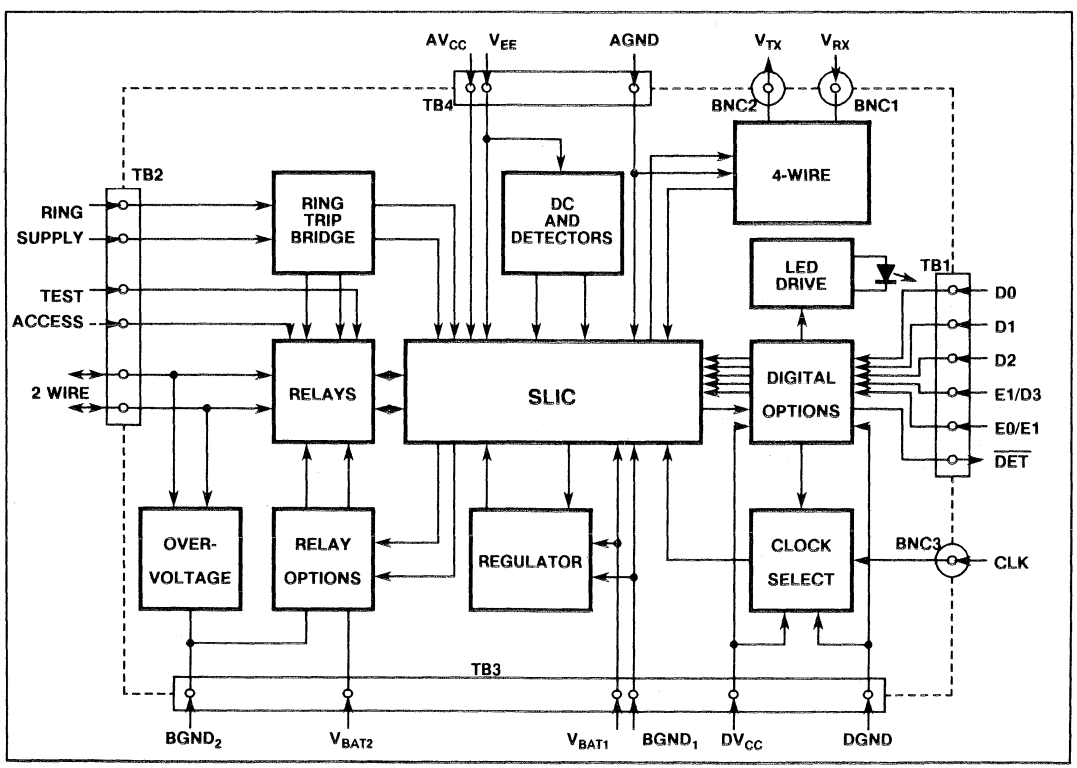


Fig. 1 Block diagram

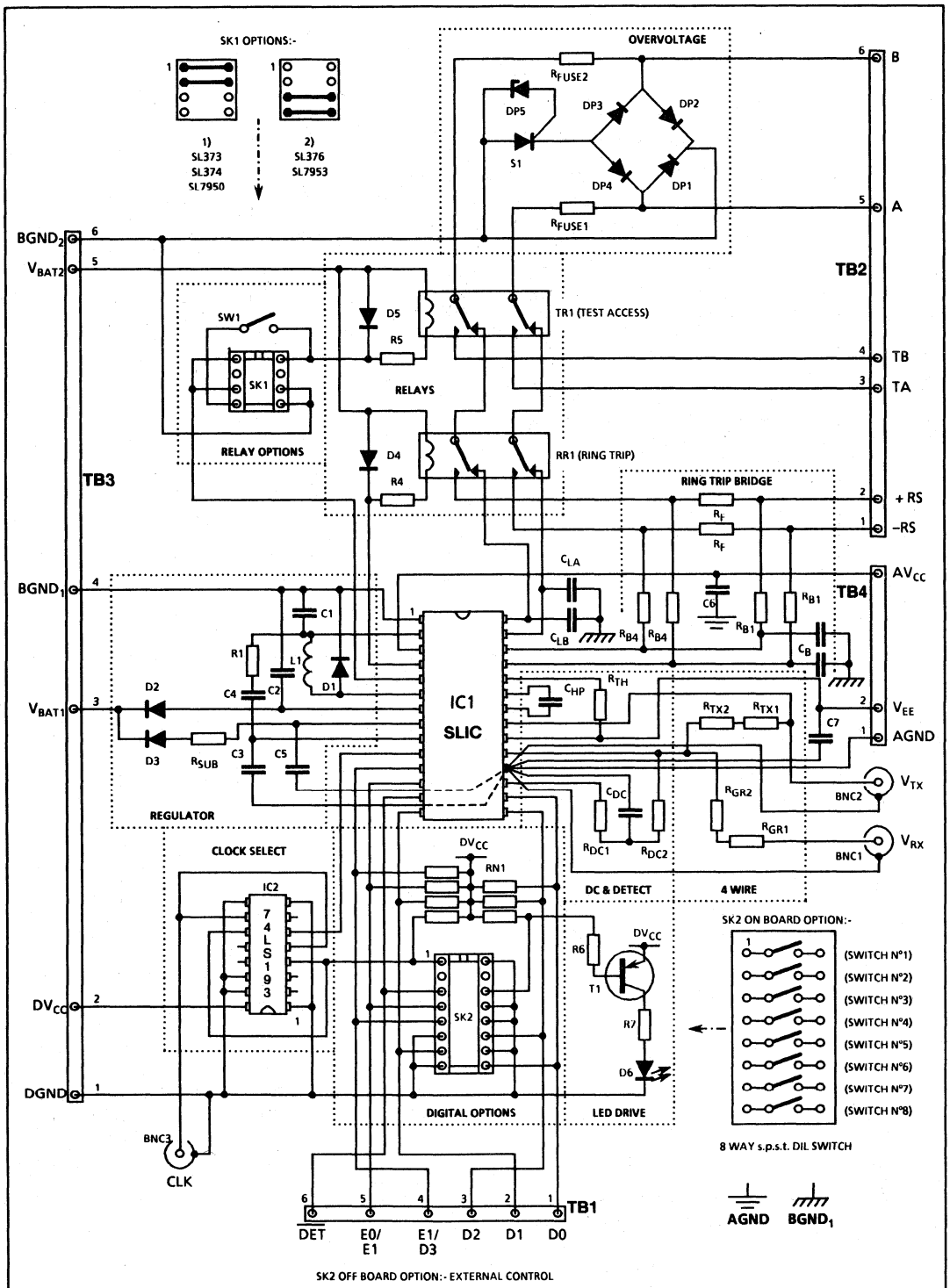


Fig. 2 Circuit diagram

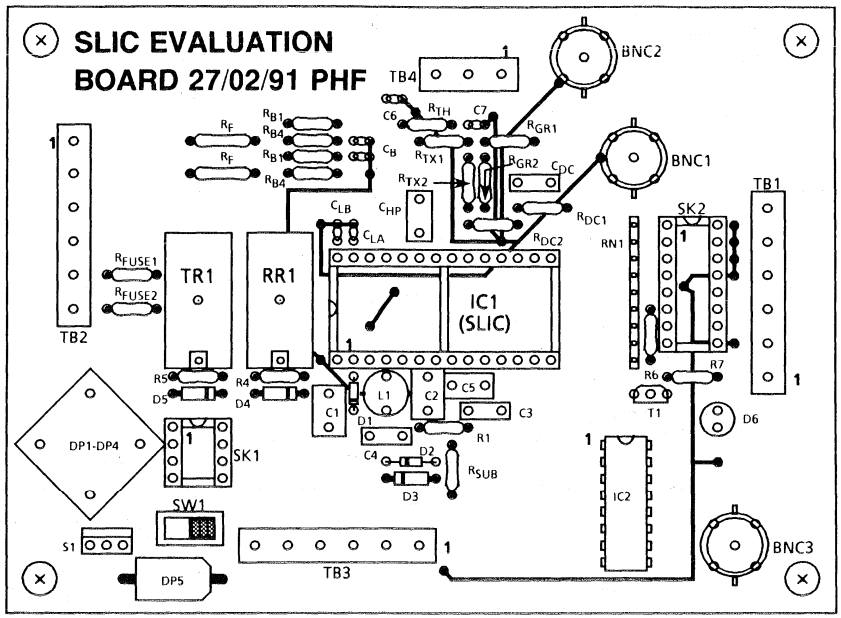


Fig. 3 PCB component layout.

NAME	VALUE	NAME	VALUE	NAME	VALUE
IC1	SLIC	R_{TX2}	†	D6	LED
IC2	74LS193	RN1	8 x 10kΩ	DP1 - DP4	KBPC102
R1	2.4kΩ	C1	470nF	DP5	BZTO3C62
R4	1kΩ	C2	470nF	L1	1mH 100mA
R5	1kΩ	C3	560pF	S1	BT152
R6	47kΩ	C4	8n2F	SK1	8-Way DIL Socket
R7	130Ω	C5	330nF	SK2	16-Way DIL Socket
R_{B1}	330kΩ	C6	100nF	SW1	s.p.d.t. Slide Switch
R_{B4}	270kΩ	C7	100nF	T1	2N3906
R_{DC1}	†	C_{LA}	10nF or 2.2nF #	TB1	6-Way Pluggable Terminal Blocks
R_{DC2}	†	C_{LB}	10nF or 2.2nF #	TB2	
R_F	390Ω	C_B	1 x 160 or 2 x 330 nF	TB3	
R_{FUSE1}	20Ω	C_{DC}	†	TB4	3-Way Pluggable Terminal Block
R_{FUSE2}	20Ω	C_{HP}	330nF		
R_{GR1}	†	D1	1N4148	BNC1	PCB BNC SOCKET
R_{GR2}	†	D2	1N4148	BNC2	PCB BNC SOCKET
R_{SUB}*	100Ω	D3*	1N4001	BNC3	PCB BNC SOCKET
R_{TH}	†	D4	1N4001	TR1	BT TYPE 47/7 RELAY
R_{TX1}	†	D5	1N4001	RR1	BT TYPE 47/7 RELAY

NOTES:- 1) Components listed as † are chosen according to the SLIC type used. Fig. 9 lists the values for a 600Ω line, 0dB Receive Gain and 40mA/800Ω DC feed.
2) Components marked with a * are only fitted for the SL373 and SL374.
3) Values of components marked with a # depend on SLIC type used (see Customised Components section).

Fig. 4 PCB components listing

REGULATOR CLOCK OPTIONS

The circuit of Fig. 2 shows use of a 74LS193 counter (IC2) associated with the clock input (CLK) at BNC3. This has been included so that one of two options can be used as the input frequency. The options are either a 256kHz clock with ÷1 set on IC2 or a 2048kHz clock with IC2 set to ÷8.

Selecting the required clock frequency is achieved by use of the Clock Select (CLKSEL) input at SK2 (see Fig. 7). With this input left open circuit the frequency at BNC3 should be 2048kHz (default condition). If a connection exists such that CLKSEL = 0V (i.e. pin 8 = pin 9 on SK2 - see later section Digital Interface) then a 256kHz clock is input at BNC3.

DIGITAL INTERFACE

The digital interface of the SLIC can be driven by either an On-Board option using SK2 or by external test systems using TB1. All of the five digital input pins of the SLIC and the $\overline{DET}$ output are available at both connectors.

On-Board Option

This uses the SK2 connector shown in Fig. 2 with connections as listed in Fig. 7. It has been so designed to accept insertion of an 8-way s.p.s.t. DIL switch. The switch will thus connects pins on opposite sides of the socket together, or will leave them open circuit.

For the five digital inputs this provides a means of setting 0V or leaving associated 10kΩ pull-up resistors to set a high level (+5V). The inputs and associated pull-ups are connected as in Fig. 7. A simple transistor switch with LED drive capability is connected to pin 6. When this is connected to pin 11 the LED will display $\overline{DET}$ output status (On = 0V, Off = +5V). Note that pins 7 and 10 are not used and pins 8 and 9 provide the CLKSEL function as described in the Regulator Clock Options section.

Figure 8 shows the functions of the 8-way s.p.s.t. switch for each SLIC type, when inserted at SK2.

Off Board Option

As an alternative to using SK2, an external test system may provide control of the SLIC via TB1. Connections are as listed in Fig. 6 and are made as appropriate. This connector has been designed to allow interface to the PSLAC Evaluation Package hardware (described in Application Note AN111) as discussed later in the Applications Summary section.

Note that if an 8 way s.p.s.t. switch is still inserted at SK2, then all switches should be placed in the Off (open) position. Switch 8, however, can still be used to set the CLKSEL status.

IMPEDANCE SELECTION

This subsection shows options for the programmable impedances of the evaluation board. The different values for each SLIC are to meet the requirements of impedance/gains/thresholds settings as discussed earlier in the introduction to this section.

2 Wire Termination

The PCB hole pattern is readily used for a 600Ω (i.e. resistive) line, but may be used to set any other desired value. R_{TX1} and R_{TX2} thus set 2-wire termination. The table of values shown in Fig. 9 are for each SLIC assuming 600Ω line and fitting of fuse resistors R_{FUSE1} and R_{FUSE2}, both 20Ω (thus Z_{AB} becomes = 640Ω; a 600Ω line appears as 640Ω at the LA/LB pins).

Receive Gain

After setting 2-Wire termination via R_{TX1} and R_{TX2}, the 4 to 2-Wire Gain (receive) is set to 0dB by the values of R_{GR1} and R_{GR2}, Fig. 9. These can be changed to other values, or made complex, if so required. With the suggested component values the Transmit gain is –6dB.

Off Hook Threshold

This is set by R_{TH} as described in each device data sheet. Values quoted below are for ≈11mA threshold and are given alongside the associated equation:

SL373;	$I_{DET} = 365 \div R_{TH}$:	$R_{TH} = 33k\Omega$
SL376, SL7950, SL7953;	$I_{DET} = 350 \div R_{TH}$:	$R_{TH} = 33k\Omega$
SL374;	$I_{DETON} = 410 \div R_{TH}$, $I_{DETOFF} = 465 \div R_{TH}$:	$R_{TH} = 43k\Omega$

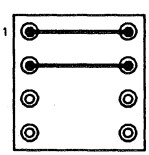
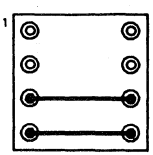
OPTION	OPTION 1	OPTION 2
HEADER		
SLIC TYPE	SL373 SL374 SL7950	SL376 SL7953
TEST RELAY ENABLED	Via SK2/TB1 *	Via SW1
RING RELAY ENABLED	Via SK2/TB1 *	Via SK2/TB1 *
* See Fig. 2 and RELAY CONNECTION OPTIONS section for details.		

Fig. 5 SK1 Socket (Relay) optional connections.

DC Feed Selection

Depending on the SLIC type, the DC Feed is set to either a 40mA constant current or an 800Ω Feed resistance, which again may be changed as required. The circuit to set this selection is via R_{DC1}, R_{DC2} and C_{DC}, as shown in Fig. 2. Fig. 9 shows component choices for the stated values of this parameter with C_{DC} setting an approximate 100Hz 3dB point in the roll-off of this network (for stability purposes - see discussion in Application Note AN82, Applications General Considerations section).

Ring Trip Setting

The Ring Trip Threshold is set at approximately 3470Ω of line by the values of R_{B1}, R_{B4} and R_F (see Applications section of data sheet for details) fitted to the board. This is the same regardless of SLIC type and may be changed if required.

With the fuse resistors fitted to the board (20Ω) the actual loop resistance for Ring Trip is 40Ω greater than the line resistance. Values of the bridge components are thus $R_{B1} = R_{B2} = 330k\Omega$, $R_{B3} = R_{B4} = 270k\Omega$ and $C_B = 160nF$. These are connected with the feed resistors, $R_F = 390\Omega$, to suit a balanced ringing supply voltage.

The PCB hole pattern allows for either a single C_B component between DA and DB (assuming no longitudinal component of AC voltage is present) or two separate capacitors to ground (see Fig. 2). The two capacitor values of 330nF thus reduce the AC ringing voltage at DA and DB by a factor of ≈6.24.

CUSTOMISED COMPONENTS

In addition to those components that may be used to program circuit parameters for the chosen SLIC, there are some components that are specific to each SLIC. These include the components R_{SUB}, D3, C_{LA} and C_{LB} as shown in Fig. 2. Thus, R_{SUB} and D3 are only required for the SL373 and SL374 SLICs. Lastly, due to the differing current gain at the virtual earth summing input of pin 18 for the SL374, the regulator noise decoupling components at LA and LB may be reduced to 2.2nF instead of 10nF (compare current gain of 1000 for all other SLICs to 200 for the SL374).

OVERVOLTAGE COMPONENTS

The hole pattern of the PCB caters for an overvoltage protection circuit as shown in Fig. 2. Two fuse resistors R_{FUSE1} and R_{FUSE2} are included in the 2-Wire loop. A 3A bridge rectifier in association with an SCR and zener diode may be fitted to the board to complete the circuit (the section on Overvoltage Protection in Application Note AN82 describes the operation of this circuit).

APPLICATIONS SUMMARY

This section summarises the use of the board for each SLIC type. In addition, recommended wiring/interconnect to the board and a discussion on interfacing to the PSLAC Evaluation Package hardware (see Application Note AN111) are also given.

BLOCK NUMBER	PIN NUMBER					
	1	2	3	4	5	6
TB1	$\overline{DET}$ OUTPUT	E0/E1 INPUT	E1/D3 INPUT	D2 INPUT	D1 INPUT	D0 INPUT
TB2	RS–	RS +	TESTA	TESTB	A	B
TB3	DGND	DV_{CC}	V_{BAT1}	$BGND_1$	V_{BAT2}	$BGND_2$
TB4	AGND	V_{EE}	AV_{CC}	-	-	-

Figure 6 : Terminal Blocks TB1..TB4 Connections Listing.

PIN NUMBER	DESCRIPTION	PIN NUMBER	DESCRIPTION
1	D0 INPUT and 10kΩ PULL-UP	16	DGND
2	D1 INPUT and 10kΩ PULL-UP	15	DGND
3	D2 INPUT and 10kΩ PULL-UP	14	DGND
4	E1/D3 INPUT and 10kΩ PULL-UP	13	DGND
5	DGND	12	E0/D1 INPUT and 10kΩ PULL-UP
6	$\overline{DET}$ LED CIRCUIT INPUT	11	$\overline{DET}$ OUTPUT
7	-	10	N/C
8	CLOCK SELECT and 10kΩ PULL-UP	9	DGND

Fig. 7 SK2 connections listing

SL373 COMPONENTS

2-Wire termination, 600Ω line with 20Ω fuse resistors $R_{TX1} + R_{TX2} = 640k\Omega$; 0dB Receive gain, $R_{GR1} + R_{GR2} = 300k\Omega$; 40mA (constant current) DC Feed, $R_{DC1} = 33k\Omega$, $R_{DC2} = 30k\Omega$, $C_{DC} = 100nF$ (100Hz 3dB point); $I_{DET} \sim 11mA$, $R_{TH} = 33k\Omega$ (Standby current feed $I_{LIM} \sim 18mA$).

SL374 COMPONENTS

2-Wire termination, 600Ω line with 20Ω fuse resistors $R_{TX1} + R_{TX2} = 128k\Omega$; 0dB Receive gain, $R_{GR1} + R_{GR2} = 300k\Omega$; 40mA (constant current) DC Feed, $R_{DC1} = R_{DC2} = 6.2k\Omega$, $C_{DC} = 470nF$ (100Hz 3dB point); $I_{DETON}/I_{DETOFF} \sim 11mA$, $R_{TH} = 43k\Omega$ (Standby current feed $I_{LIM} \sim 20mA$).

SL376 COMPONENTS

2-Wire termination, 600Ω line with 20Ω fuse resistors $R_{TX1} + R_{TX2} = 320k\Omega$; 0dB Receive gain, $R_{GR1} + R_{GR2} = 300k\Omega$; 800Ω (resistive) DC Feed, $R_{DC1} = 20k\Omega$, $R_{DC2} = 18k\Omega$, $C_{DC} = 160nF$ (100Hz 3dB point); $I_{DET} \sim 11mA$, $R_{TH} = 33k\Omega$ (Standby current feed $I_{LIM} \sim 18mA$).

SK2 PIN Nos.		8/9	7/10	6/11	5/12	4/13	3/14	2/15	1/16
SWITCH No.		8	7	6	5	4	3	2	1
STATUS		OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
SLIC Type	SL373	CLKSEL = +5V	-	D6 = Disable	E1 = +5V	D3 = +5V	D2 = +5V	D1 = +5V	D0 = +5V
	SL374	CLKSEL = +5V	-	D6 = Disable	E1 = +5V	D3 = +5V	D2 = +5V	D1 = +5V	D0 = +5V
	SL376	CLKSEL = +5V	-	D6 = Disable	E0 = +5V	E1 = +5V	D2 = +5V	D1 = +5V	D0 = +5V
	SL7950	CLKSEL = +5V	-	D6 = Disable	E0 = +5V	D3 = +5V	D2 = +5V	D1 = +5V	D0 = +5V
	SL7953	CLKSEL = +5V	-	D6 = Disable	E0 = +5V	E1 = +5V	D2 = +5V	D1 = +5V	D0 = +5V
STATUS		ON	ON	ON	ON	ON	ON	ON	ON
SLIC Type	SL373	CLKSEL = 0V	-	D6 = Enable	E1 = 0V	D3 = 0V	D2 = 0V	D1 = 0V	D0 = 0V
	SL374	CLKSEL = 0V	-	D6 = Enable	E1 = 0V	D3 = 0V	D2 = 0V	D1 = 0V	D0 = 0V
	SL376	CLKSEL = 0V	-	D6 = Enable	E0 = 0V	E1 = 0V	D2 = 0V	D1 = 0V	D0 = 0V
	SL7950	CLKSEL = 0V	-	D6 = Enable	E0 = 0V	D3 = 0V	D2 = 0V	D1 = 0V	D0 = 0V
	SL7953	CLKSEL = 0V	-	D6 = Enable	E0 = 0V	E1 = 0V	D2 = 0V	D1 = 0V	D0 = 0V

Fig. 8 Digital interface on board option, SK2 functions (switch inserted to SK2 as in Fig. 2)

Component name	SLIC Type				
	SL373	SL374	SL376	SL7950	SL7953
R_{TX1}	510k	110k	300k	510k	510k
R_{TX2}	130k	18k	20k	130k	130k
R_{TX}(Total)	640k	128k	320k	640k	640k
R_{GR1}	150k	30k	150k	150k	150k
R_{GR2}	150k	30k	150k	150k	150k
R_{GR}(Total)	300k	60k	300k	300k	300k
R_{DC1}	33k	6.2k	20k	20k	33k
R_{DC2}	30k	6.2k	18k	18k	30k
C_{DC}	100n	470n	160n	160n	100n

Fig. 9 Component choices for 600Ω line, 0dB Receive Gain and 40mA/800Ω DC Feed

SL7950 COMPONENTS

2-Wire termination, 600Ω line with 20Ω fuse resistors $R_{TX1} + R_{TX2} = 640k\Omega$; 0dB Receive gain, $R_{GR1} + R_{GR2} = 300k\Omega$; 800Ω (resistive) DC Feed, $R_{DC1} = 20k\Omega$, $R_{DC2} = 18k\Omega$, $C_{DC} = 160nF$ (100Hz 3dB point); $I_{DET} \approx 11mA$, $R_{TH} = 33k\Omega$ (Standby current feed $I_{LIM} \approx 18mA$).

SL7953 COMPONENTS

2-Wire termination, 600Ω line with 20Ω fuse resistors $R_{TX1} + R_{TX2} = 640k\Omega$; 0dB Receive gain, $R_{GR1} + R_{GR2} = 300k\Omega$; 40mA (constant current) DC Feed, $R_{DC1} = 33k\Omega$, $R_{DC2} = 30k\Omega$, $C_{DC} = 100nF$ (100Hz 3dB point); $I_{DET} \approx 11mA$, $R_{TH} = 33k\Omega$ (Standby current feed $I_{LIM} \approx 18mA$).

RECOMMENDED WIRING SCHEME

In order to achieve the best performance from the board, the general wiring for power supplies and ground connections should be as in Fig. 10. This uses a single ground point defined at TB4 pin 1. Note that the PCB defines an Analog Ground point at pin 18 of IC1 (SLIC socket) and a Battery Ground ($BGND_1$) point at pin 1 of IC1, routed to TB3 pin 4. Separate grounds for digital (DGND) and overvoltage ($BGND_2$) circuits route to TB3 pins 1 and 6 respectively. The single ground point thus minimises the noise levels, notably the regulator clock fundamental (256kHz) and harmonics.

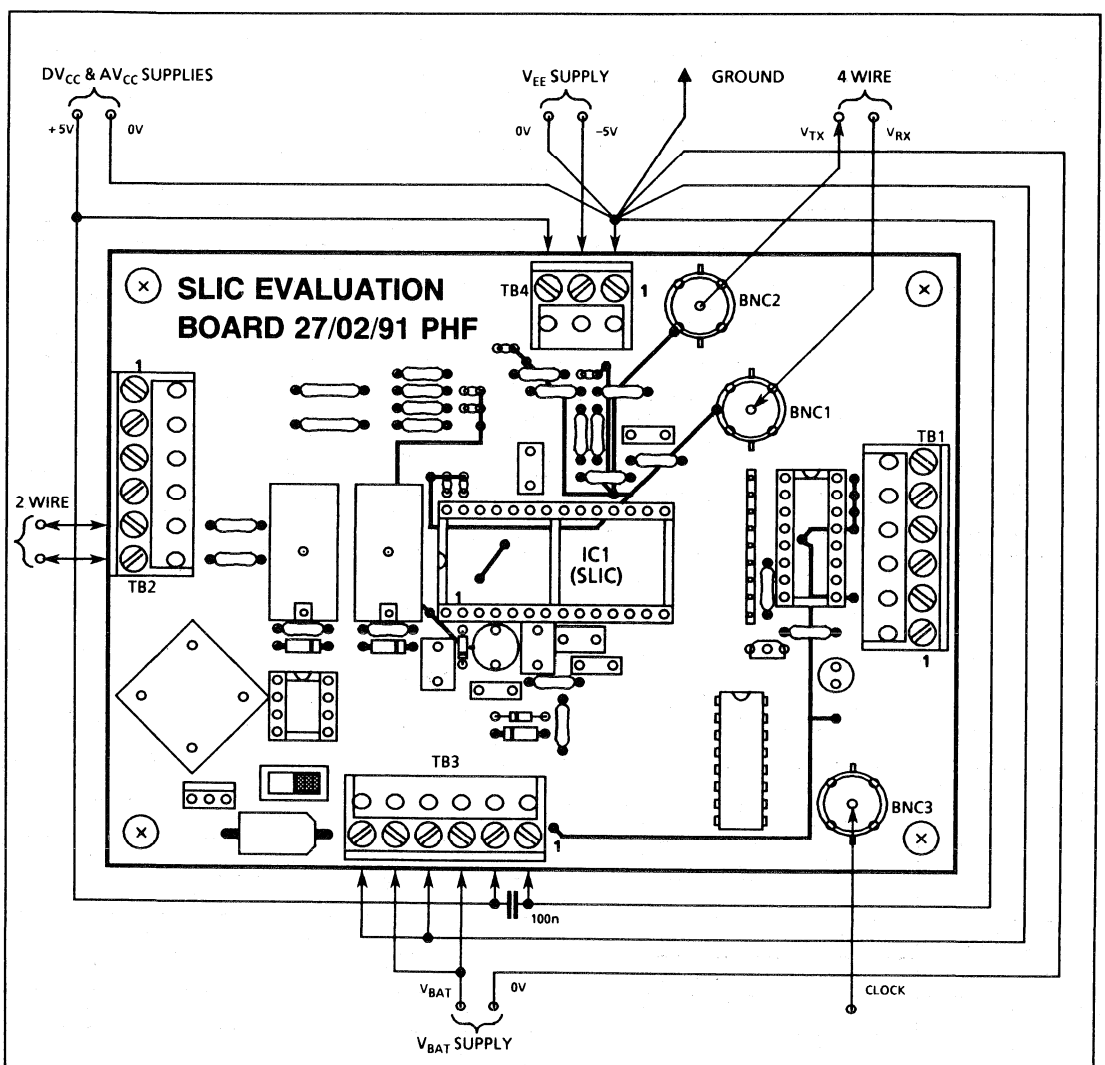


Figure 10 : Recommended Wiring Scheme.

INTERFACE TO PSLAC EVALUATION PACKAGE

Fig. 11 shows how the SLIC Evaluation Board is connected to the PSLAC Evaluation Package hardware (PCB) to provide evaluation of a SLIC/PSLAC application (i.e. Line Card environment). The PSLAC Evaluation Package is described separately in Application Note AN111.

The interface consists of the 4-wire ports connecting to the appropriate analog input and output of PSLAC1 on the PSLAC Evaluation Package hardware. Additionally, this board provides a 2048kHz clock which can be used to drive the regulator (from TB7 pin 2) such that SK2 on the SLIC board can be left unconnected. TB2 on the PSLAC board wires to TB1 on the SLIC board, as shown. All SLIC modes are now controlled via this interface which is under software control of the PSLAC Evaluation Package.

Part of the PSLAC Evaluation Package software display (via an IBM PC/Compatible) are two SET UP SCREENS showing all programmable parameters status for both PSLACs of the PCB. These include the SI and CP1...CP5 status of each PSLAC, with of course those of PSLAC1 controlling the SLIC. Thus all of CP1...CP5 for PSLAC1 should be set to output (letter O on the display) mode in order to drive the SLIC inputs. With the connectors wired as in Fig. 11, the order of inputs across the screen will be as follows:-

D0 Level, D1 Level, D2 Level, E1/D3 Level, E0/E1 Level

The levels as displayed (0 = 0V logic low, 1 = +5V logic high) will set SLIC status according to that shown in Table 2 of each SLIC Data Sheet and are changed under software control. Additionally, the $\overline{\text{DET}}$ Status will be shown as that of the SI Status on the SET UP SCREEN of PSLAC1.

As a guide, listed below is the exact correspondence of each SLIC digital input to that of the CP Latch number for each SLIC in turn :

SL373	CP1, CP2, CP3, CP4, CP5 = D0, D1, D2, D3, E1
SL374	CP1, CP2, CP3, CP4, CP5 = D0, D1, D2, D3, E1
SL376	CP1, CP2, CP3, CP4, CP5 = D0, D1, D2, E1, E0
SL7950	CP1, CP2, CP3, CP4, CP5 = D0, D1, D2, D3, E0
SL7953	CP1, CP2, CP3, CP4, CP5 = D0, D1, D2, E1, E0

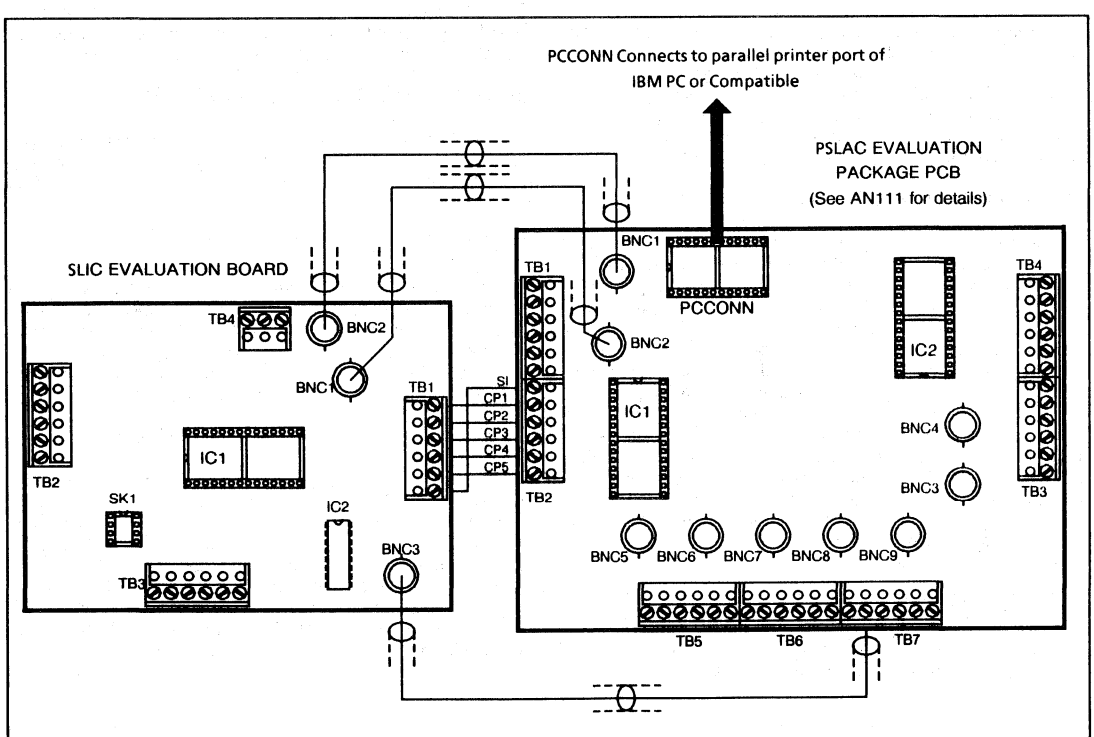


Fig. 11 Interface to PSLAC Evaluation Package PCB

Features of the MV3010 Subscriber Line Audio Circuit

AN102

Subscriber Line Audio Circuits (SLAC and COMBO devices) have been traditionally realised using switched capacitor techniques. Such devices have a mainly analog content with limited programmability. Digital Signal Processing (DSP) techniques have been used to realise the MV3010 PSLAC (Plessey Subscriber Line Audio Circuit). This has allowed the analog content of the device to be minimised in favour of powerful DSP. The device therefore offers many features not found on even the most advanced switched capacitor design. This Application Note provides a ready summary of these features.

DSP REPEATABILITY

DSP techniques ensure excellent transmission parameter repeatability. This applies to such effects as part-to-part variations, long term aging, power supply dependence and temperature variations.

ADAPTIVE ECHO CANCELLATION FILTER

The first important additional feature available from the PSLAC DSP routines is the inclusion of an echo cancellation filter. This can be enabled so as to reduce the level of any echo from line interface circuitry (due to a mismatch of terminating and line impedances). The filter can be used to ensure optimum Echo Return Loss (ERL) is achieved over a wide range of line lengths and terminating impedances. Most important of all, is the inclusion of a powerful self-adaptive echo cancellation algorithm, which can maintain required ERL over the life of the line, even if line length and/or telephone instruments should change.

A signal Correlator and programmable Double Talk detector form part of the adaptive algorithm, to ensure that resultant (adapted) ERL can never allow system instability. It is then completely robust, whatever signal types (i.e. frequency spectrum) are presented to it. The algorithm is discussed further in Application Note AN103 and a performance summary is given in Application Note AN104.

FLEXIBLE FIXED MODE CANCELLATION

The echo cancellation filter can also be used in a programmable fixed mode of operation, to give a predetermined response. It can then be optionally allowed to adapt continuously or for a user defined time period and then frozen (disable adaption).

Programming of a fixed response can be done accurately to meet most of the likely required responses. Each of the nine Finite Impulse Response (FIR) taps of the filter are fully programmable in the range –2 to +2 using a 12 bit (2s' complement) data format. Each tap is spaced at 62.5µs delay giving at least 562.5µs of echo path delay that can be accurately cancelled. There is also the addition of a tenth tap which contains a recursive loop (Infinite Impulse Response type). This can add an exponential tail to the filter impulse response, so allowing even longer echo delays to be attenuated.

FREQUENCY EQUALISATION FILTERS

The DSP provides the option of user programmable 4 tap FIR type filters in both transmit and receive paths of the PSLAC. These can be used to correct for amplitude and phase errors that may be introduced by external circuitry, such as 2-wire to 4-wire and 4-wire to 2-wire conversion. Alternatively, the PSLACs fixed CCITT/AT&T filter responses may be customised by these filters.

WIDE GAIN RANGE

(Transmission parameters fully specified)

The transmit and receive path gains are both programmable over a wide range at small linear step sizes, using a 12 bit (2s' complement) data format (typically <0.1dB adjustment). These ranges are:-

$$-\infty \leq \text{Transmit Gain} \leq +15.56\text{dB}$$
$$-\infty \leq \text{Receive Gain} \leq +6.02\text{dB}$$

The full Transmission path specifications meet or exceed CCITT requirements over most of this range, i.e. with 0 to +13dB Transmit Gain and/or 0 to +12dB Receive loss.

SINGLE POWER SUPPLY VOLTAGE

The MV3010 requires only a single +5V power supply (±5%), simplifying supply decoupling and board tracking. System reliability is improved over circuits needing dual supplies.

16 BIT LINEAR PCM ACCESS

This is available as a user selectable option alongside the more usual A-Law and µ-Law PCM codes. It can be used to simplify the implementation of such features as conference bridges or further external signal processing (e.g. ADPCM compression). This mode provides full 16-bit accuracy over the complete dynamic range.

CLOCK OFFSET PROGRAMMABILITY

In addition to user defined time slot assignment (up to 64 on each of dual Transmit/Receive PCM ports) it is possible to further offset the chosen time slot by additional PCM clock cycles. These can be from 0 to 7 cycles independently for each transmission path.

The device works in plesiochronous mode (CCITT G.701 2.6) where PCM clocks and synchronisation signals should be frequency locked to the device master clock, the exact phase relationships being unimportant.

PCM CLOCKING CAPABILITIES

The backplane interface of the PSLAC has been made completely flexible, supporting a wide range of clock rates independently for the transmit and receive directions. Thus, either transmission path can be set with a clock rate between 64kHz and 4096kHz. In addition, the inclusion of dual transmit and receive ports (via one of two selectable pins for each path) provides additional security of transmission, or can be used as a simple means of space switching in the exchange.

TRANSMISSION DIAGNOSTIC FUNCTIONS

The normal range of transmission diagnostic functions has been complemented by further user selectable functions. These include receive path disable, receive path 6 dB attenuate and a code to disable the fixed high pass filters of the PSLAC.

STAND ALONE OPERATION

In most applications, the design of a line card utilising all the benefits of the MV3010 PSLAC, will require an active digital control interface to the device. This is used to fully control all the features, including the self adaptive cancellation filter, of the PSLAC. However, a further possible mode of operation is possible with the MV3010, namely Stand Alone operation.

Stand Alone operation works by setting the functions of the device to its default conditions (as given in the data sheet). For this mode to be active, the control interface is hard-wired to predetermined input conditions. These input conditions may be changed to allow the device to be set to active or standby status (providing power saving capability) and to enable (with adaption) or disable the Cancellation filter. Thus for some applications, a greatly simplified line card design is possible.

MV3010 Achieves Stable Robust Adaption

AN103

This Application Note discusses the issues affecting the performance of the MV3010 Plessey Subscriber Line Audio Circuit (PSLAC) Cancellation Filter (C Filter), giving particular regard to conditions under which the self adaption algorithm achieves stable and robust operation. Fig. 1 illustrates the basic system architecture for a line card application and shows the basic terminology used throughout this document. Specifically, the 'Near End' is considered to be the line card with the adaptive PSLAC. The 'Far End' may be any other form of line card architecture, including an MV3010 based design.

Normal convention for the term Echo Return Loss is considered to be the level of receive PCM signal that appears in the transmit path. However, this parameter will change with any alterations to both Transmit and Receive gains programmed within the MV3010 (assuming an echo path exists). For this reason the term Cancellation is preferred, this being the attenuation of the PCM receive signal at DRA/DRB by the MV3010's C Filter, in combination with the line interface 'starting point', at the PCM transmit output DXA/DXB. The term 'starting point' is the basic echo level between the V_{OUT} and V_{IN} pins of the MV3010.

INTRODUCTION

The MV3010 contains a user-programmable echo cancellation filter (C Filter). This attenuates any part of the receive signal that may be present in the transmit path due to an imperfect hybrid (i.e. 2-wire/4-wire conversion) function. Retransmission of this signal back to the far end is therefore minimised. When optimally programmed, this filter can give excellent echo cancellation. Most lines in a real network will of course never be optimally programmed as the performance of each individual line's hybrid function will not be known to the system. In addition, the coefficients needed for optimum cancellation for each line will change with time, for example due to component aging or a change to the telephone instrument being used.

These limitations can be overcome by the use of self adaptive echo cancellation. In this set up, filter coefficients self adapt to changing echo conditions to maintain a minimum level of receive signal present in the transmit path. The MV3010 implements a Clipped LMS type adaptive filter based on the classic Widrow-Hoff algorithm. Particular care has been taken in its design to ensure that this algorithm is optimised and sufficiently well controlled to prevent any undesirable adaptions that may lead to network instability.

The algorithm has been extensively tested using various single and multiple sinusoids, prerecorded and live speech with a wide range of near and far end echo path combinations. In all cases (except where preprogramming was particularly accurate) adaptions have resulted in improved cancellation. Unwanted adaptions that may have lead to network instability were always prevented. The features of the MV3010 C Filter are now described in greater detail.

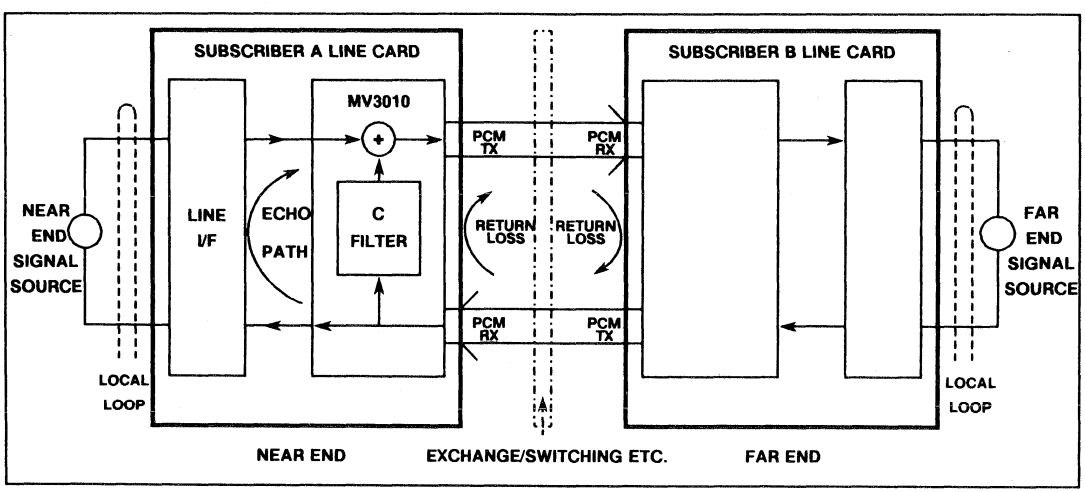


Fig.1 Basic system architecture, End - End loop.

ADAPTION - THE PROBLEMS

The normal requirements for good adaption include a dominantly wideband far end signal. Note that we assume the adaptive filter to be operating at the near end; the far end signal is therefore received in PCM form from the network. The echo response around the near end line circuit is then readily cancelled by the adaptive filter. Fig. 2 illustrates a typical response to a wide band far end signal.

If the incoming far end signal is narrow band periodic (e.g. single tone or whistle) then a simple LMS adaptive filter would optimise cancellation for the frequencies present with no regard for the resultant response at other frequencies. Whilst this may give extremely good cancellation at the signal frequencies, almost arbitrary cancellation will be obtained at other frequencies within the audio band. A possible degradation in overall ERL may then result. An example of this type of behaviour is given in Fig. 3. If far end overall ERL is also poor (as is likely if the far end has non-adaptive cancellation) then loop gain may approach unity at some frequencies. This may then allow oscillation to be triggered by noise components in the end-end loop. The filter may then re-adapt to attenuate this oscillation, allowing oscillation at some other frequency to build up. This behaviour is clearly unacceptable.

Periodic signals generated at the near end can also cause problems because the adaptive filter cannot determine from which end it originates. Adaption to minimise near end echo is only possible with a signal originating at the far end. However, if there is a large amount of far end echo, an adaptive filter can try to cancel a near end originating periodic signal using the echo from around the far end loop. Doing this may result in large adaptive coefficients in the C Filter (the near end signal is larger than the far end echo level). If there is also gain programmed in the transmit and/or receive directions (for a long line condition) then under these circumstances, oscillations can build up in the end-end loop.

ADAPTION - THE SOLUTIONS

The MV3010 solves these problems by adding a signal correlator circuit to detect periodic signals in the receive path, inhibiting adaption until a reasonably broad band signal is available.

A second feature, added to the basic algorithm, is the addition of a Double Talk detector. This has been added to give extra protection against undesirable adaptions. If we again consider the case of near end originating signals (and large far end echo), there may be some correlation which is not enough to cause the correlator to inhibit adaption (while the ideal signal to adapt to is a wide band noise source, the MV3010 must adapt to speech signals which contain some degree of correlation). It is very unlikely that signals which are not detected by the correlator will be a problem, but the addition of the double talk detector allows extra robustness to be built in.

The double talk detector compares the receive signal (which is being output to the analog line interface) with a reprocessed version of the incoming signal (i.e. near end plus echo at the analog input to the PSLAC). This reprocessed signal is obtained by subtracting the C Filter output and any DC component from it, then multiplying this by the programmable (via the Control Interface) Double Talk Coefficient (DTC). Fig. 4 shows a conceptual model of the detector operation. If the receive signal is smaller than the reprocessed transmit signal, the adaption process is paused. Note that a zero or negative value for the DTC will disable the detector, whilst values up to +8.0 give a range of sensitivity to cater for different line interface circuits.

As double talk is equivalent to poor ERL, (the detector cannot distinguish the signal origin) the sensitivity of the detector must be less than the worst case echo level else adaption is effectively inhibited. Thus an optimum value for the DTC can be obtained after the C Filter has been preprogrammed. Thus by comparing the signal after the C

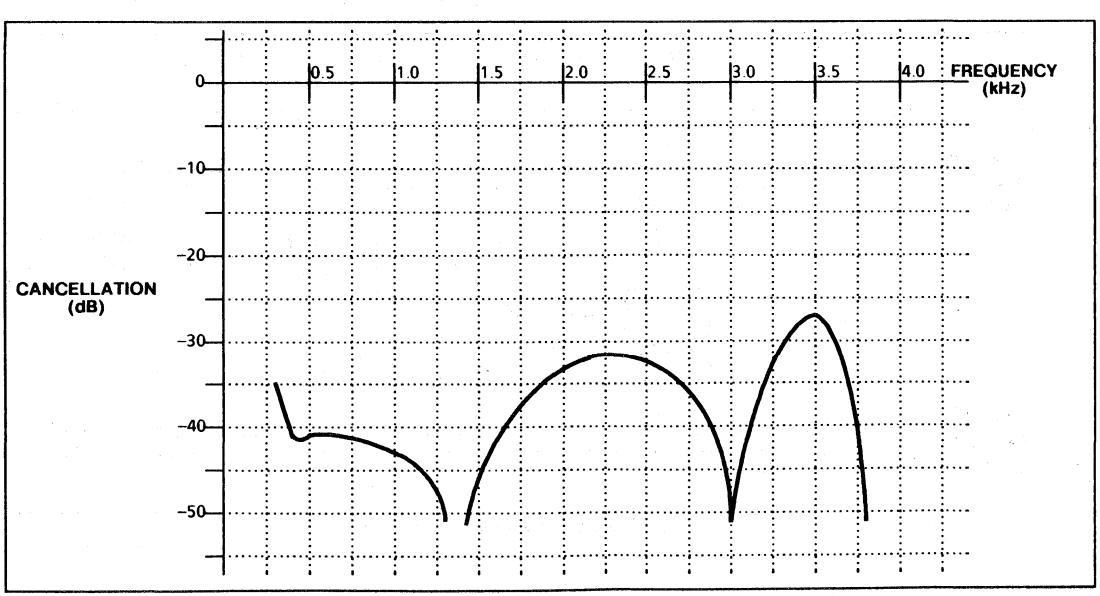


Fig. 2 Typical Cancellation after preprogramming and Adaption to wide band far end signal

Filter output has been subtracted from the transmit path, the double talk sensitivity can be improved (as opposed to comparing the incoming signal before the C Filter output has been removed) by the minimum Echo Return Loss Enhancement that the C Filter preprogramming gives with the expected loads.

Finally, an Oscillation Quench circuit has been built into the MV3010 to cater for the extremely unlikely event that a set of C Filter adapted coefficients result in oscillations in the end-end loop. If such an oscillation is detected, the last set of preprogrammed coefficients are restored to the C Filter foreground filter so as to quench the oscillation. Of course, the basic system must be stable with any programmed gains (transmit and/or receive), preprogrammed C Filter coefficients and far end echo, but this is an obvious requirement of even a stable nonadaptive system. It is not expected that the oscillation quench feature will ever be invoked in normal usage.

In summary, the MV3010 allows the advantages of adaptive echo cancellation (over a range of unknown conditions) to be obtained without using any special test signals other than the normal speech traffic, yet has built in immunity to conditions/signals that would otherwise cause undesirable adaptions. Full control of the adaption process is thus available by enabling/disabling (freezing the current set of coefficients) adaption, preprogramming the C Filter, controlling the correlator and programming the Double Talk Coefficient.

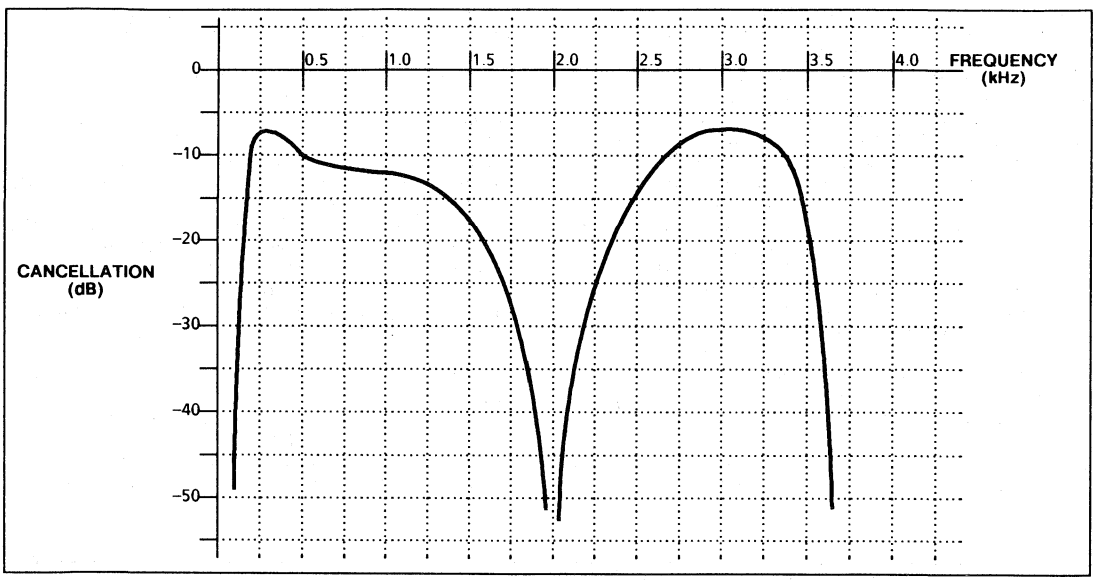


Fig. 3 Typical Cancellation after Adaption to a single tone far end signal

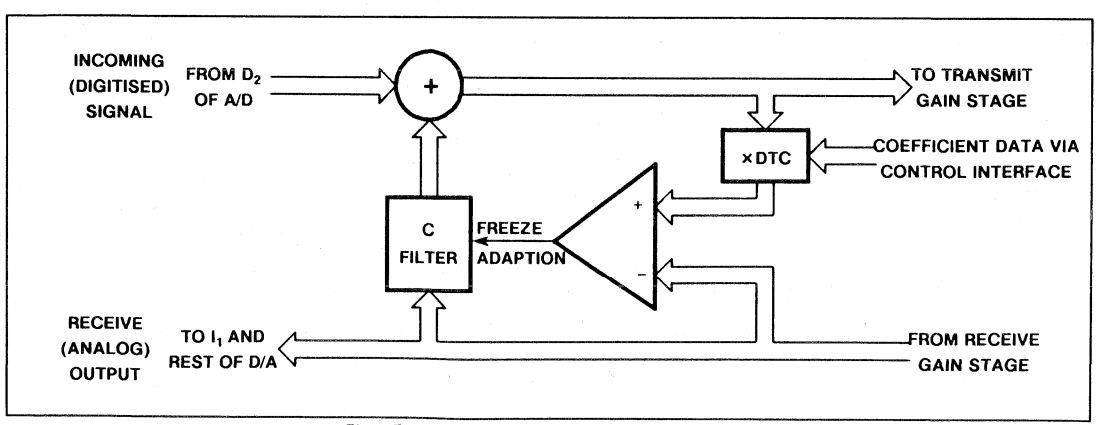


Fig.4 Double Talk Detector, conceptual model.

Benefits of the MV3010 Adaptive Echo Cancellation Filter

AN104

This Application Note summarises the typical echo cancellation performance of the MV3010 Subscriber Line Audio Circuit when used in Line Card type applications.

TEST CIRCUITS

Two different types of Interface Circuit to the 2-wire line were used in obtaining the results given. In each case, an MV3010 Demo Board and Controller PCB (see Application Note AN42) was used in association with the Line Interface. This is connected to the circuits shown in Figs. 1 and 2, to form two all-analog test circuits.

In Fig. 1, an Op Amp drives the 2-wire line via 600Ω and an 600Ω-600Ω isolating transformer (type HED 25819). A single pole complex impedance is used as the line load (Z_N), with or without a simulated 7-mile line connected in series. For Fig. 2, a real telephone (GPT designer phone type 5010) is used as the 2-wire line load (Z_N) and the line is driven by the GPS SL373 Subscriber Line Interface Circuit (SLIC). The SLIC circuit is terminated with a complex impedance, and again, a simulated 7-mile line may be connected in series with the phone. For both circuits, no cancellation circuit is provided externally to the MV3010 and the C Filter performance is evaluated by programming and enabling/disabling its various features.

TEST RESULTS

Two tables of results are given below. Table 1 summarises the results for the circuit of Fig. 1, whilst the results in Table 2 are for the circuit of Fig. 2.

The performance of the C Filter is given for six different conditions in each case. These are obtained by the following test procedure:

Step 1. C Filter disabled, 0 mile line.
Step 2. C Filter enabled after preprogramming for 0 mile line (using the technique described in AN84).
Step 3. C Filter adapted to white noise following step 2.
Step 4. C Filter disabled, 7 miles of line.
Step 5. C Filter enabled and preprogrammed with the coefficients of step 3 (7 mile cable still connected).
Step 6. C Filter readapted from step 5 to optimise the adaptive taps of the filter for the 7 mile line.

Measurements were taken with a nominal end-end gain, for both transmit and receive directions, of 0dB (i.e. both MV3010s on the demo board have transmit gain of 0dB and receive gain of 6dB to remove the effect of the difference in PSLAC analog input and output dynamic ranges). The figures are quoted for the demo board analog output level relative to the analog input level. For each step in the tests, the worst case cancellation only that occurred at any frequency within a 200-3800Hz bandwidth, is quoted. Note that for each circuit, a small amount of cancellation results from the interface circuit, of a nominal 6dB, with a matched line load (i.e. $Z_N = Z_I$). Also, the line model assumes a specification of 277Ω/mile and 82nF/mile of cable.

CONCLUSION

The results of Tables 1 and 2, steps 3 and 6, show that the MV3010 C Filter can provide at least 20dB of Cancellation without any external circuitry. This is maintained over a wide range of line lengths (i.e. 0 to 7 miles), by use of its self-adaptive algorithm, starting from a single set of preprogrammed coefficients. Note that the structure of the filter, with multiple taps in the time domain, is well suited to matching real lines which may suffer from several reflections.

Test step	Line length	Worst case cancellation	Frequency
1	0 Miles	4.7dB	500Hz
2	0 Miles	12.1dB	300Hz
3	0 Miles	24.4dB	1010Hz
4	7 Miles	3.3dB	400Hz
5	7 Miles	17.7dB	300Hz
6	7 Miles	22.2dB	300Hz
Line Load = Z_N = 370Ω + (620Ω ‖ 310nF) Input Impedance = Z_I = 600Ω			

Table 1 Transformer interface circuit results (see Fig. 1)

Test step	Line length	Worst case cancellation	Frequency
1	0 Miles	5.5dB	2800Hz
2	0 Miles	25.5dB	1500Hz
3	0 Miles	31.1dB	3300Hz
4	7 Miles	4.7dB	300Hz
5	7 Miles	15.8dB	500Hz
6	7 Miles	23.0dB	200Hz
Line Load = Z_N = GPT Designer Phone 5010 Input Impedance = Z_I = 300Ω + (1kΩ ‖ 220nF)			

Table 2 SLIC interface circuit results (see Fig. 2).

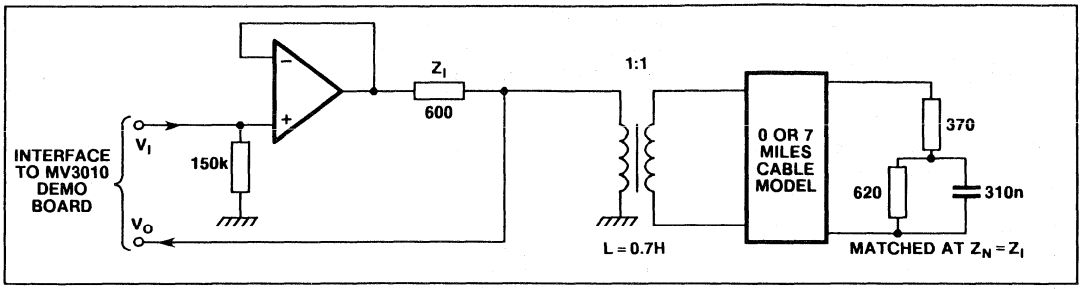


Fig.1 Cancellation test circuit, simple op amp line interface

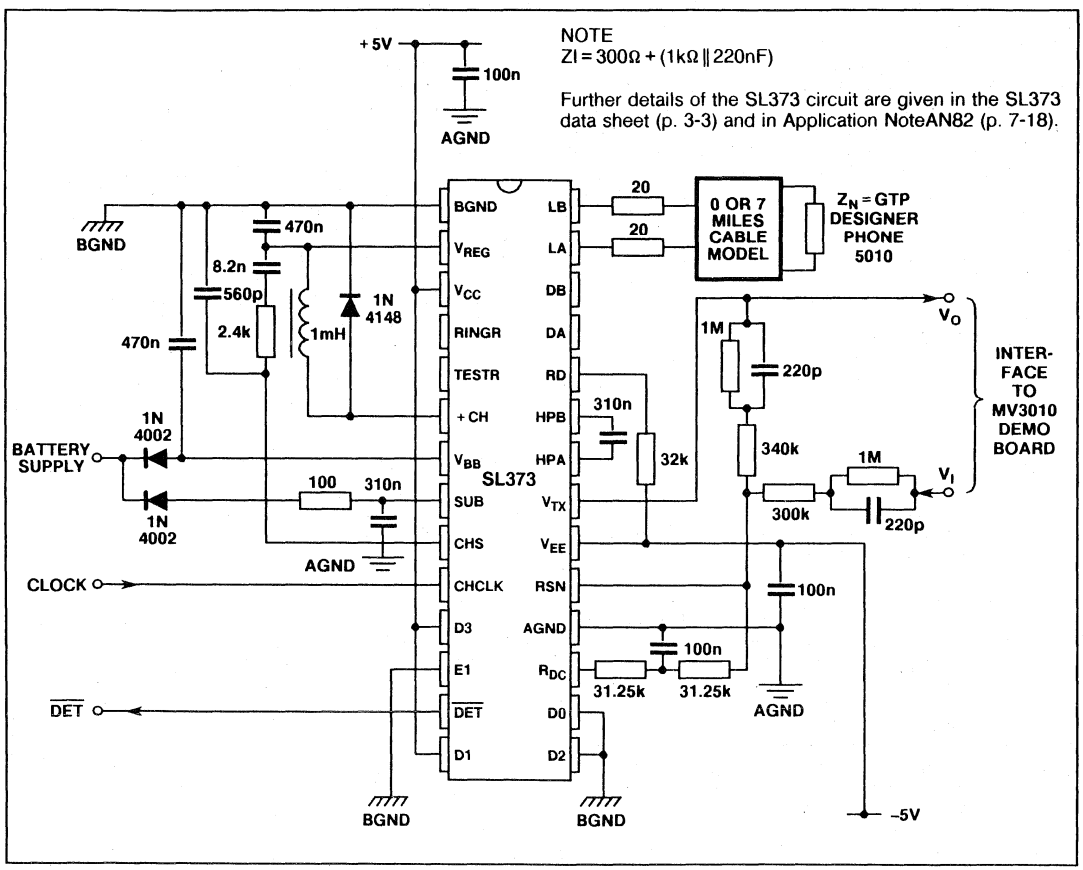


Fig.2 Cancellation test circuit, SL373 SLIC

Preprogramming the MV3010 C Filter using the Measurement Method

AN84

A major feature of the MV3010 PSLAC is the C Filter and its adaptive mode, which is used to provide echo cancellation in various applications, such as line card architectures/line interfaces in a telephone system. Data on the MV3010 functions, including the C Filter operation, is given in the MV3010 data sheet (p. 3-135).

In certain circumstances, reasonable echo cancellation can be obtained using only the adaptive taps of the MV3010 C Filter (A_1, A_3, A_5, A_7, A_9), as would be obtained if adaption starts from an all coefficients at zero condition. However, improved echo cancellation is usually obtained by preprogramming some, or all, of the taps of the C Filter. This provides a good starting point/initial cancellation with a known set of line and terminating impedances (preprogramming). The adaptive mode of the C Filter is then used to maintain/improve cancellation as these known conditions vary.

Calculating such coefficients for preprogramming the MV3010 C Filter for a known initial condition/echo level of the PSLAC's line interface can be done in various ways. Since it is recognised that numerous different line interfaces and line/terminating impedances may be used in association with the PSLAC, differing coefficients will be needed for each case. To make the job of determining these coefficients for preprogramming in a given application easier, this document describes a simple preprogramming technique. This technique, which uses the PSLAC adaptive mode of the C Filter, avoids the need for software models and/or arduous calculations. It is therefore applicable to any type of line interface.

This preprogramming technique has been fully automated as part of a complete PSLAC Evaluation Package. Application Note AN111 (p. 7-82) describes both the hardware (PCB evaluation board) and software (for IBM/compatibles) that are included in this package. It is recommended that this evaluation package be used for preprogramming the C Filter, although the technique described in this document may still be done manually if so required.

CONTENTS

DESCRIPTION

The C Filter of the MV3010 is a ten tap FIR structure, operating at a sample rate of 16kHz. The last tap has a recursive loop to provide better matching of the echo path should there be a long tail in the input response of the echo. The transfer function of the C Filter can be written as:-

$$H(z) = A_0 + A_1Z^{-1} + A_2Z^{-2} + .. + A_8Z^{-8} + \frac{A_9Z^{-9}}{[16 - (15Z^{-1})]}$$

where $Z = e^{j\omega t}$ with t = 1/16kHz and only the odd taps (A_1, A_3, A_5, A_7, A_9) are adaptive. This filter structure is described fully in the MV3010 Data Sheet.

Preprogramming the MV3010 uses the self-adaptive nature of the C Filter to characterise the echo path over the audio bandwidth. This is possible since even without preprogramming the C Filter, cancellation of a single tone to better than 50dB is possible using only the adaptive (odd) taps. (Note that the C filter correlation should be disabled to allow adaption to a single tone. The correlator is normally enable for use in line card environments to prevent adaption under certain systems/line conditions that otherwise may cause instabilities/ oscillations to occur if adaption was to take place - see AN103, p. 7-60, for details). C Filter coefficients obtained in such a set up are then a measure of the real and imaginary parts of the echo path transfer function, at the frequency of the single tone used. Thus, if this type of measurement is repeated at various frequencies across the audio bandwidth, then the resulting sets of coefficients obtained are a measure of the echo path transfer function across the band.

After this information has been obtained, a single set of coefficients is generated such that when these are programmed back into the C Filter (nonadaptive mode), then good echo cancellation will result for the characterised echo path.

This calculation is achieved using a simple computer program that utilises the individual sets of coefficients as input data. Firstly the program calculates the nature of the echo path as measured. Secondly, assuming all zero coefficients as a starting point, the program uses an iterative technique to search for a set of coefficients that best match this calculated response. This is achieved by varying each tap value in turn, by the largest possible step size, and calculating the error between the required response and that obtained from this new set of coefficients. The greatest improvement in this error by a change (±) in a single coefficient by the step size is stored for comparison. The program now searches for the next best change of a single coefficient to produce the least error. This process continues until it is no longer possible to reduce the error (between the required response and these search coefficients) by changing a single tap by the largest step size. The step size is reduced by a factor of two, and the program repeats the search procedure. This process continues until the smallest possible step size of a coefficient is reached. The program then prints out the final set of coefficients giving the best match of the C Filter response to the measured echo response.

TAKING THE MEASUREMENTS

The measurement technique involved is very straightforward, and is now described in detail in this section. However, it is recommended that the MV3010 Evaluation Package is used to automate this procedure. If this is not possible, then measurements may be made manually at a customer site or by a GPS Applications Engineer.

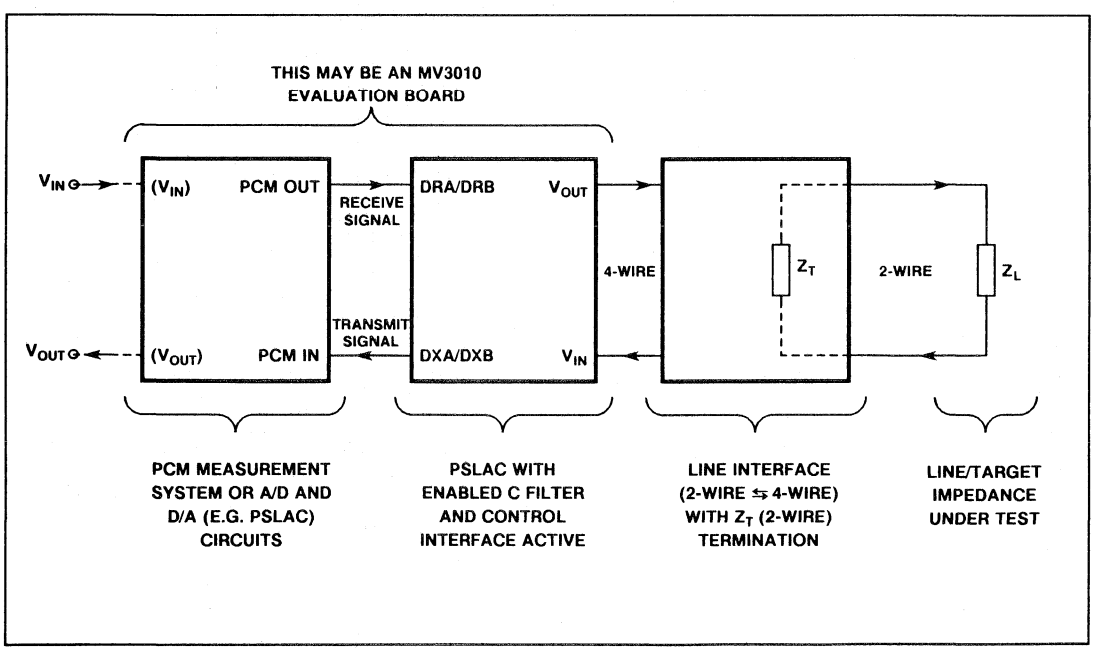


Fig. 1 Preprogramming test set up

The initial measurements at spot frequencies are made using the test set up shown in Fig. 1. The line interface circuit 4-wire port, with the desired termination impedance (Z_T), is connected to the 4-wire port of the MV3010 (i.e.V_{IN}/V_{OUT}) with the target line impedance connected to the 2-wire port. MV3010 transmit and receive gains are set to 0dB with all filters, except the C Filter (nonadaptive), disabled. Connections to the PCM ports of the MV3010 are now made in order to apply a test tone of about 2Vp-p equivalent to the DRA input. This signal can be generated by a PCM Test System, another MV3010 'back to back' (as for the MV3010 Evaluation Board - see Application Note AN111) or other suitable A-D/D-A system. The frequencies used for these spot frequency measurements are shown in the blank form 'C Filter Preprogramming Measurements' on page 7-74.

Under the conditions just described, the signal level at the MV3010 PCM output (DXA), depends on the echo level of the line interface. If C Filter adaption is enabled (both the double talk detector and correlator features of the C Filter should be disabled), this signal should now be reduced to a level 50dB, or better, below the original level. Note that the better the cancellation obtained, then the better the coefficients represent the characteristics of the echo path at the test frequency, so the greater is the accuracy of the final preprogramming (broadband) result. Single tones can cause adaption to converge on many different sets of coefficients with differing resultant cancellation. If sufficient cancellation does not result, it may therefore be necessary to readapt by momentarily switching the test frequency to another value, or changing to a broadband signal. The input signal should be returned to the original setting to ensure the C Filter now cancels to better than 50dB. Once this situation has occurred, adaption should be disabled, and the coefficient values read out via the MV3010s DI/O pin (as described in the data sheet). The resulting Hex data should be recorded on the blank form mentioned earlier. The whole procedure is then repeated at each frequency, listed on this form in turn.

EXAMPLES

This section illustrates the preprogramming technique by presenting some examples of line interfaces/echo paths that are connected to the MV3010. In all cases, note that the term cancellation refers to the attenuation of the receive PCM input signal (DRA/DRB) by the PSLAC C Filter/line interface, at the PCM transmit output (DXA/DXB). The actual Echo Return Loss (ERL) from PCM input to PCM output will exhibit an extra 6dB loss due to the difference between V_{OUT} and V_{IN} dynamic ranges (assuming both transmit and receive gains are set to unity i.e. 0dB). Where adaption has been done after preprogramming, a broadband signal (a suitable signal would be white noise or a sinusoid swept from 0-4kHz at a 50ms rate) has been used to ensure broadband cancellation. All measurements of cancellation are done with the C Filter in its nonadaptive mode or disabled to show starting conditions.

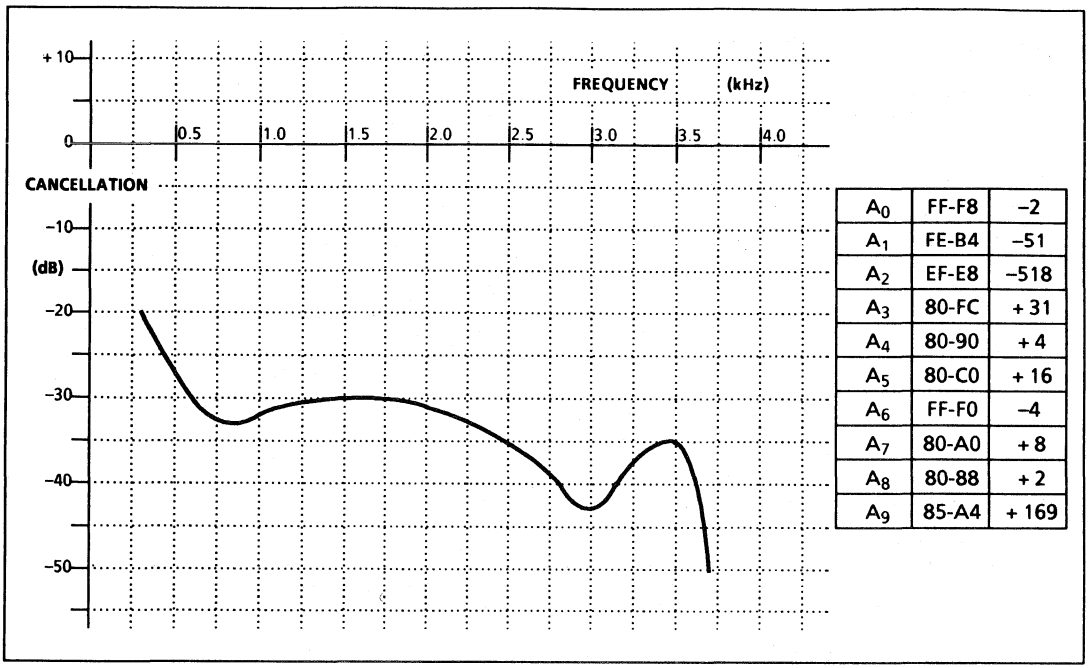
EXAMPLE 1

This directly links the MV3010 V_{OUT} pin to the V_{IN} pin via a 10µF DC blocking capacitor. The results confirm that the MV3010 internal delays from the point where the receive signal is input to the C Filter, through the analog interface and back to the C Filter output summing node, is nominally 125µs ($\approx A_2$ of the C Filter) with a gain around the loop of nominally –8/15 ($A_2 = -0.533$ or coefficient value –546/Hex EE-F8).

Fig. 2 lists the coefficients obtained at the spot frequencies, whilst Fig. 3 gives the cancellation obtained after preprogramming the MV3010. Also listed are the coefficients obtained as output by the computer program. Note the close correlation between the A_2 theoretical and preprogramming values. Fig. 4 shows the enhancement obtained after adaption to a broadband signal, and again lists the coefficients that result.

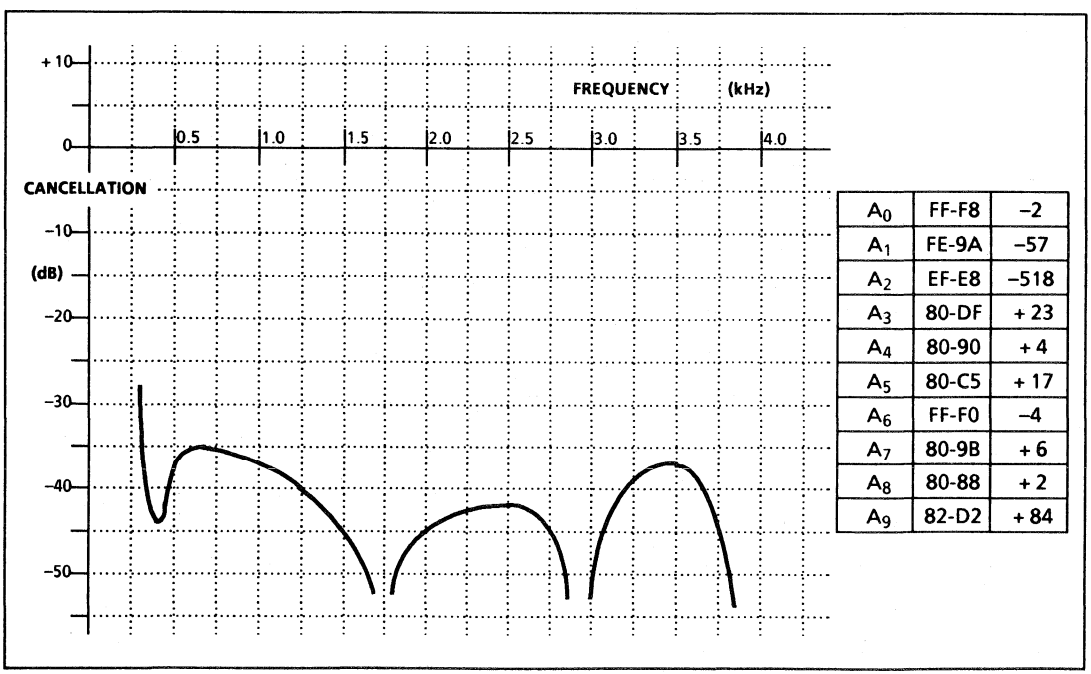
Frequency (Hz)	A_9	A_7	A_5	A_3	A_1
200	84-C9	FD-A4	81-9F	F9-D1	F6-9C
300	82-F3	FD-EC	83-FE	F7-EA	F5-B7
500	88-CD	FE-A3	82-AA	F8-87	F7-DC
800	88-B2	FF-C0	82-B0	F7-EA	F6-A6
1200	83-97	FC-8B	82-DC	F6-FA	F2-A6
1700	FF-93	FF-9B	80-D5	F5-EE	F3-EE
2100	80-EE	80-8B	81-FB	F5-A1	F3-EF
2400	95-9E	FE-A4	84-B2	F3-AD	F6-8D
2700	8B-E2	FA-DD	85-F2	F6-D3	F9-A8
3000	82-B2	FC-9C	84-B7	F5-92	F2-A6
3300	8C-D5	F9-F4	86-87	F8-F6	F0-C7

Fig. 2 Spot frequency coefficients for Example 1



A_0	FF-F8	–2
A_1	FE-B4	–51
A_2	EF-E8	–518
A_3	80-FC	+ 31
A_4	80-90	+ 4
A_5	80-C0	+ 16
A_6	FF-F0	–4
A_7	80-A0	+ 8
A_8	80-88	+ 2
A_9	85-A4	+ 169

Fig. 3 Cancellation after preprogramming; Example 1



A_0	FF-F8	–2
A_1	FE-9A	–57
A_2	EF-E8	–518
A_3	80-DF	+ 23
A_4	80-90	+ 4
A_5	80-C5	+ 17
A_6	FF-F0	–4
A_7	80-9B	+ 6
A_8	80-88	+ 2
A_9	82-D2	+ 84

Fig. 4 Cancellation after preprogramming and adaption; Example 1

EXAMPLE 2

This makes use of a simple operational amplifier and transformer line interface circuit, as shown in Fig. 5. The interface was designed to be matched with $R_L = 560\Omega$ and assumes an inductance from the transformer of 0.7H. Under these conditions this circuit gives a reasonable 30dB of initial cancellation without use of the MV3010. This degrades significantly as the line impedance becomes mismatched with the 2-wire termination impedance. The example given uses a mismatch of 430Ω as the echo test network ($Z_L = 430\Omega$), the cancellation obtained being shown in Fig. 6. Similar to example 1, Fig. 7 shows the spot frequency coefficients and Fig. 8 the cancellation resulting from preprogramming. Lastly, Fig. 9 shows the enhancement obtained by adaption together with the new set of coefficients.

EXAMPLE 3

Example 3 makes use of one of the range of Subscriber Line Interface Circuits (SLICs) available from GEC Plessey Semiconductors, the SL373, to interface the MV3010 to the line. The circuit diagram of the SL373 application is shown in Fig. 10, with a full description of the device given in the data sheet (page 3-3) and applications information given in the SL373/SL376 Application Note AN82 (page 7-18).

The SL373 makes no attempt to separate the directions of transmission such that 100% of the received 2-wire signal is returned to the 4-wire output. With the line impedance balanced at the 2-wire termination (set to 600Ω in this case) this means the nominal 4 to 4-wire gain (echo) is 0dB, as shown in Fig. 11. Spot frequency measurements gave the coefficients of Fig. 12, with better than 45dB of cancellation in each test. The resulting preprogramming coefficients and cancellation are both given in Fig. 11. Following self adaption, an improvement of ~5dB to better than 25dB across the band was obtained as illustrated in Fig. 13, along with the modified coefficients. Lastly, comparing the two curves of Fig. 13 shows the necessity of preprogramming, in this case. This is because the SL373 echo is dominantly centred on coefficient A_2, which is not involved in the adaptive process.

THE COMPUTER PROGRAM

The software for this preprogramming technique was written in PASCAL. It forms part of the MV3010 Evaluation Package, or can be supplied separately for use at a customer location on DEC VAX/VMS, IBM PC or compatibles. Alternatively, the blank form on page 7-74 can be copied, filled out as appropriate, and returned to GEC Plessey Semiconductors as indicated. After this has been processed by the computer, the results can be returned to the customer. It must be remembered that the resulting coefficients, so returned to the customer, will only provide the necessary degree of preprogramming if the spot frequency measurements were made correctly. Finally, as mentioned earlier, the entire preprogramming procedure can be carried out by GEC Plessey Semiconductors if the customer makes the relevant circuit diagrams and/or hardware available.

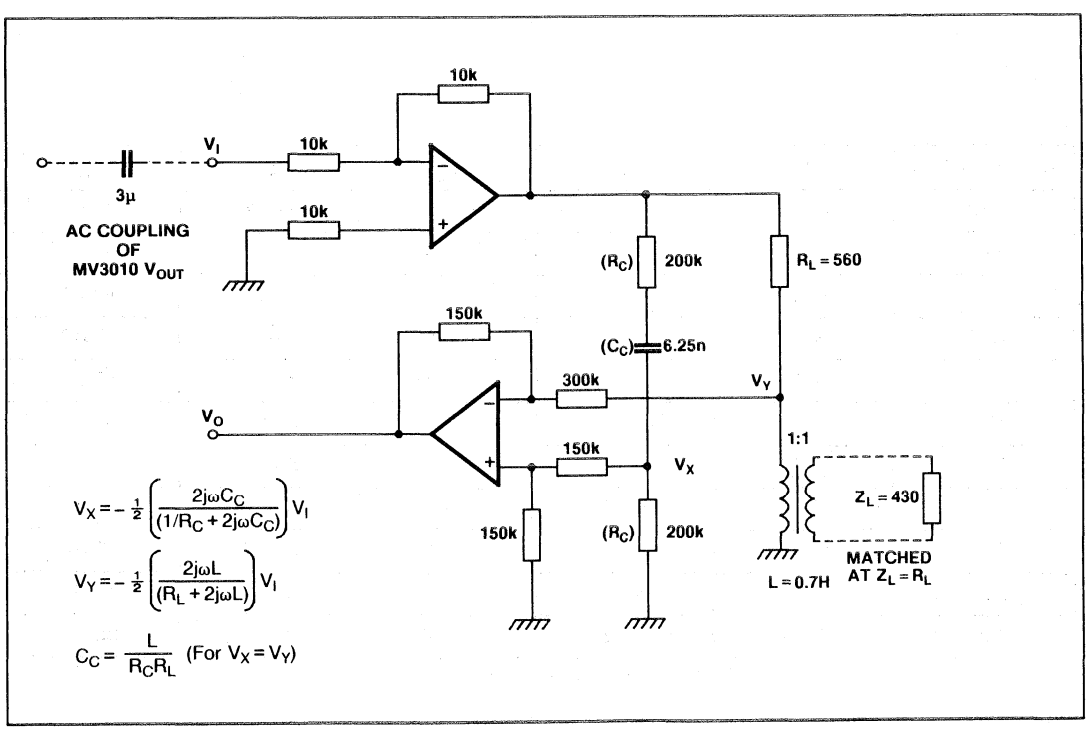
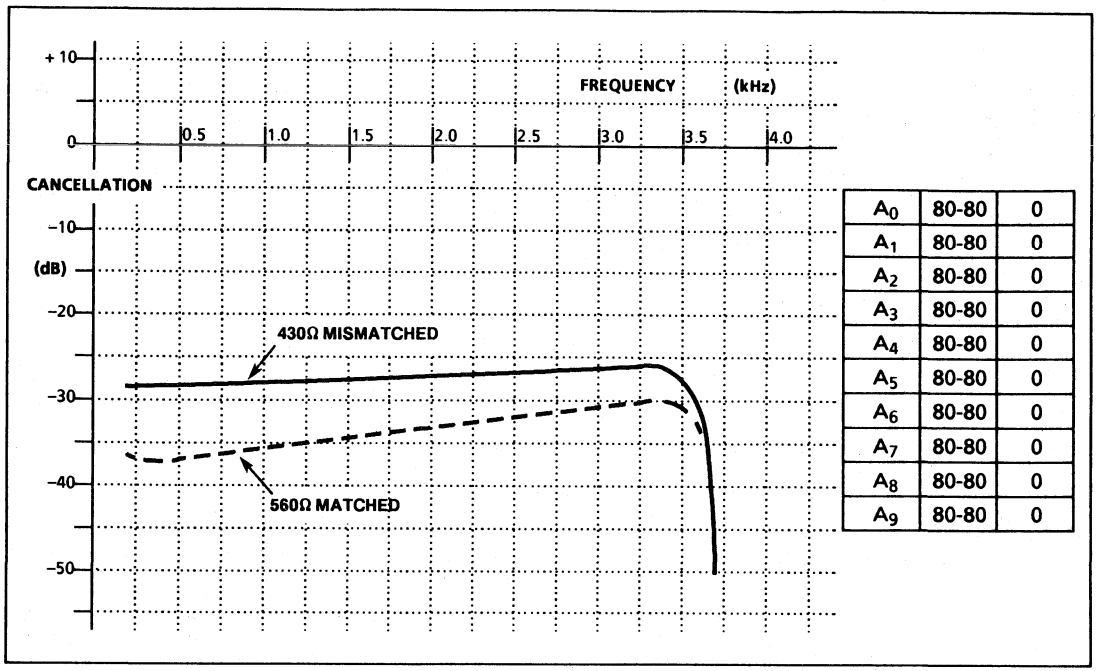


Fig. 5 Simple op amp & transformer line interface circuit; Example 2

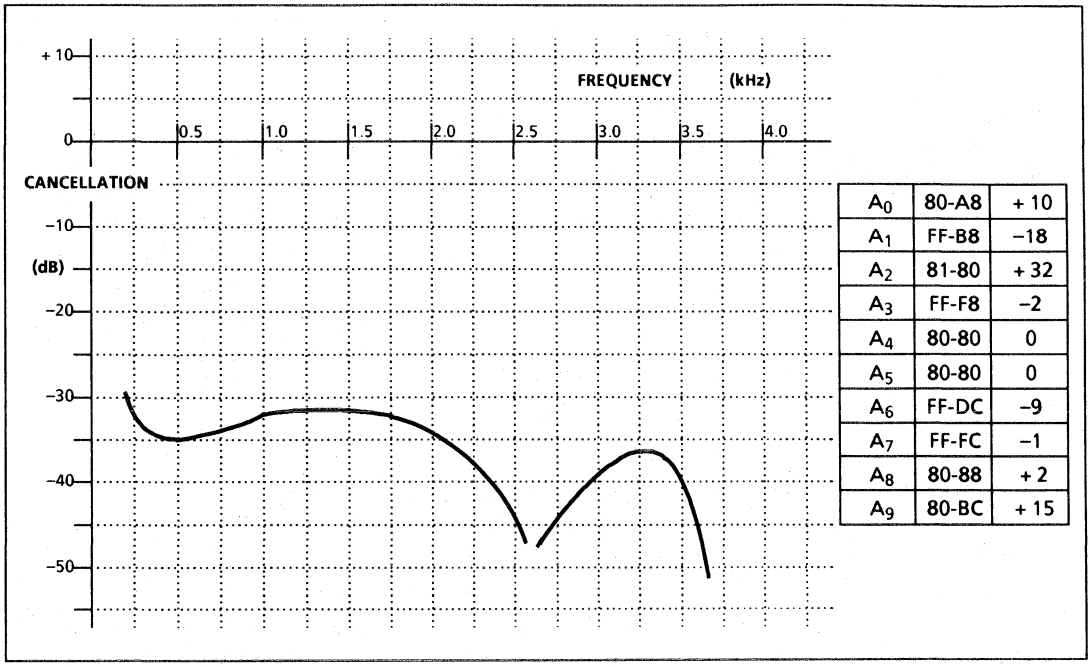


A_0	80-80	0
A_1	80-80	0
A_2	80-80	0
A_3	80-80	0
A_4	80-80	0
A_5	80-80	0
A_6	80-80	0
A_7	80-80	0
A_8	80-80	0
A_9	80-80	0

Fig. 6 Initial cancellation produced using circuit of Fig. 5 (Example 2)

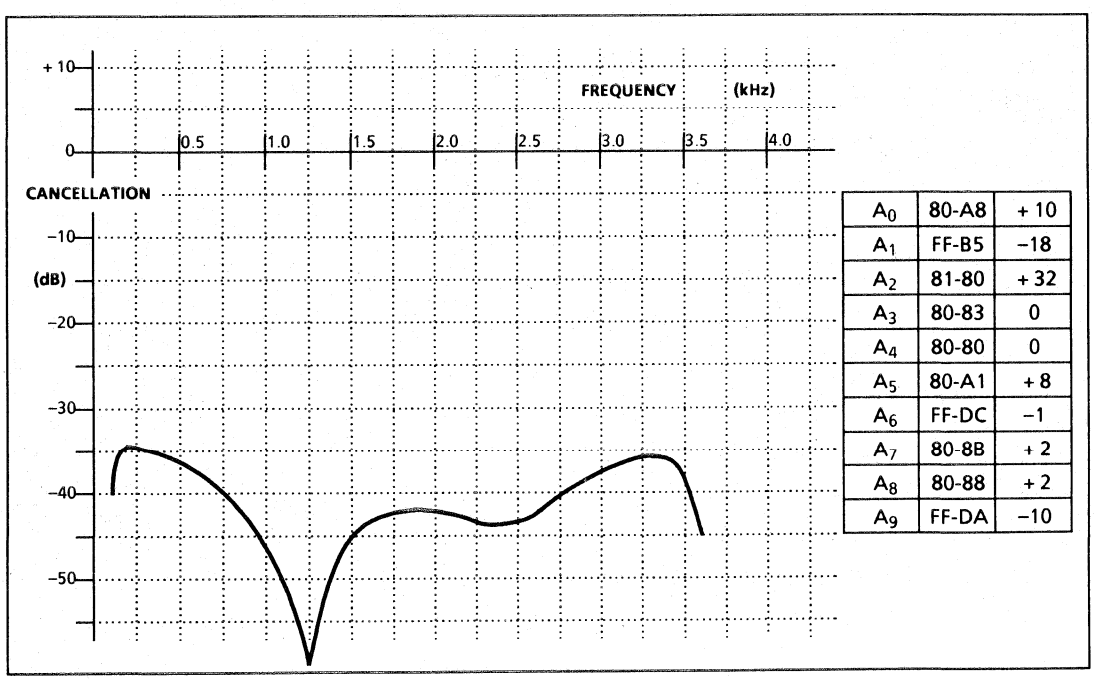
Frequency (Hz)	A_9	A_7	A_5	A_3	A_1
200	81-F9	FD-A2	FF-AA	FE-F8	84-C4
300	FC-F5	81-DB	FF-B4	81-AA	FE-86
500	82-EC	FF-CA	FF-AA	81-B9	80-E8
800	FC-A0	80-C3	FE-99	81-E3	FF-A9
1200	FB-EA	83-91	FA-B5	85-A0	FE-EC
1700	FE-E9	80-D3	FE-D6	81-E3	80-8A
2100	FF-B1	FF-E2	80-80	80-C3	80-AF
2400	FF-CE	FF-F7	FF-F8	80-DF	80-AD
2700	FE-E6	80-94	FF-BC	80-AD	FF-DA
3000	FD-EE	FF-F3	FF-CC	80-C7	80-9F
3300	FF-87	80-95	FF-D8	80-C8	80-AB

Fig. 7 Spot frequency coefficients for Example 2



A_0	80-A8	+ 10
A_1	FF-B8	−18
A_2	81-80	+ 32
A_3	FF-F8	−2
A_4	80-80	0
A_5	80-80	0
A_6	FF-DC	−9
A_7	FF-FC	−1
A_8	80-88	+ 2
A_9	80-BC	+ 15

Fig. 8 Cancellation after preprogramming; Example 2



A_0	80-A8	+ 10
A_1	FF-B5	−18
A_2	81-80	+ 32
A_3	80-83	0
A_4	80-80	0
A_5	80-A1	+ 8
A_6	FF-DC	−1
A_7	80-8B	+ 2
A_8	80-88	+ 2
A_9	FF-DA	−10

Fig. 9 Cancellation after preprogramming and adaption; Example 2

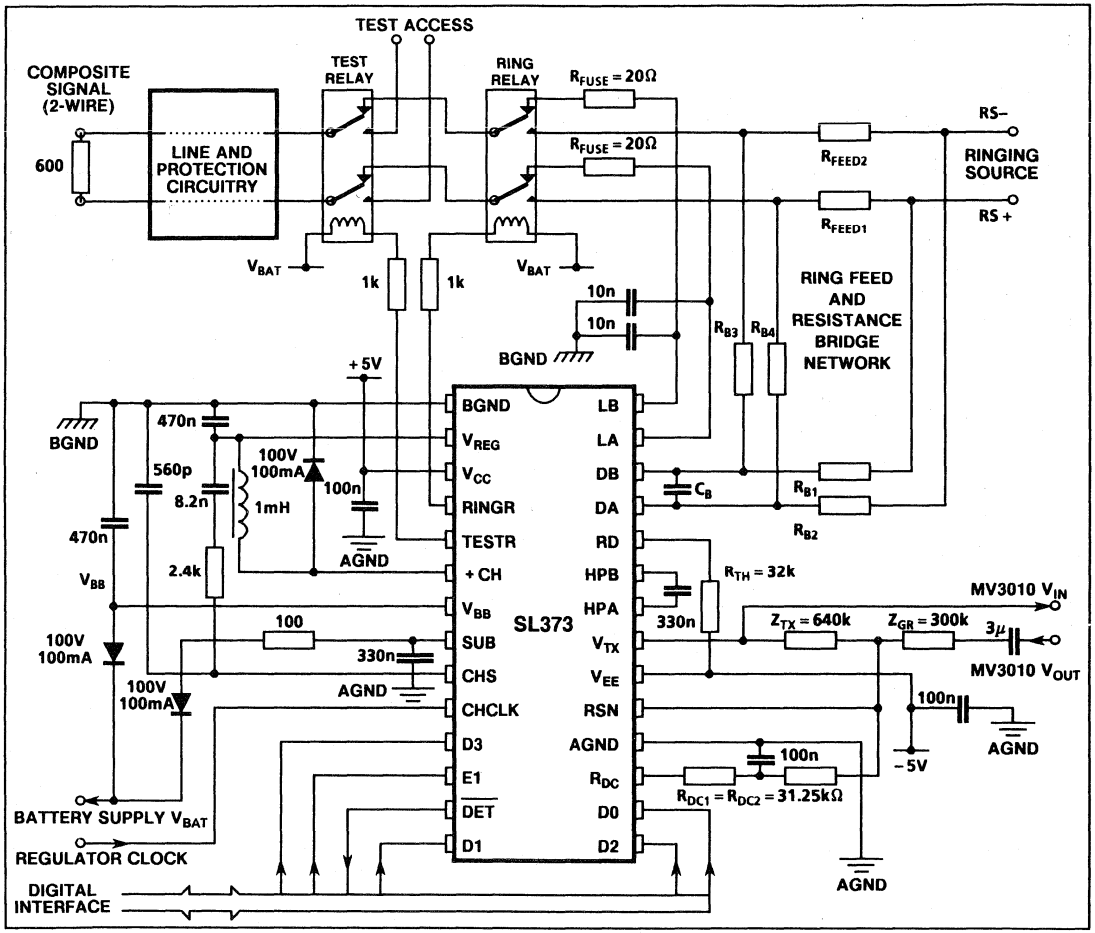
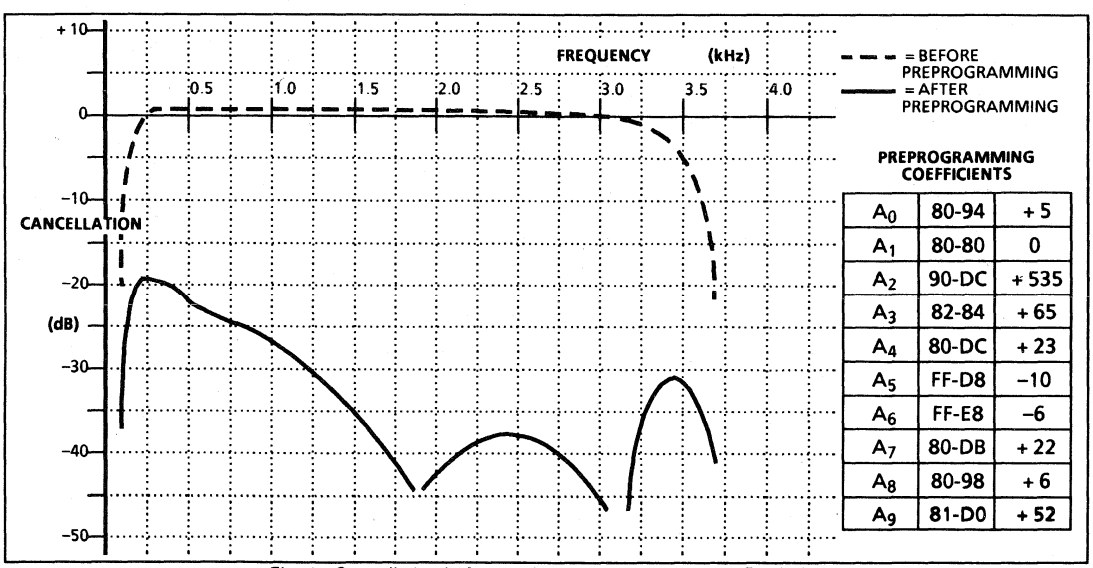


Fig. 10 PSLAC with SL373 SLIC line interface (See SL373data sheet and AN82 for details); Example 3.

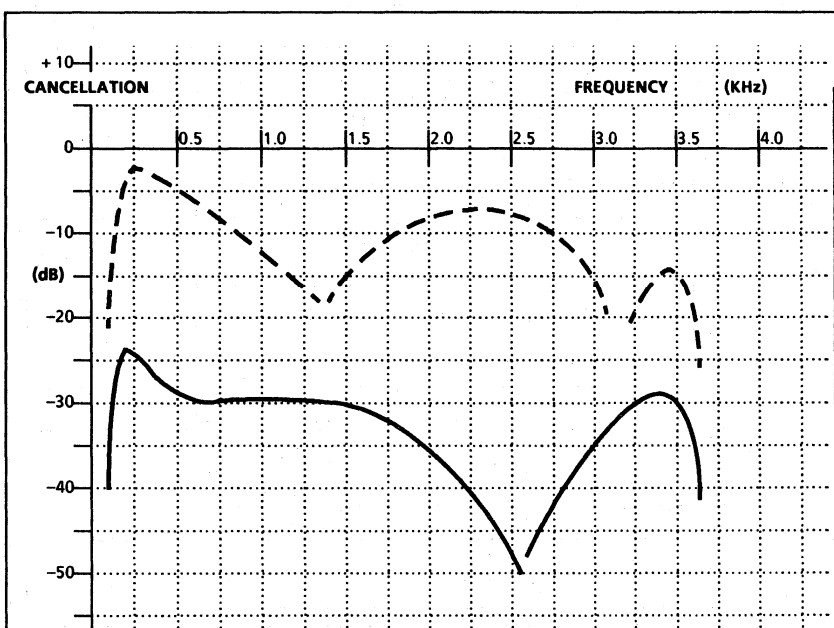


A_0	80-94	+5
A_1	80-80	0
A_2	90-DC	+535
A_3	82-84	+65
A_4	80-DC	+23
A_5	FF-D8	–10
A_6	FF-E8	–6
A_7	80-DB	+22
A_8	80-98	+6
A_9	81-D0	+52

Fig. 11 Cancellation before and after preprogramming; Example 3.

Frequency (Hz)	A_9	A_7	A_5	A_3	A_1
200	80-C6	80-AE	FF-91	88-8F	8A-E8
300	FE-B3	84-9D	FB-86	8A-D8	88-EB
500	F1-DC	85-B3	FB-A2	8A-9F	85-D5
800	86-91	82-B6	FB-C9	8E-DF	88-CA
1200	8E-C1	FF-DC	80-F5	8C-B7	88-A7
1700	85-B4	FC-83	84-DB	87-84	8D-99
2100	80-F7	80-F8	FA-EC	8E-BC	88-91
2400	FE-DF	84-A5	FA-E3	8E-D7	87-DD
2700	FE-D4	82-E9	FA-DE	8D-E6	88-FC
3000	F4-AD	83-E6	FA-EC	8C-EE	8A-DA
3300	FC-B1	86-C4	FA-9F	8B-BE	8D-ED

Fig. 12 Spot frequency coefficients for Example 3.



COEFFICIENTS AFTER ADAPTING FROM A_0-A_9 = 0

A_0	80-80	0
A_1	8E-98	+ 454
A_2	80-80	0
A_3	8E-C0	+ 464
A_4	80-80	0
A_5	FD-8F	-93
A_6	80-80	0
A_7	85-C6	+ 177
A_8	80-80	0
A_9	87-B5	+ 237

COEFFICIENTS AFTER ADAPTING FROM A_0-A_9 = PREPROGRAMMED

A_0	80-94	+ 5
A_1	FF-D7	-11
A_2	90-DC	+ 535
A_3	81-DA	+ 54
A_4	80-DC	+ 23
A_5	FF-B6	+ 20
A_6	FF-E8	-6
A_7	80-A2	+ 8
A_8	80-98	+ 6
A_9	FD-CB	-78

Fig. 13 Cancellation due to daption from C Filter empty and after preprogramming; Example 3

PSLAC MV3010 C FILTER PREPROGRAMMING MEASUREMENTS

Complete Section B and Return to:- TELECOMS MARKETING MANAGER
GEC PLESSEY SEMICONDUCTORS
CHENEY MANOR
SWINDON
WILTS SN2 2QW
UNITED KINGDOM
TELEPHONE (44) 0793 518000
FAX (44) 0793 518411

[A] DESCRIPTION

The GEC Plessey Semiconductors recommended method of preprogramming the PSLAC C Filter, for fixed or self-adaptive mode of operation, uses the self adaptive mode to characterise the line interface (echo path) between PSLAC V_{OUT} and V_{IN} pins. This should be carried out using the PSLAC Evaluation Package. If this is not possible, then the measurement may be done manually using this form. The line interface should be terminated with the desired 'Target Impedance' with the PSLAC operating with default conditions (i.e. transmit and receive gains set to unity). The C Filter is enabled and set to adapt from all coefficients at zero (80-80) for each frequency listed below, ensuring that the correlator is disabled (code B5) to allow adaption to a single tone. The procedure is summarised as follows:-

1. Apply a test signal at the PCM input port (DRA) equivalent to 2V p-p (the exact level is not important).
2. Measure the level of Echo Return Loss (ERL) at the PCM output port (DXA) at the test frequency. This should be at about –50dB for most line interfaces. If this level is not achieved then re-adapt until good ERL results. Adaption can be initiated by switching to another frequency (or to a broad band signal) before returning to the test frequency, should any difficulties be obtained.
3. With the C Filter now set to its nonadaptive state, read out the Hex values of the coefficients via the PSLAC DI/O pin. Details of how this is done are given in the PSLAC Data Sheet. The coefficient order will be A_8, A_6, A_4, A_2, A_0, A_9, A_7, A_5, A_3, A_1 (fixed or nonadaptive taps will of course read zero i.e. 80-80).

[B] SPOT FREQUENCY RESULTS (Hex Values)

FREQUENCY (Hz)	A_9	A_7	A_5	A_3	A_1
200					
300					
500					
800					
1200					
1700					
2100					
2400					
2700					
3000					
3300					

[C] COMPUTER COMBINED COEFFICIENTS

COEFFICIENT	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9
VALUE (HEX)										
BINARY (Normalised to 1024)										

[D] ADDITIONAL INFORMATION

CUSTOMER AND CONTACT:-
LOCATION:-
TELEPHONE:-
APPLICATIONS INFORMATION:-

Form for recording spot frequency measurements.

PABX/Line Card Control Circuit AN42

This application note details how a control circuit and up to 128 Subscriber Line Audio Circuits (SLACs such as the GPS MV3010 PSLAC) can be connected together to form a simple PABX.

The two possible modes of operation of the control circuit are described, showing in each case how it is connected to the matrix of PSLACs. The controller has been designed to interface to an industry standard microprocessor (such as an Intel 8051), and to allow control data to be written and read via the PSLAC's serial control port.

The whole circuit has been designed using 74HCT logic throughout and operates from a single 4MHz clock source generating antiphase 2MHz clock signals.

DESIGN CONCEPT

The basis of the Line Card/PABX controller design utilises the time slot switching capabilities of the PSLAC (MV3010). Each PSLAC can transmit/receive PCM data in 32 (64 in expanded mode of operation) time slots, which can appear on either of two transmit and input at either of two receive ports, A and B. This gives a maximum capacity of 128 time slots, each associated with one PSLAC (i.e. telephone).

Operation of the controller simply allows the serial control information of the PSLACs to be generated by a microprocessor. This processor provides all the necessary intelligence to control call routing, off hook status, gain variations etc in software. Communication with the controller is via the microprocessor interface, designed to suit an industry standard processor, such as the Intel 8051.

CONTENTS

CIRCUIT DESCRIPTION (Refer to Fig. 1)

Microprocessor Interface

This allows control data to be written to and read from the controller. In addition the Control Address data is written to the device, which is then used to control either up to 8 PSLACs directly or one of up to 128 PSLACs at an individual address.

Control Data or Control Address is written under the determination of the A0 input. If A0 = 0, then the data byte from the microprocessor is designated as Control Address. This is then loaded into an eight bit latch on the rising (+ve) edge of the $\overline{WR}$ input. If A0 = 1, then the data byte is designated Control Data. This is loaded into the '299 shift register by a positive edge of the 2M clock during the $\overline{WR}$ = 0 period (see timing diagram, Fig. 2).

It is necessary to ensure that the $\overline{WR}$ pulse is long enough (>500ns) for a 2M rising edge to occur. This limits the 8051 to 10MHz operation. This data will then be sent to the PSLACs, as determined by the $\overline{CAM}$ input, when the $\overline{WR}$ input returns to a logic 1. Note that control data must not be written again to the controller during the next 8µs in order to avoid corruption of the previous data byte.

In order to read Control Data from a PSLAC, the following considerations must be observed. First, note that the PSLAC outputs data following a relevant Control Data word in. Each data byte that is to follow is then clocked out of the PSLAC's DIO pin during subsequent PSLAC $\overline{CS}$ = 0 (active) periods.

Due to the I/O structure of the PSLAC control interface, the output data of the controller must be all ones at these times. This ensures that the controller does not output data that will corrupt the PSLAC output data (open collector output). The microprocessor must therefore write FFH during the referred to $\overline{CS}$ active periods.

Secondly, note that only one data byte out will be held by the controller (in the '299) at any one time. This means that the microprocessor must read from the controller after each successive write of FFH, thus forming an organised sequence. This will ensure that no data is lost. Since it is only possible to read from one PSLAC at a time (see also Control Address Outputs), then a suitable operational procedure would be as follows :

(a) Write Control Address
(b) Write Control Data
(c) Write FFH
(d) Read first Data byte
(e) Write FFH
(f) Read second Data byte
(g) Repeat FFH/Read as necessary until all data has been output.

When the $\overline{RD}$ input = 0, the '299 I/O pins are configured as outputs and shift register data is available at the µD0-µD7 pins.

The $\overline{CS}$ input disables the microprocessor interface when this pin is at logic 1. For normal operation as described, this pin should be held at logic 0.

Output Port

This provides the three connections normally associated with the serial control of a single PSLAC. That is specifically Control Data Input/Out (CDIO) providing input/output for the PSLAC, Control Pin Address ($\overline{CPA}$) providing PSLAC $\overline{CS}$ and Control Clock Output providing the DCLK input.

The CDIO and $\overline{CPA}$ pins become active only after a Control Data byte has been written from the microprocessor (ie A0 = 1). Following the $\overline{WR}$ → 1 transition, the '169 counter counts down through a controlled sequence. This counter provides the $\overline{CPA}$ output directly, and also instructs the '299 register to shift right, providing a CDO output as shown in the timing diagram of Fig. 2.

To obtain acceptance of the CDIO data from the PSLAC, it is first retimed to the 2MB clock. CDIO data is then loaded into the '299 register as the CDO data (all ones) is clocked out. When the once off sequence stops, PSLAC output data is held in the register ready to be read by the microprocessor (see also Microprocessor Interface).

Control Address Outputs & Mode Input

Control Address data from the microprocessor is held in the '574 latch. The outputs of this device can be used in two ways, depending on the $\overline{CAM}$ input.

If the $\overline{CAM}$ input = 1, then the $\overline{CPA}$ signal will strobe the CA0-7 outputs during the PSLAC Control Data load sequence (see section Output Port). If the pins CA0-7 have pull-up resistors to +5V connected, then those outputs that have a 0 loaded into the latch will go low as $\overline{CPA}$. Thus, if one PSLAC $\overline{CS}$ input is connected to each control address output (Fig. 3), control data is sent to each of the 8 PSLACs that has a $\overline{CS}$ low as previously described. This mode can be used when reading data from the PSLACs, only if one of CA0-7 = 0.

Alternatively, if $\overline{CAM}$ = 0, then the '574 outputs are permanently enabled. The 8-bit output byte can now be decoded as an individual PSLAC address. This mode can be used to write/read data to/from a single PSLAC only, of which up to 128 in a PABX are permissible.

Note that in both modes, the CDIO and CCO outputs are common to all PSLACs.

SYSTEMS APPLICATIONS

Line Card Controller

The configuration of controller and PSLACs to form a line card is shown in Fig. 3. Each $\overline{CS}$ input of a PSLAC is driven by one of the CA0-7 outputs. For this application the $\overline{CAM}$ (mode input, Figure 1) = 1 mode is used.

When initialising, or sending common commands to the PSLACs, a Control Address value of 00H can be written to the '574 latch. When the Control Data is written, then all 8 PSLACs are loaded with this data.

If the writing of a Control Data word will cause a PSLAC control data output, or a single PSLAC is to be written to, the Control Address word must contain only one 0 (such as FEH, BFH etc). This ensures that only one PSLAC will output data at a time.

PABX Application

The interconnection of controller and PSLACs to form a simple PABX is shown in Fig. 4. In this application, the PSLACs are organised in 16 blocks of 8 (a line card), each block selected by a one-of-sixteen decoder (Line Card Address). This decoder (e.g. a 74 series '154 or two '138s) acts on the next four most significant bits of CA7-0, that define the Line Card Address (i.e.CA6-3). Each

output of the '154 enables a one-of-eight decoder, associated with each block of 8 PSLACs. All sixteen of these 1-of-8 decoders (e.g. '138) act on the three least significant bits of CA7-0, that define a PSLAC Address. The second enable input of each '138 ($\overline{G2B}$) is driven by $\overline{CPA}$ so that the finally decoded output is enabled as $\overline{CPA}$. Then, since the first enable input ($\overline{G2A}$) of each '138 is enabled exclusively by the '154, only one PSLAC can have an active $\overline{CS}$ input at any one time. This PSLAC is defined by the Line Card Address, CA6-3, and PSLAC Address, CA2-0.

Control Data to and from each PSLAC is achieved on an individual basis. The address of the required PSLAC is sent (written) first to the controller (A0 = 0). With A0 = 1 writes/reads via the microprocessor interface are concerned with this PSLAC only.

PABX Application with Multiple Control

To speed up operation of control when using 128 PSLACs, more than one controller can be used. In this case each controller works in $\overline{CAM}$ = 1 mode controlling 8 PSLACs. This then requires a total of 16 controllers.

Improved operation is obtained by writing Control Address 00H to all controllers for subsequent loading of Control Data to all 128 PSLACs simultaneously. For successful capture of Control Data from the PSLACs the Control Address of every controller is next loaded with an address value containing only one 0 (such as DFH). This ensures only one PSLAC sends data to each controller at this time. Each controller can then be read individually (addressed) by the processor. To obtain Control Data from the other PSLACs, a different Control Address, containing one 0, is used in the same manner just described. Control Data can thus be obtained from each PSLAC by using all of the 8-possible CA0-7 combinations that contain one 0.

Finally, note that when writing Control Data to a common number of PSLACs (not all 128), then using differing combinations of Control Address in each controller can load subsequent data to any number of PSLACs in any combination. Similarly, by using different combinations of CA0-7 (with one or no 0) in each controller, then up to 16 PSLACs in any combination of one per controller can send Control Data to their respective controller.

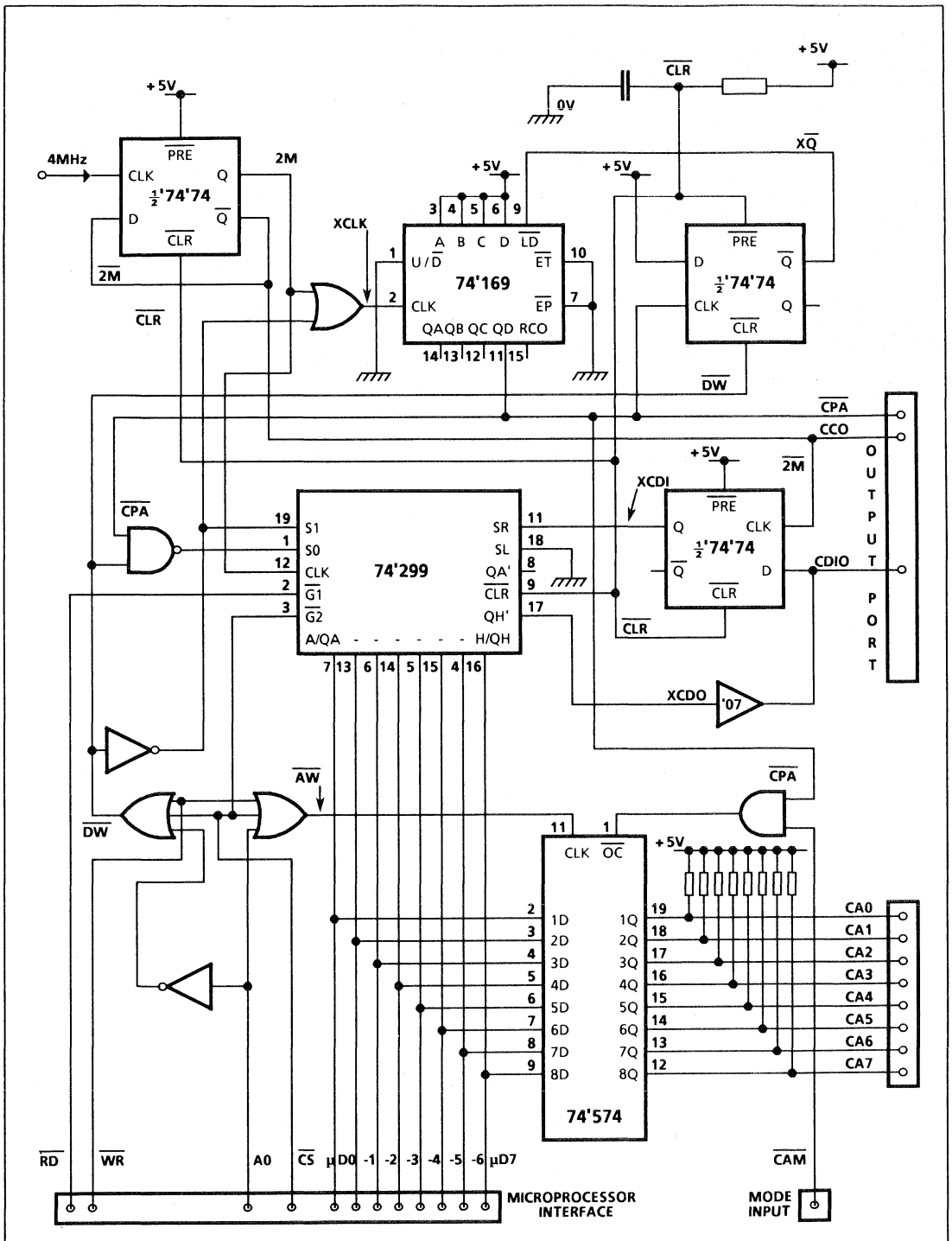


Fig. 1 Line Card Controller logic diagram.

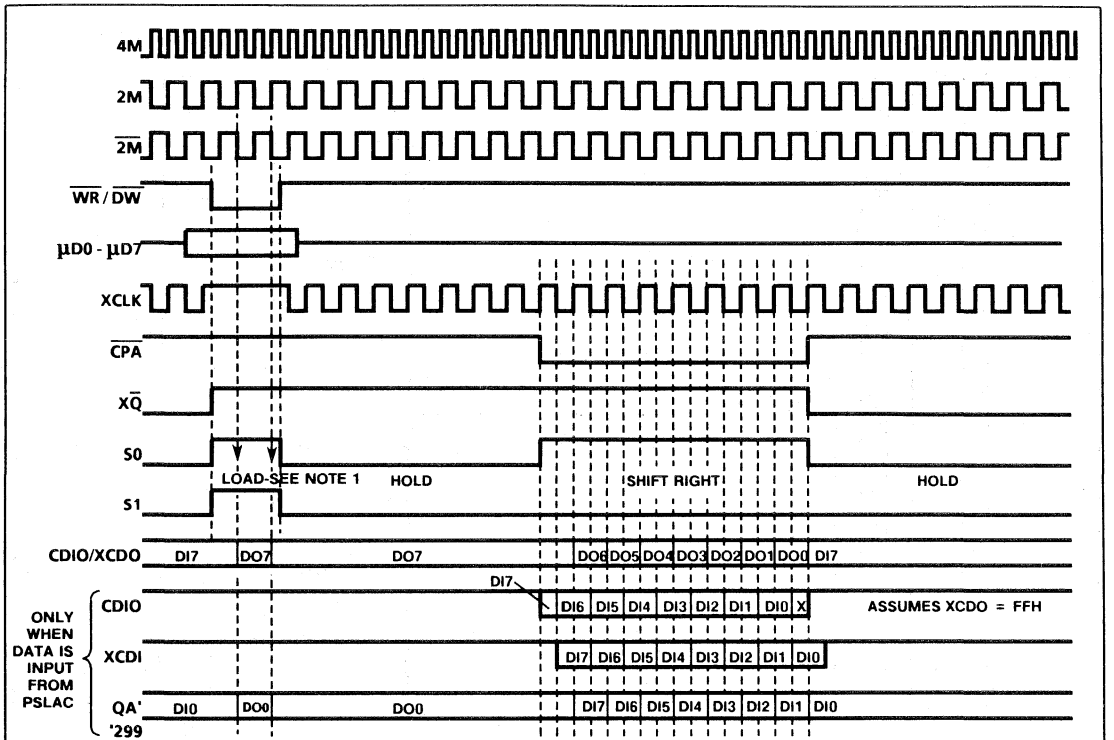


Fig. 2a Control Data sequence. Note 1: $\overline{WR}$ low period must be >500ns-see text

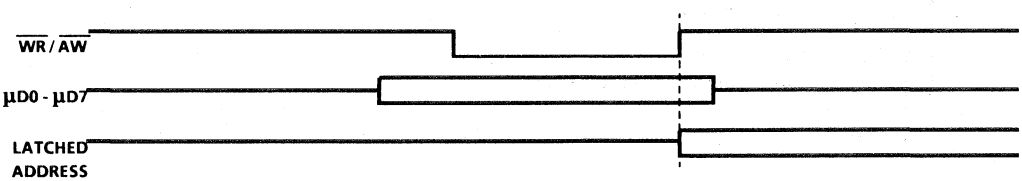


Fig. 2b Microprocessor Write

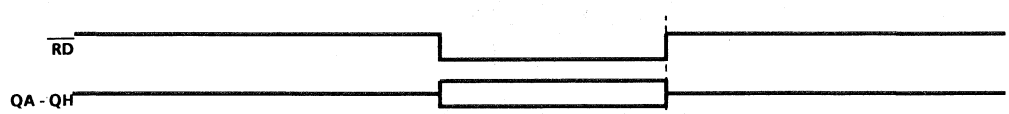


Fig. 2c Microprocessor Read; A0 = X, $\overline{CS}$ = 0, $\overline{WR}$ = 1

Fig. 2 Timing diagrams

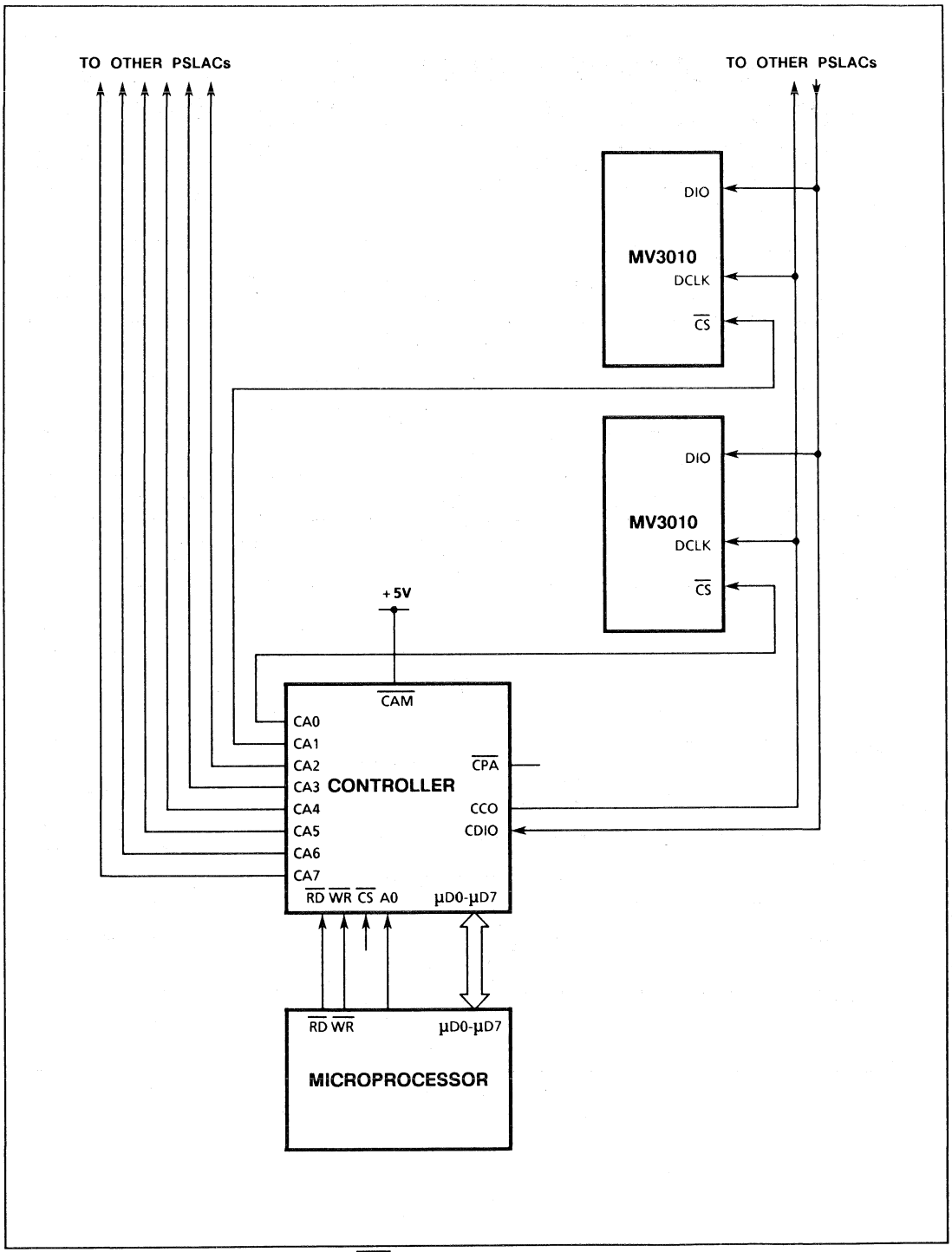


Fig. 3 $\overline{CAM}$ = 1 Mode, Line Card application.

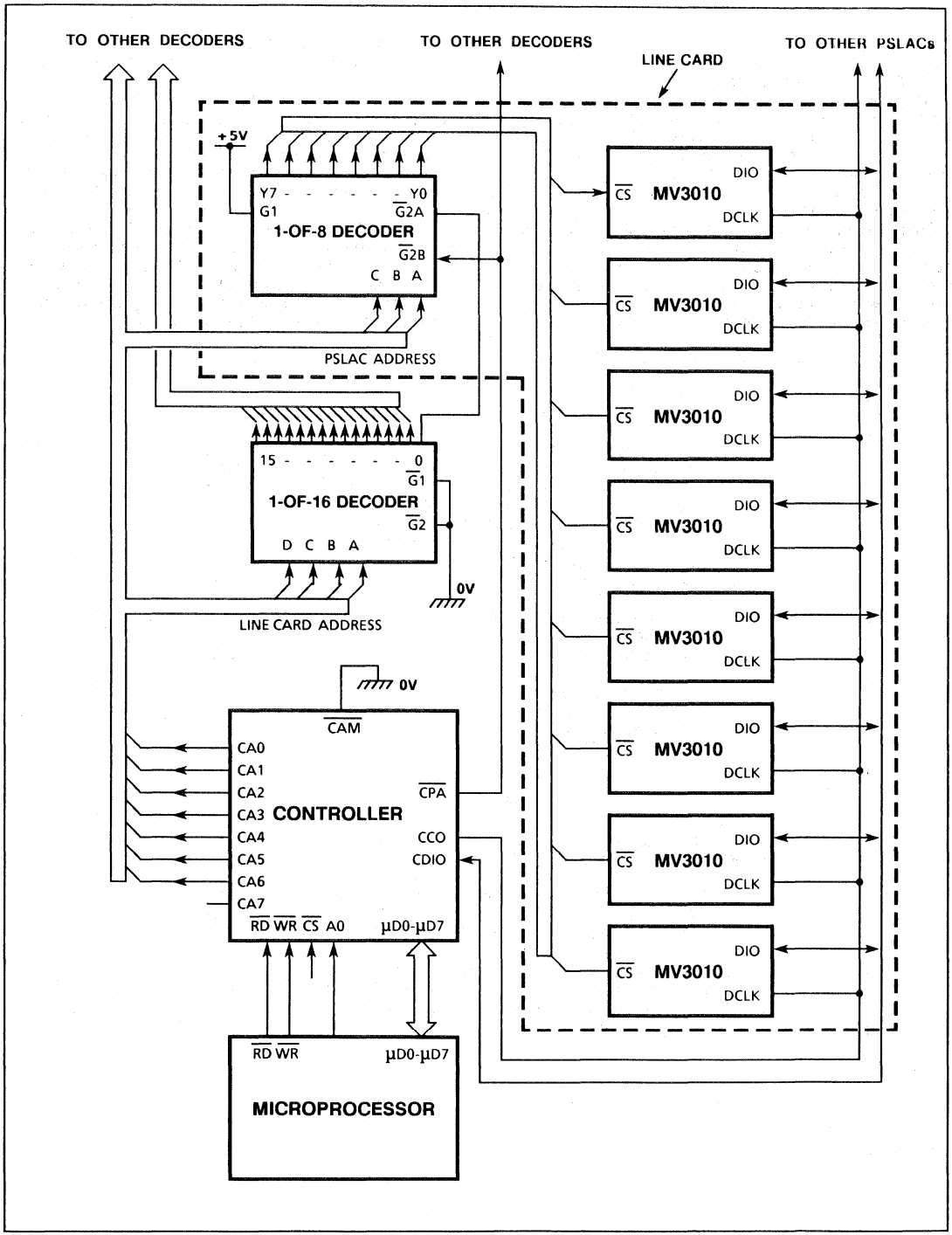


Fig. 4 $\overline{CAM}$ = 0 Mode, PABX Application.

MV3010 Evaluation Package

AN111

This Application Note describes the PCBAN111 evaluation package (see page 3-174) for the MV3010 Subscriber Line Audio Circuit (SLAC). The package contains both hardware and supporting software for use with IBM PCs or compatibles.

Hardware for the evaluation package consists of a circuit board containing two MV3010 devices with full and flexible access to analog and digital ports of both devices. The board has been so designed to operate without any external control facility (Stand Alone option) or by utilising the additional on-board logic, it can be interfaced to an IBM PC or compatible. In the latter case, the software of the evaluation package can be used to fully control/monitor all programmable features of both MV3010s on the circuit board. These features are displayed on a single screen format, one for each MV3010, with additional menu driven screens for access to features of the software.

Since the circuit board was designed with access to the MV3010s PCM ports, the software provides additional features other than control capability. This allows automated preprogramming of C Filter coefficients (using the method as described in Application Note AN84) and measurement/plotting of Echo Return Loss (ERL) performance. Note, however, that since these features require real time transfer of PCM data, this will only be possible with medium-to-high end performance PCs. Note also that running under a multitasking environment such as windows, will degrade the real time transfer rate and may prevent successful PCM data transfer.

CONTENTS

DIAGRAMS

HARDWARE DESCRIPTION

The hardware of the evaluation package is a circuit board which contains two PSLAC devices with associated discrete components and a number of LSTTL devices to buffer the PC interface. Figure 2 shows the circuit schematic with figure 3 showing the PCB layout of the board. The design of the circuit board is such that terminal block connectors TB5, TB6 and TB7 together with uncommitted BNC connectors BNC5,-,BNC9 can be custom wired for interface to a test system. Thus it is possible to use the board in a Stand Alone mode of operation, or if rewired, to interface to a PC (PC Control modes) depending on the connections at the PCCONN socket. Additionally, the board provides on-board clocking (IC3 & IC4) or again by rewiring at TB5,-,TB7, it can be used with external clocks. This flexibility results in five possible modes of operation which will be described later.

An external +5V power supply is required for connection to the AV_{CC} and DV_{CC} supplies of the board, which should be independently connected. Note that the two PCM ports of each PSLAC are connected in a cross coupled arrangement such that (unless combined at TB5,-,TB7) two separate analog-digital-analog paths are formed from one PSLAC to the other. Simple A/D and D/A measurements are possible utilising only one PSLAC with PCM ports available at TB5,-,TB7.

All of the PSLAC analog ports connect via associated discrete components to dedicated BNC sockets on the board, in addition to being available at TB1 and TB3. Thus, TB1 is the analog interface to PSLAC1 and TB3 is the Analog interface for PSLAC2. Resistors R2 and R12 provide DC connection to ground for VIN of PSLAC1 and PSLAC2 respectively. The value of each termination can be user defined by additional resistors R1 and R13. Both the VOUT pins of the PSLACs are AC coupled to the output ports (C2 and C18) to provide necessary DC blocking. This allows direct AOUT→AIN connections on the board. Note that if an AOUT port is driving a high impedance, then it may take some time for the DC conditions to settle.

A list of all components on the circuit board is given in Fig. 4, whilst Figs. 5, 6 and 7 show connection listings for terminal blocks TB1,-,7, BNC1,-,9 and the PCCONN socket respectively.

HARDWARE OPERATING MODES

Listed below are the five possible configurations of the hardware to give the operating modes as described.

STAND ALONE MODE - ON-BOARD CLOCKS

This mode is selected by inserting a 24 pin DIL header in the PCCONN socket. It should be wired as shown in Fig. 8. With this in place, then Active and Standby modes of each PSLAC are controlled by S1 for PSLAC1 and S2 for PSLAC2 (S1/S2 closed sets Standby, S1/S2 open sets Active). On-board clocking is utilised by connecting the following terminal block pins together :-

TB5p2 = TB5p3 = TB5p4
TB7p2 = TB6p4 = TB6p5 = TB6p6

which gives 8K = FS1 = FS2
and 2M = MCLK = CLK2 = CLK1

STAND ALONE MODE - EXTERNAL CLOCKS

Stand alone operation is again used by inserting a header at PCCONN wired as Fig. 8. External clocking can be connected to the terminal block pins as listed on page 7-86 and should meet the static and dynamic requirements as given in the device data sheet.

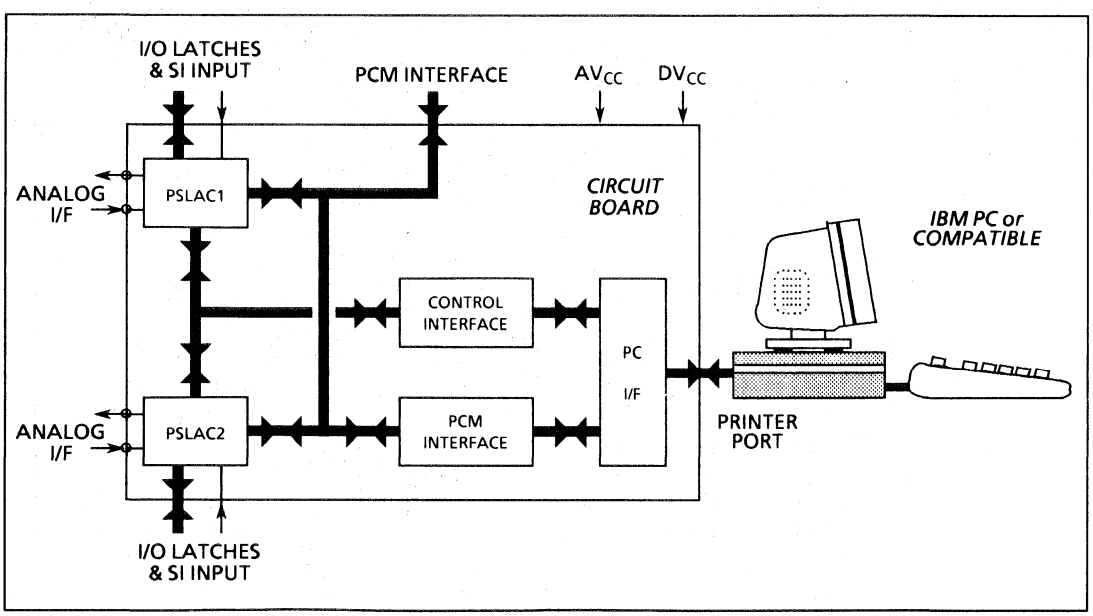
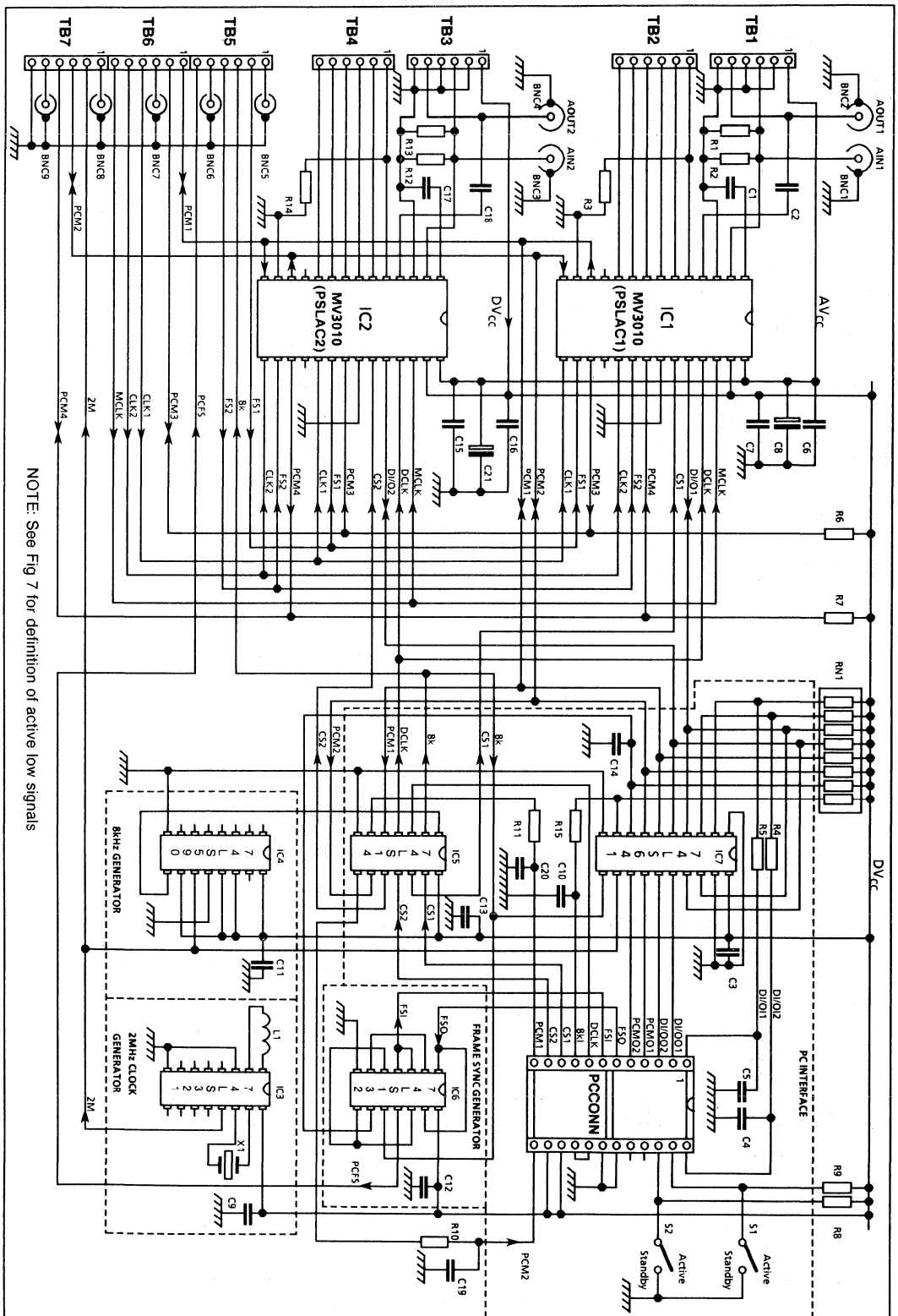


Fig. 1 Block Diagram of Evaluation Package



NOTE: See Fig 7 for definition of active low signals

Fig. 2 Circuit board schematic

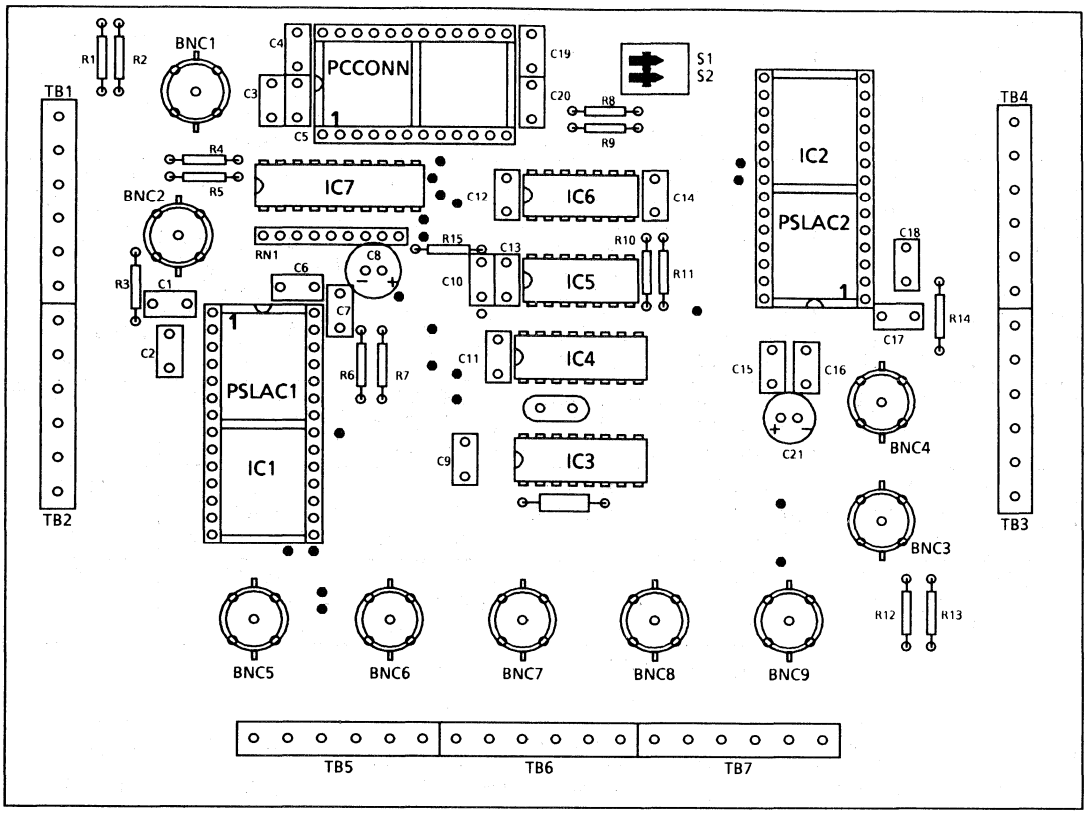


Fig. 3 Circuit board component layout

Name	Value	Name	Value	Name	Value
IC1	MV3010	RN1	8 x 10kΩ	X1	4096kHz Crystal
IC2	MV3010	C1	100nF	L1	330µH Inductor
IC3	74LS321	C2	3.3µF	S1	s.p.s.t Switch
IC4	74LS590	C3	100nF	S2	s.p.s.t Switch
IC5	74LS14	C4	Not fitted	PCC	24 WAY DIL
IC6	74LS132	C5	Not fitted	TB1	Pluggable 6 Way 0.2" Connectors (see Fig. 5)
IC7	74LS641	C6	100nF	TB2	
R1	Termination AIN1	C7	1µF	TB3	
R2	10kΩ	C8	10µF	TB4	
R3	10kΩ	C9	100nF	TB5	
R4	27Ω	C10	Not fitted	TB6	
R5	27Ω	C11	100nF	TB7	
R6	10kΩ	C12	100nF	BNC1	PCB BNC Socket
R7	10kΩ	C13	100nF	BNC2	PCB BNC Socket
R8	10kΩ	C14	33pF	BNC3	PCB BNC Socket
R9	10kΩ	C15	100nF	BNC4	PCB BNC Socket
R10	27Ω	C16	1µF	BNC5	PCB BNC Socket
R11	27Ω	C17	100nF	BNC6	PCB BNC Socket
R12	10kΩ	C18	3.3µF	BNC7	PCB BNC Socket
R13	Termination AIN2	C19	Not fitted	BNC8	PCB BNC Socket
R14	10kΩ	C20	Not fitted	BNC9	PCB BNC Socket
R15	27Ω	C21	10µF		

Fig. 4 Circuit board component listing

Block number	Pin number					
	1	2	3	4	5	6
TB1	AV_{CC} INPUT	0V	AIN1, ANALOG INPUT TO PSLAC1	0V	AOUT1, ANALOG OUTPUT FROM PSLAC1	0V
TB2	SI INPUT PSLAC1	CP1 I/O LATCH PSLAC1	CP2 I/O LATCH PSLAC1	CP3 I/O LATCH PSLAC1	CP4 I/O LATCH PSLAC1	CP5 I/O LATCH PSLAC1
TB3	DV_{CC} INPUT	0V	AIN2, ANALOG INPUT TO PSLAC2	0V	AOUT2, ANALOG OUTPUT FROM PSLAC2	0V
TB4	SI INPUT PSLAC2	CP1 I/O LATCH PSLAC2	CP2 I/O LATCH PSLAC2	CP3 I/O LATCH PSLAC2	CP4 I/O LATCH PSLAC2	CP5 I/O LATCH PSLAC2
TB5	BNC5 I/O U/C SOCKET	FS1 INPUT PSLAC1 to PSLAC2 PCM	8k 8kHz OUTPUT	FS2 INPUT PSLAC2 to PSLAC1 PCM	BNC6 I/O U/C SOCKET	PCFS OUTPUT
TB6	PCM1 DXA PSLAC1 to DRA PSLAC2	PCM3 DXB PSLAC1 to DRB PSLAC2	BNC7 I/O U/C SOCKET	CLK1 PSLAC1 to PSLAC2 PCM	CLK2 PSLAC2 to PSLAC1 PCM	MCLK PSLAC1 and PSLAC2
TB7	BNC8 I/O U/C SOCKET	2M 2MHz O/P INTERNAL CLOCK	PCM2 DXA PSLAC2 to DRA PSLAC1	PCM4 DXB PSLAC2 to DRB PSLAC1	BNC9 I/O U/C SOCKET	0V

Fig. 5 Terminal Blocks TB1..TB7 connection listing

BNC1 = AIN1	BNC4 = AOUT2	BNC7 = UNCOMMITTED
BNC2 = AOUT1	BNC5 = UNCOMMITTED	BNC8 = UNCOMMITTED
BNC3 = AIN2	BNC6 = UNCOMMITTED	BNC9 = UNCOMMITTED

Fig. 6 BNC Sockets BNC1..BNC9 connection listing

Pin number	Name	Description	Pin number	Name	Description
1	DI/OI1	DI/O Output from PSLAC1	24	DI/OI2	DI/O Output from PSLAC2
2	DI/OO1	DI/O Input to PSLAC1	23	S1	Output SWITCH1 Status
3	DI/OO2	DI/O Input to PSLAC2	22	S2	Output SWITCH2 Status
4	PCMO1	Input to PCM1 Bus	21	N/C	No connection
5	PCMO2	Input to PCM2 Bus	20	N/C	No connection
6	FSO	Frame Sync Input from PC	19	0V	Ground
7	FSI	Frame Sync Output to PC	18	0V	Ground
8	$\overline{DCLK}$	Inverse of DCLK from PC	17	16	Internally connects to pin16
9	8kI	Internal 8kHz Output to PC	16	17	Internally connects to pin17
10	$\overline{CS}1$	$\overline{CS}$ Input to PSLAC1 from PC	15	+ 5V	DV_{CC} Supply Output
11	$\overline{CS}2$	$\overline{CS}$ Input to PSLAC2 from PC	14	+ 5V	DV_{CC} Supply Output
12	$\overline{PCM1}$	Inverse of PCM1 Output to PC	13	$\overline{PCM2}$	Inverse of PCM2 Output to PC

Fig. 7 PCCONN connection listing.

TB5p2 = FS1 = 8kHz
TB5p4 = FS2 = 8kHz
TB6p6 = MCLK = 2048kHz
TB6p4 = CLK1 = 64-4096kHz
TB6p5 = CLK2 = 64-4096kHz

PC CONTROL MODE - ON-BOARD CLOCKS

For this mode, the circuit board is connected to a PC parallel printer port via the PCCONN socket with connections made as given in figure 9 (a ready made cable is supplied with the evaluation package). On-board clocks are selected by using the same interconnect for TB5,-,TB7 as the Stand alone case, i.e:-

TB5p2 = TB5p3 = TB5p4
TB7p2 = TB6p4 = TB6p5 = TB6p6

which gives 8k = FS1 = FS2
and 2M = MCLK = CLK2 = CLK1

Control of each PSLAC is now achieved via the supporting software package, as described later. Note that this mode does not support software features that require use of PC generated clocks (auto preprogramming and ERL plots), this mode being described later.

PC CONTROL MODE - EXTERNAL CLOCKS

Keeping the same connections between PCCONN and PC printer port as for on-board clocks, external clocking can be used instead by changing the terminal block connections. These then become the same as for the Stand alone case, i.e:-

TB5p2 = FS1 = 8kHz
TB5p4 = FS2 = 8kHz
TB6p6 = MCLK = 2048kHz
TB6p4 = CLK1 = 64-4096kHz
TB6p5 = CLK2 = 64-4096kHz

again meeting all static and dynamic timing requirements. In order to obtain optimum results for transmission performance measurements, on-board clocking should be disabled. This can be affected by removing IC3 (74LS321) and IC4 (74LS590) from the board. Control of each PSLAC is now achieved via the supporting software package, and again, this mode does not support software features that require use of PC generated clocks.

PC CONTROL MODE - PC GENERATED CLOCKS

To obtain all of the features of the supporting software, the circuit board should be wired for this mode. Again the PCCONN is connected as in Fig. 9. The necessary clocking is obtained by wiring the terminal blocks as follows :-

TB5p2 = TB5p3 = TB5p4
TB7p2 = TB6p6
TB5p6 = TB6p4 = TB6p5

which gives 8k = FS1 = FS2
2M = MCLK
and PCFS = CLK1 = CLK2

SOFTWARE DESCRIPTION

The software is normally supplied on a $5\frac{1}{4}$", 360K floppy disk as an executable file which is written in Turbo Pascal. All displays and menus use the standard textual display format, thus allowing the software to run on any IBM PC/compatible machine. Part of the program caters for display of frequency response measurements for which a graphics card in the PC will be required. Note that the PC must also have a standard parallel printer port to allow connection to the circuit board, as described in the Hardware Description section. With the circuit board wired for one of the PC control modes, the program can now be run.

RUNNING THE PROGRAM

If the program is to be run from the floppy disk, then the command SCAMP is simply entered at the keyboard. However, the program may be copied into a working directory of the PC and run from hard disk, by carrying out appropriate procedures for the PC used. With the program running, operations are mainly menu driven via the PC Function Keys F1-F10 or accessed under cursor control. The menus available are denoted the CONFIGURATION MENU and the MAIN MENU, described later. From the MAIN MENU, access is provided to two SETUP SCREENS (one per PSLAC) to allow control of programmable parameters. The SETUP SCREENS also provide a HELP screen which lists available Function Key options. Fig. 10 shows a basic flow chart for the SCAMP software.

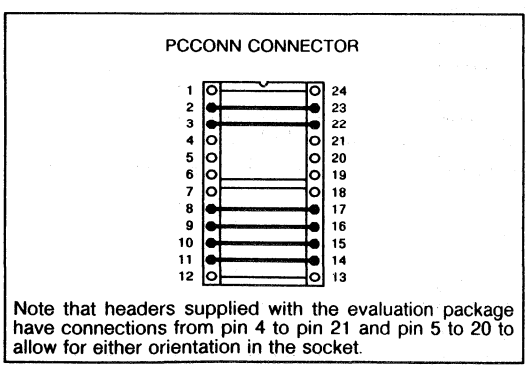


Fig. 8 PCCONN Stand Alone Modes connections.

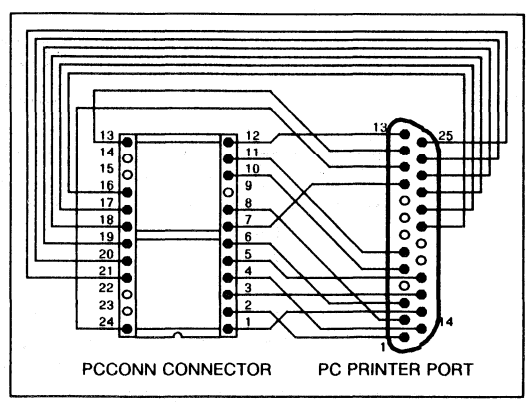


Fig. 9 PCCONN PC Control Modes connections.

The CONFIGURATION MENU is used to reconfigure the PC as required and allow a number of checks on the PC and the hardware connected to the printer port. In contrast, the MAIN MENU runs measurement routines on the selected PSLAC and allows access to the two SETUP SCREENS. The following sections now describe the functions within each screen format in more detail.

THE CONFIGURATION MENU

After entering the command SCAMP, one of two options occur. If the program is being run for the first time, then a file called PSLAC.CON will be created. This contains data on the default printer port, graphics card set up, hardware (circuit board) status and file location. This file is simply read if the program was run previously.

In creating the PSLAC.CON file, the program prompts for entry of a default printer port (i.e. where cable is connected), carries out a check on the existence of that port and if successful, checks the status of the connected hardware via further prompts. These automatically check that command data can be written to and read from each PSLAC on the circuit board (as described for the F5 key of this menu) and then tests PCM transmission capability (as F6 key). After completing these checks, the CONFIGURATION MENU is displayed.

The menu itself has eight associated functions attached to keys F2 and F4-F10. These are listed below along with a brief description of available options :-

F2 KEY : This is used to change the PC printer port used to interface to the circuit board. Three ports numbered 1, 2 or 3 may be selected.

F4 KEY : Changes the hardware status between Disconnected and Connected status. If the status is set to Connected, then appropriate hardware checks will be rerun.

F5 KEY: This key reruns the control hardware status check routine when pressed.

F6 KEY: This reruns the PCM hardware check routine which will fail if the transmit and/or receive PCM verification fail.

F7 KEY: The PSLAC analog ports are tested by this routine, which requires that AIN = AOUT for both PSLACs on the circuit board.

F8 KEY: Toggling through the available graphics card options occurs when pressing this key. Most graphics card types can be automatically detected when set for AUTO (default option), but two types will not be. These are the IBM8514 and ATT400 which can be set explicitly with the remaining two options.

F9 KEY: Toggling to TRUE sets a monochrome mode for text displays (which may be clearer if a monochrome monitor is used with a colour interface card) and sets a higher resolution monochrome mode with low colour resolution graphics card.

F10 KEY: Pressing this key will exit the CONFIGURATION MENU and enter into the MAIN MENU.

THE MAIN MENU

This menu provides control of the PSLAC devices on the circuit board. Again, the PC function keys are used to invoke the available routines. These keys allow access to the SETUP SCREENS for control of PSLAC programmable parameters (described in separate section), run routines for automatic preprogramming of target PSLAC C Filter and plotting of ERL response. A listing of valid function key depressions and associated actions for that key are given on the following page (note that '★' refers to a string of alpha characters).

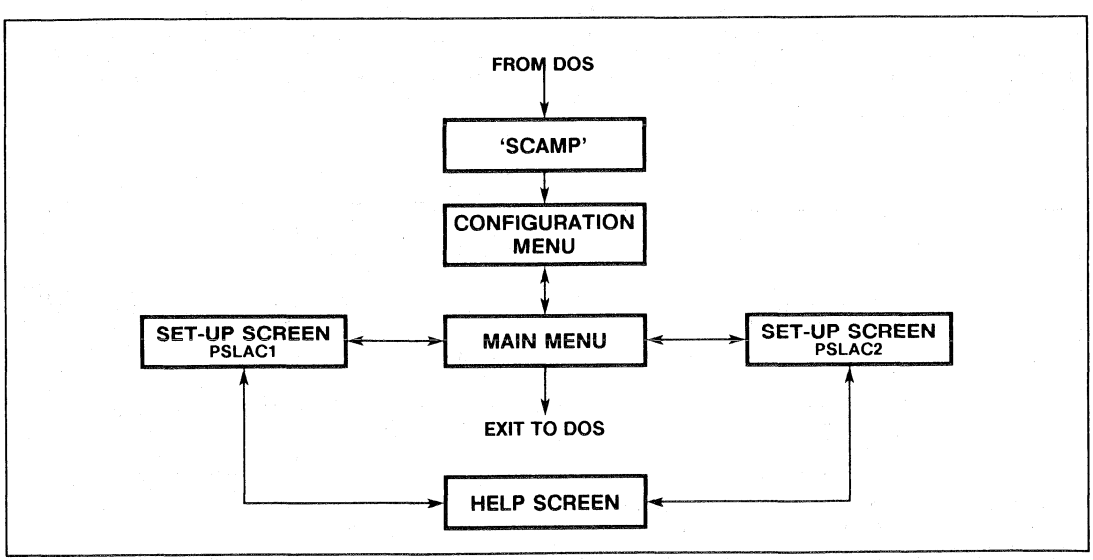


Fig. 10 Basic flow chart for SCAMP software.

F2 KEY : This key returns to the CONFIGURATION MENU.

F3 KEY : Access to the two SETUP SCREENS, one screen per PSLAC of the circuit board, is provided by calling up a filename in the format '★'.SET. Such files contain the status of both PSLACs. If the file is found, then the SETUP SCREENS are entered, else a File Not Found routine occurs and exits back to the MAIN MENU. When running the program for the first time, no setup files will exist such that the F4 key should be used (see later).

F4 KEY : A file "LASTAUTO.SET" is used to enter the SETUP SCREENS. This contains the last used setup data and will be rewritten every time the user exits the SETUP SCREENS. Note that user specific setup files may be created when in the SETUP SCREENS (see later section) in addition to this automatically maintained file. If the program is being run for the first time, then no "LASTAUTO.SET" file will exist, so the program creates one using default parameters when entering the SETUP SCREENS.

F5 KEY : This routine provides automatic preprogramming of the PSLAC adaptive C Filter, and as such requires PCM transmission to be verified (see Configuration Menu F6 Key). Note that only PSLAC1 can be used with this routine such that the target Line Interface should be connected between AOUT1 and AIN1. After prompting for a filename of format '★'.TBL, measurements of spot frequency response (as described in Applications Note AN84) are taken and the results stored in this file. Note that the program uses a temporary '★'.SET file for PSLAC1 status, setting PSLAC2 to DXB to avoid contention with PC generated PCM. Using the same filename as for '★'.TBL, new files will be created in the form '★'.DAT and '★'.SET by entering the preprogramming calculation routine as described for the F6 key, before returning to the MAIN MENU.

F6 KEY After prompting for a '★'.TBL file, the program now carries out a preprogramming calculation for the C Filter coefficients. This generates a set of preprogramming coefficients which are written to an extended version of the input '★'.TBL file and to a new '★'.SET file. The new '★'.SET file contains setup data so that both PSLACs will be programmed into appropriate modes to allow frequency response measurements to be made when using the F7 key on the MAIN MENU.

The time to reach a solution to the preprogramming calculation varies according to the nature of the Echo Response to be matched (i.e. AOUT→AIN). If this proves to take too long, or for any other reason, then key F10 provides an abort option to return to the MAIN MENU.

F7 KEY : The program prompts for a '★'.SET file which would normally have been generated via the F6 key. The setup data in the file allows frequency response measurements to be taken (i.e. PSLAC2 to DXB) with the C Filter of PSLAC1 both disabled and enabled (with preprogrammed calculated coefficients). Measurements are of Echo Return Loss (ERL) from DRA to DXA and assume the target line interface is connected between AOUT1 and AIN1.

The frequencies used for ERL are between 200 and 3500 Hz at a user definable number of points in this range (default = 20). A prompt is made to allow this to be changed. All results at each frequency are written to a text file called '★'.FRQ.

After the '★'.FRQ file has been created, the program allows for entry into the frequency response plot routine (using this file) as described for key F8, provided that a graphics card is present in the PC.

F8 KEY : This allows for on screen plotting of data from the user entered '★'.FRQ file, provided that a graphics card is present in the PC (the CONFIGURATION MENU is used to set the graphics card options) The display shows both sets of results for disabled and enabled C Filter with preprogrammed calculated coefficients.

If a print of the frequency response is required, then note that normally the PCs Print Screen Key (PRS) is disabled while SCAMP is running. However, if the hardware connected status is set to "Disconnected" (F4 key CONFIGURATION MENU) then PRS is enabled while the plots are displayed. As this is a graphics mode display, suitable software to modify the action of PRS for the Printer being used, must have been installed prior to running SCAMP.

SETUP SCREENS

This section describes the use of the SETUP SCREENS which will have been entered via the MAIN MENU (F3/F4 KEY). These screens contain all of the programmable parameters which determine the status of both PSLACs on the circuit board, one screen per PSLAC. When entering the SETUP SCREENS, both PSLACs will be set to the status contained in the '★'.SET file used. Each screen also shows the PSLAC with which it is associated and the format for both is now described.

Fig. 11 shows the format of the SETUP SCREENS, which now include a cursor. This is moved to any one of a number of Parameter Fields using the cursor control keys. These fields occur to the right of each parameter that is displayed on the screen, the available options for each being described in a later section. Such options may be typed manually or selected using function keys F2, F3 and F4. Remaining function keys provide additional features of the SETUP SCREENS as now described below.

Key Options (<S> = SHIFT KEY, <C> = CONTROL KEY)

→ : Moves the cursor to the first character of the next parameter field to the right and initiates transfer of data, as written for the current selection, to the identified PSLAC.

← : Acts as Right Cursor except that cursor moves to the left.

↑ : Moves the cursor up to the next parameter field and initiates transfer of data, as written for the current selection, to the identified PSLAC.

↓ : Acts as up cursor (↑) except that cursor moves down the screen.

<C>→ : Moves the cursor one character to the right within the parameter field. If this is the last character, then the cursor moves to the next parameter field to the right and initiates transfer of data, as written for the current selection, to the identified PSLAC.

<C>← : Acts as CONTROL right cursor except that the cursor moves to the left.

F1 KEY : Invokes the HELP screen which lists available options for the SETUP SCREENS.

F2 KEY : This will toggle the Active/Standby (power down) state of the selected PSLAC.

<S>F2 : Changes display to the SETUP SCREEN of the other PSLAC.

F3 KEY : Each depression of this key causes the currently selected parameter field to decrement one step through the available options.

F4 KEY : Each depression of this key causes the currently selected parameter field to increment one step through the available options.

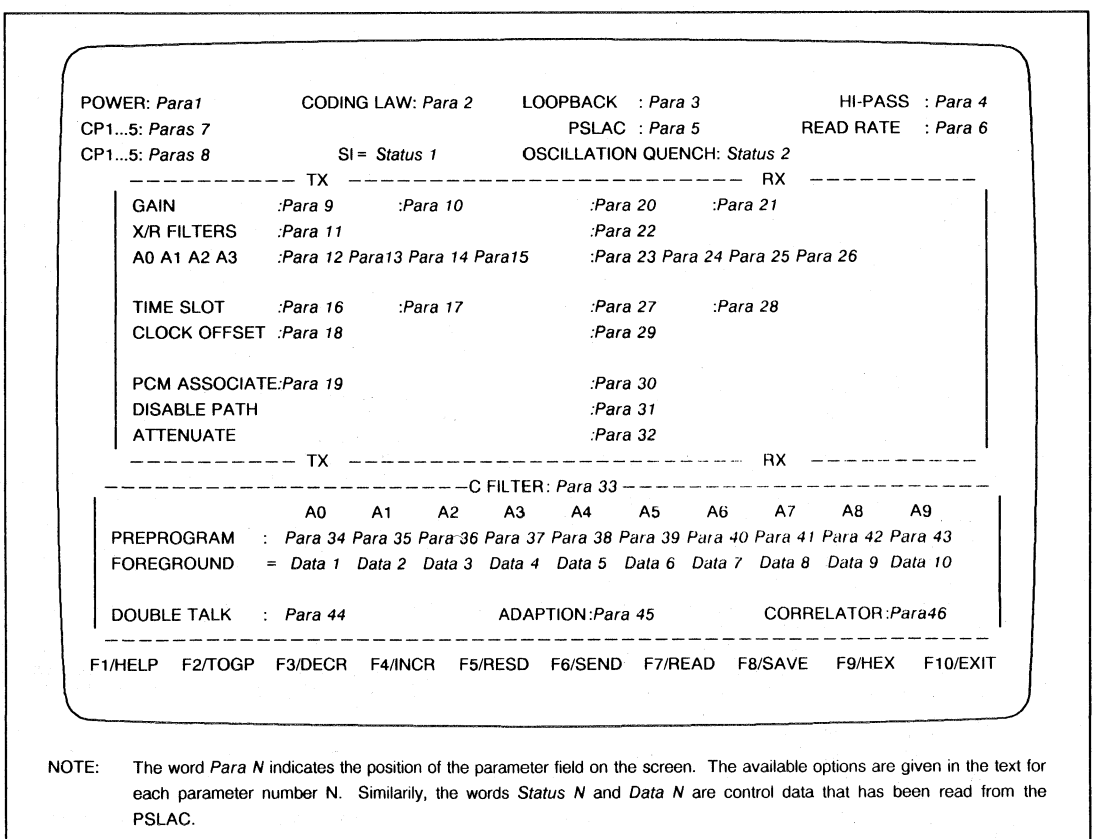
F5 KEY : Depressing this key resets all parameter fields of the SETUP SCREENS to their default setting.

F6 KEY : Each depression of this key causes all of the vailable programmable parameters of each setup screen to be transmitted to the associated PSLAC.

F7 KEY : This will prompt for a '★'.SET setup file and will alter the SETUP SCREENS to the conditions stored in that file. If the file does not exist, the program returns to the SETUP SCREENS after reporting an error.

F8 KEY : The current status of the SETUP SCREENS will be stored in a file '★'.SET entered after the prompt.

F9 KEY : Changes the displayed format of all the PSLAC filter coefficients (X, R and C Filters) from the normalised (to +1024) into HEX data bytes. Also changes display of gain setting data from dBs to HEX.



NOTE: The word *Para N* indicates the position of the parameter field on the screen. The available options are given in the text for each parameter number N. Similarily, the words *Status N* and *Data N* are control data that has been read from the PSLAC.

Fig. 11 SETUP SCREENS format

F10 KEY : This is the escape key to return to the MAIN MENU. Note that each time the SETUP SCREENS are exit, then the file LASTAUTO.SET is modified to the current parameter selection.

Parameter Options

Each programmable parameter field of one setup screen has a number of available options, always associated with the PSLAC of the current setup screen. These are listed below where the *Parameter, Status or Data number* refer to the position on the setup screen as shown in Fig. 11. The format of the list uses *Parameter Number*: Parameter Name: Options A/B/-./X: Description.

Para 1: STATUS: ACTIVE/STANDBY: Places the selected PSLAC in either its Active or Standby (Power Down) mode.

Para 2: PCM CODING: A-LAW/μ-LAW/LINEAR: Changes the PCM coding scheme of the selected PSLAC to the displayed option.

Para 3: LOOPBACK: NONE/ANALOG/DIGITAL: Sets either no loopback or Analog/Digital as displayed.

Para 4: HI-PASS FILTERS: ENABLED/DISABLED: Allows disabling of the selected PSLAC Hi-pass filters as shown.

Para 5: PSLAC: 1/2: Shows the selected PSLAC for each setup screen.

Para 6: READ RATE: 1/2/3/---/255: This relates to the reading of I/O Latches CP1...CP5, reading of the SI pin input level, reading of foreground C Filter coefficients and interrogation of the Oscillation Quench bit. It controls the rate at which data is read from the selected PSLAC in one second steps from 1 to 255 seconds.

Para 7: CP1...CP5 I/O STATUS: I/O: The parameter field consists of a row of five alpha characters which can be either I or O. Letter I sets a CPn latch to input mode and letter O sets a CPn latch to output mode. The five letters across the screen associate with CP1, CP2, CP3, CP4 and CP5 in that order setting latch status accordingly.

Para 8: CP1...CP5 LEVEL: 0/1: The parameter field consists of a row of five numeric characters which can be either 1 or 0. Number 0 implies a low logic level and number 1 implies a high logic level. The five numbers across the screen associate with CP1, CP2, CP3, CP4 and CP5 in that order. If the latch status is input, then this implies a detected logic level and if the latch status is output, then this implies an output condition. The rate at which CPn pins are read from is set by the READ RATE parameter.

Status 1: SI LEVEL: 0/1: The character is 0 or 1 depending on whether the SI pin voltage is at logic low or logic high. The rate at which the pin is read is determined by the READ RATE parameter.

Status 2: OSCILLATION QUENCH: YES/NO: This shows whether the Oscillation Quench bit has been set in accordance with the C Filter operation, as described in the PSLAC Data Sheet. The status is read at intervals as set by the READ RATE parameter. If the status becomes set to YES, then this will remain so until reset to NO by the user.

Para 9: TRANSMIT GAIN: 'VALUE': Sets the Transmit Gain stage of the selected PSLAC to the value of the gain as indicated. 'Value' may be entered in dB or HEX depending on the displayed format as set by the F9 Key.

Para 10: TRANSMIT GAIN: NORMAL/INVERSE: Sets the Transmit Gain stage of the selected PSLAC to Normal (0° phase shift) or Inverse (180° phase shift) as indicated.

Para 11: TRANSMIT FILTER: DISABLED/ENABLED: This is used to disable or enable the selected PSLAC Transmit Filter, as indicated.

Para 12, Para 13, Para 14, Para 15: A0, A1, A2, A3: 'VALUE', 'VALUE', 'VALUE', 'VALUE': Four numbers in the range –2048 to +2047 (in integer steps) set the values of the four Transmit Filter coefficients (refer Data Sheet for format description). Note that coefficients are normally in the range ±2 but are normalised to 1024 for convenience, and may alternatively be displayed in HEX format using the F9 Key of the SETUP SCREENS.

Para 16: TRANSMIT TIME SLOT: 0/1/2/--/63: The entered value in the range 0-63 in integer steps, sets the selected PSLAC transmit time slot for PCM data.

Para 17: TRANSMIT TIME SLOT: NORM/EXPAND: Sets the selected PSLAC transmit PCM format to Normal (0-31) or expanded (32-63) mode of operation (refer Data Sheet for format description).

Para 18: TRANSMIT CLOCK OFFSET: 0/1/-/7: The Transmit PCM of the selected PSLAC will be offset by an integer number of PCM clock periods, depending on the selected value.

Para 19: PCM ASSOCIATE: DXA/DXB: Transmit PCM of the selected PSLAC will appear at the indicated PCM port.

Paras 20 to 30: Note that the PSLAC has complementary types of parameters for the receive path as for the transmit path. Thus there are equivalent parameters available on the SETUP SCREENS (right hand half of upper box - see figure 11) for Receive Gain, Receive Filter status, Receive Filter A0-A3 values, Receive Time Slot, Receive Clock Offset and Receive PCM Port Associate. There are additional parameters applicable only to the Receive Path, which are included in the continuation below, of SETUP SCREENS parameters.

Para 31: RECEIVE PATH DISABLE: NO/YES: This will send the diagnostic code for receive path disable if set to YES. The NO condition clears this state (see also Diagnostic Code Control description).

Para 32: RECEIVE PATH ATTENUATE: 0dB/–6dB: Setting to –6dB sends the diagnostic control code to set 6dB attenuation in the receive path (see also PSLAC Data Sheet). Setting to 0dB clears this condition (see also Diagnostic Code Control description).

Para 33: C FILTER STATUS: DISABLED/ENABLED: This is used to enable or disable the selected PSLAC C FILTER as set.

Para 34, 35, -, 43: PREPROGRAM A0, A1, -, A9: 'VALUE', VALUE',- , 'VALUE': These are ten numbers listed across the screen, each with a Value in the range –2048 to +2047

in integer steps, representing the selected PSLAC C Filter coefficients. Normally values are in the range ±2 but they are normalised to 1024 for convenience. The values may be displayed in HEX format by using the F9 Key on the SETUP SCREENS. Note that it is this set of coefficients that will be preprogrammed from the '★'.SET file of the automatic preprogram calculation routine on the MAIN MENU (applicable to PSLAC1 only).

Data 1, Data 2, -, Data 10: FOREGROUND A0, A1, -, A9: 'VALUE', VALUE',- , 'VALUE': Listed underneath the preprogram values for C Filter coefficients are the ten numbers (also normal to 1024 or HEX format) that represent the foreground C Filter coefficients. These are read from the PSLAC at a rate determined by the READ RATE parameter. Actual values may of course vary from the preprogram data depending on the occurrence of C Filter adaption.

Para 44: C FILTER DOUBLE TALK: 'VALUE': A number in the range –2048 to +2047 sets the selected PSLAC C Filter Double Talk Coefficient (see description in PSLAC Data Sheet). Normally the value is in the range ±2 but it is normalised to 1024 for convenience. The value may be displayed in HEX format by using the F9 Key on the SETUP SCREENS.

Para 45: C FILTER ADAPTION: DISABLED/ IF SI HI/ ENABLED: This parameter controls the adaptive process on the selected PSLAC C Filter. Disabled implies no adaption, Enabled implies adaption and IF SI HI implies that adaption occurs when the SI Input is high (see also description in device Data Sheet).

Para 46: C FILTER CORRELATER: DISABLED/ENABLED: The selected PSLAC C Filter correlator can be disabled or enabled (using the PSLAC diagnostic control codes) as set by this parameter (see also Diagnostic Code Control description).

Diagnostic Code Control

Within each setup screen a number of PSLAC diagnostic codes can be set for the associated device. Since the diagnostic codes contain only a master reset code to reset all diagnostic conditions and no codes to reset individual conditions, the following procedure is adopted. Each time a diagnostic condition is changed, all of the diagnostics will first be reset by sending code B0 via DI/O. The status of all diagnostics is then retransmitted according to the settings on the screen.

Default Settings

The parameter default settings as associated with the F5 Key for the SETUP SCREENS are listed in the PSLAC Data Sheet, and will be as for the first application of power. These are also the default settings used to create the file "LASTAUTO.SET" when the program runs for the first time (i.e. F4 Key on MAIN MENU).

SCAMP ERROR MESSAGES

In order to assist the user in fault diagnosis, a number of error messages have been built into the SCAMP software. These are so designed to aid identification of any problems with the associated hardware and/or software environment. The main error messages that can occur are briefly described below. Note that they may occur separately or in combination with other messages.

"MISSING CONFIG FILE - CREATING ONE CALLED PSLAC.CON"

Usually occurs when the program is run for the first time and no configuration file exists. The program creates one using the default settings.

"CANNOT WRITE TO DEFAULT DIRECTORY - ABORTING"

This will usually occur if the disk containing the PSLAC.CON file is write protected.

"NONEXISTENT PORT"

The selected parallel printer port of the PC does not exist or an illegal entry has been entered.

"DISK IS WRITE PROTECTED"
"DRIVE NOT READY"
"FILE DOES NOT EXIST"
"PATH NOT FOUND"
"ERROR READING FILE"

These are occurrences of the DOS error messages.

"NO / INCORRECT RESPONSE FROM PSLAC"

Occurs during checks of the control port of the PSLACs on the circuit board and implies write to and subsequent read back of coefficients has failed.

"SORRY NOT IMPLEMENTED YET - TO BE INCLUDED IN A LATER RELEASE"

This function key has no operation associated with it, but may do in future SCAMP issues.

"FILE ACCESS ERROR"

This normally occurs in association with one of the DOS error messages.

"NOT A VALID FILE FOR THIS OPERATION"

Each file in SCAMP contains a header to identify the type of file for use in the program. This message implies an error in the header or no such header (i.e. not a SCAMP file).

"HARDWARE PROBLEM - FRAME SYNC SIGNAL NOT DETECTED"

The PCM frame sync signal on the circuit board is not functional or is disconnected; check hardware.

"PSLAC TRANSMITTING PCM MAYBE IN STANDBY STATE - $FF PCM CODES RECEIVED"

The received PCM is at logic high state and a check on hardware operation should be made.

"CANNOT ACHIEVE MINIMUM ACCEPTABLE NULL - ABORTING MEASUREMENT SEQUENCE"

The C Filter automatic preprogram routine contains a target value for spot frequency measurements. If this minimum level of cancellation is not achieved for any one measurement frequency, then the process is aborted. A check should be made on the target line interface and/or associated hardware.

"NOT ENOUGH SPACE ON THIS DISK TO SAVE RESULTS"

Occurs if the program cannot find enough disk space to store data or results. Any unwanted files should be deleted to make space or a new SCAMP disk inserted.

"DATA PORT"
"CONTROL PORT"
"DATA AND CONTROL PORT"

These are error reports associated with the PC internal hardware, and occur during the hardware test routines to identify problems with the data port and/or control port of the selected I/O port of the PC. Appropriate checks should therefore be made.

"CONTROL DATA HARDWARE PSLAC N"

Occurs during testing of the control interface to the circuit board, and may be associated with other error messages. Appropriate checks should therefore be made.

"PCM HARDWARE PSLAC N
CHECK CLK1, CLK2 ARE CONNECTED TO PCFS ON CONNECTOR BLOCK OR PC MAY NOT BE FAST ENOUGH OR OTHER PROBLEM"

Identifies problems associated with the PCM interface to the circuit board, and appropriate checks should be made.

"ANALOG LOOP CHECK, PSLAC N"

Identifies the PSLAC undergoing analog loop verification, and occurs as part of any error report should verification fail.

"PSLAC N"

Occurs as part of an error report to identify a given PSLAC.

"H/W ERROR. FRAME SYNC SIGNAL IS NOT ASSERTED"

Indicates that the FS signal is continually low and that the hardware should be checked.

"H/W ERROR. FRAME SYNC SIGNAL IS CONTINUALLY ASSERTED"

Indicates that the FS signal is continually high and that the hardware should be checked.

"NOT ENOUGH MEMORY TO CREATE PCM TEST SEQUENCE"

During testing of the PCM transmission capability, a PCM sequence is generated and results of received PCM stored for analysis. This indicates that memory space is insufficient for this to take place and corrective measures will be required.

"PCM HARDWARE MUST BE VERIFIED BEFORE TAKING MEASUREMENTS
GO TO CONFIG MENU TO RUN HARDWARE CHECKS"

When running preprogramming or ERL measurement routines the hardware status in the CONFIG menu should be verified. This indicates that the status is incorrect for these routines to be implemented and corrective action, as described, should be taken.

"NO GRAPHICS CARD DETECTED"

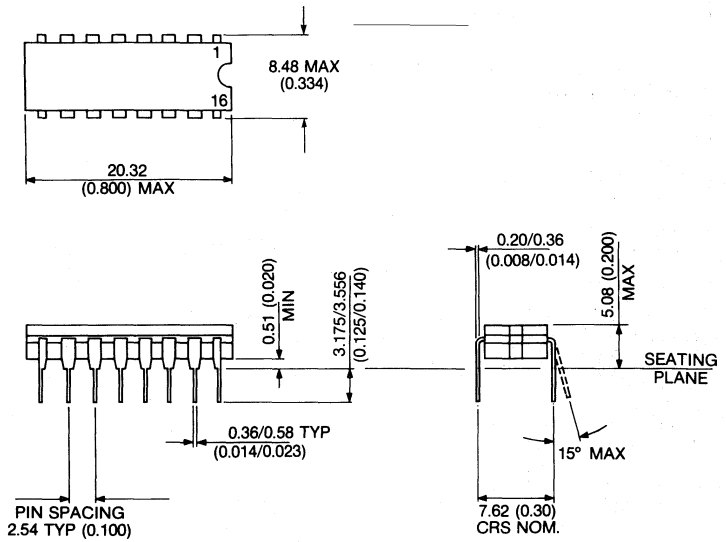
There is no graphics card in the PC or the program is unable to detect it. This will occur for example when trying to display ERL plots.

"ERROR WHILE ATTEMPTING INIT GRAPH"

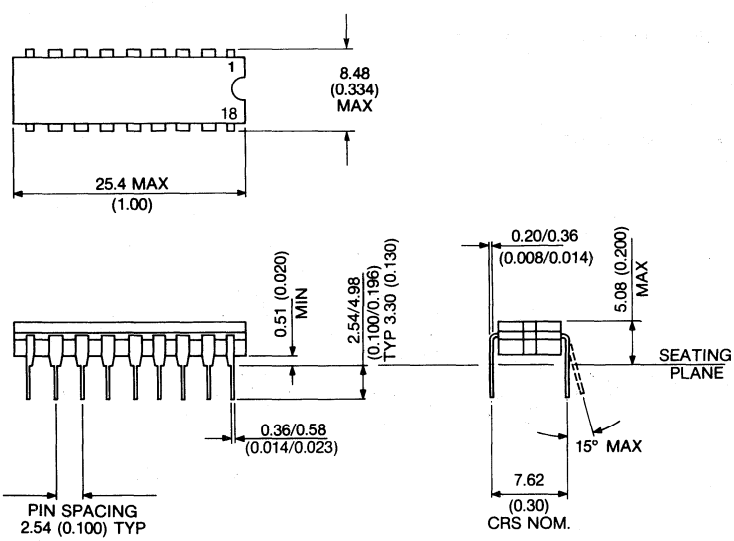
This error message may occur if the graphics card is not a type that is catered for by SCAMP and therefore it cannot successfully be initialised.

Section 8
Package Outlines

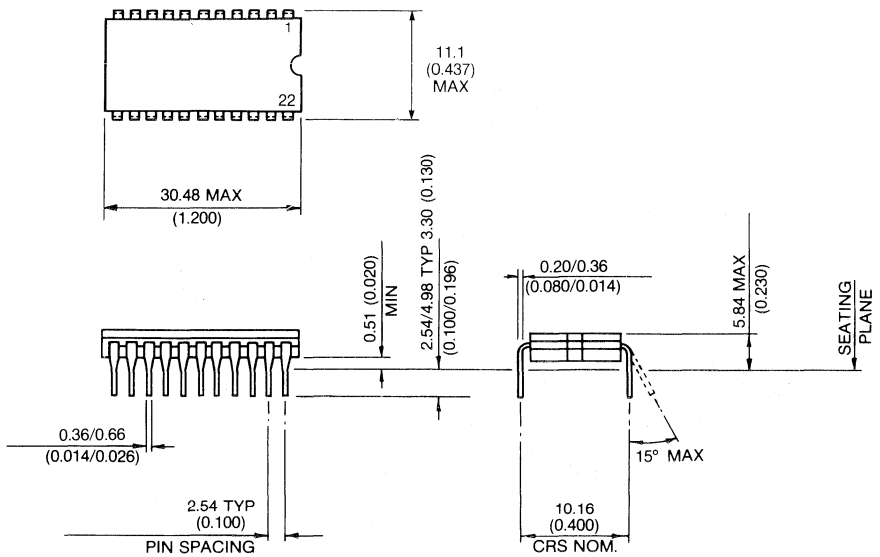
NOTE: On all package outlines, dimensions are shown thus: mm (in).



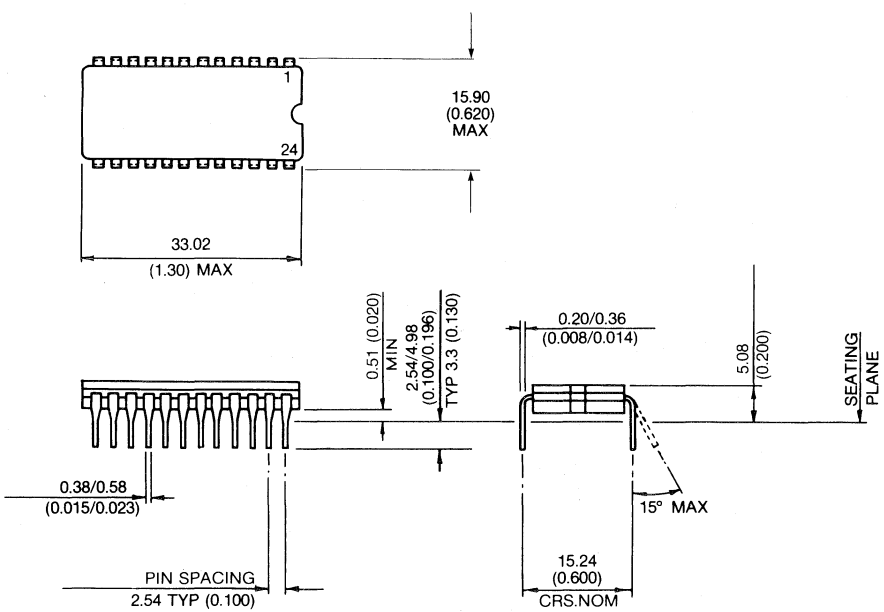
16-LEAD CERAMIC DIL - DG16



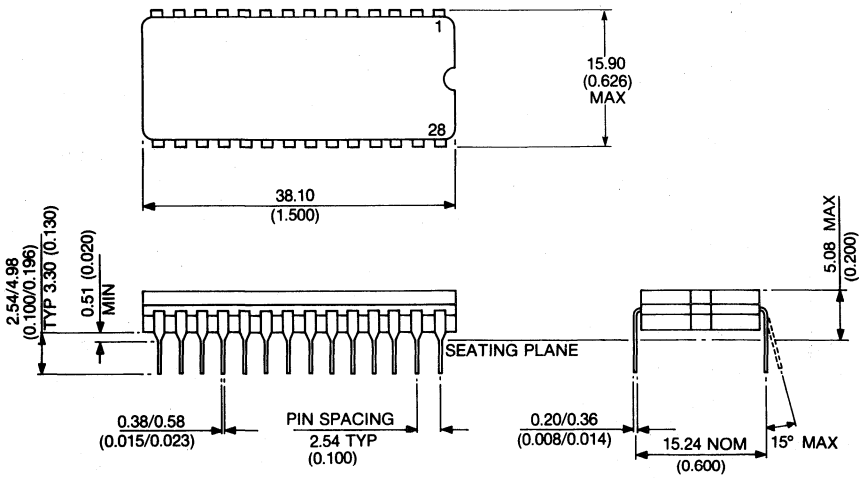
18-LEAD CERAMIC DIL - DG18



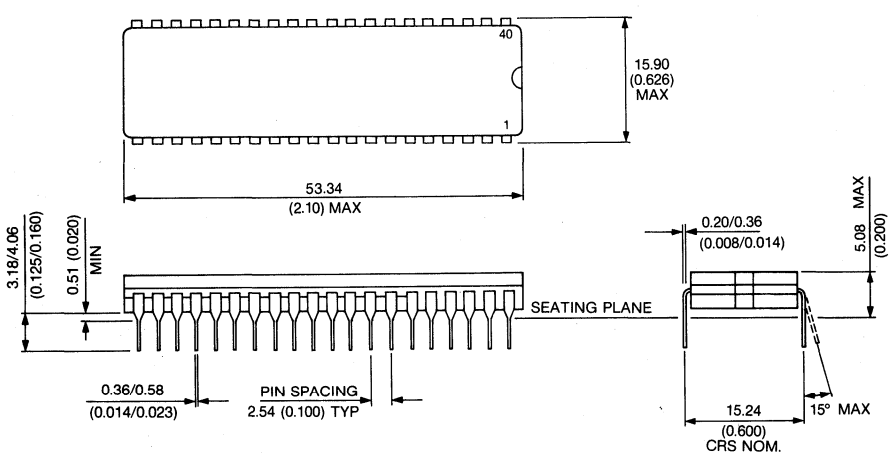
22-LEAD CERAMIC DIL - DG22



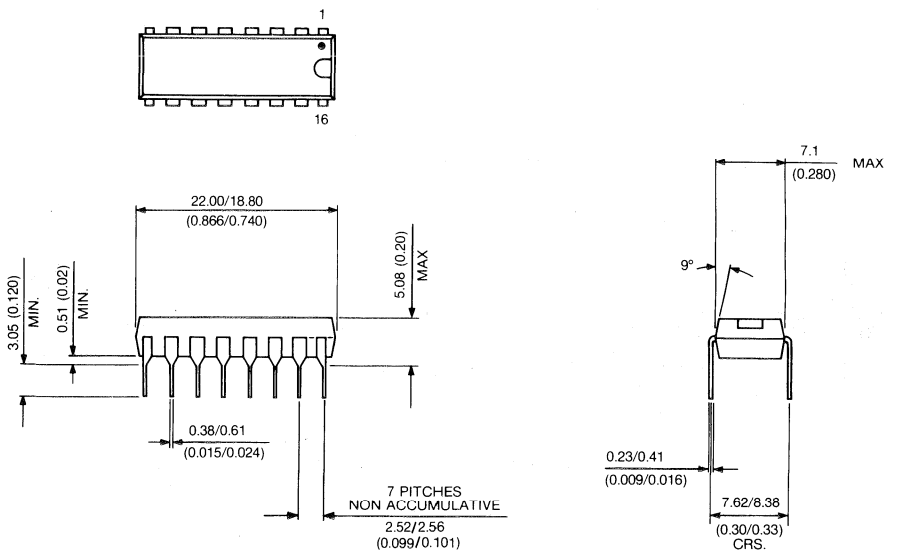
24 LEAD CERAMIC DIL - DG24



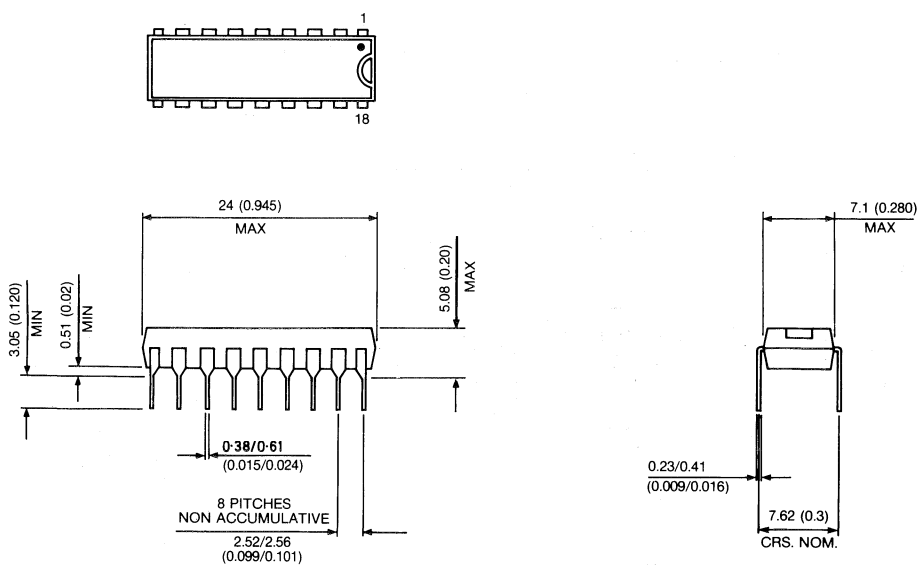
28-LEAD CERAMIC DIL - DG28



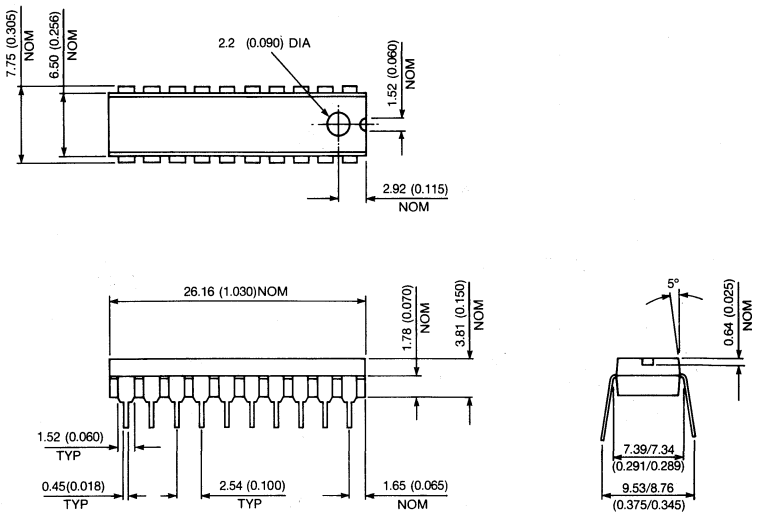
40-LEAD CERAMIC DIL CERDIP - DG40



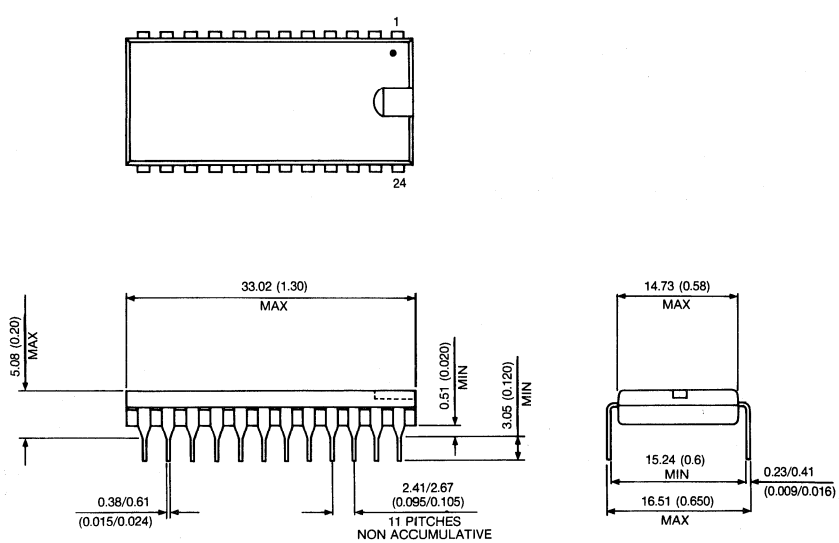
16-LEAD PLASTIC DIL - DP16



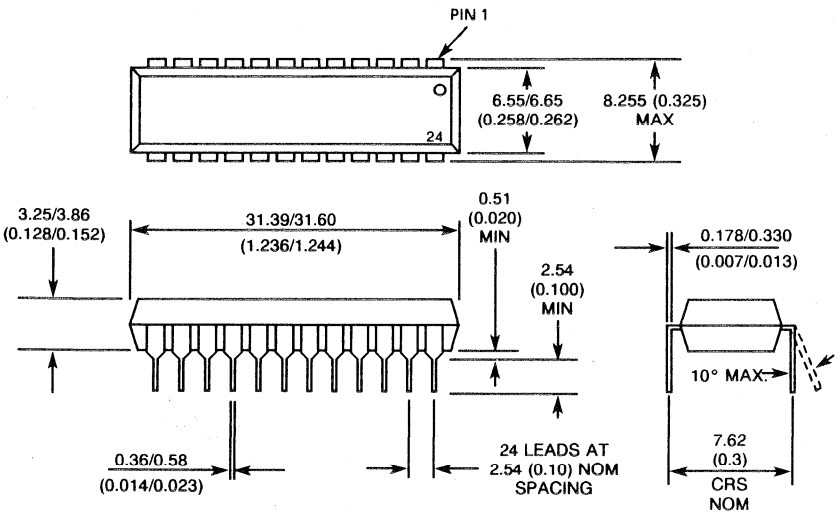
18-LEAD PLASTIC DIL - DP18



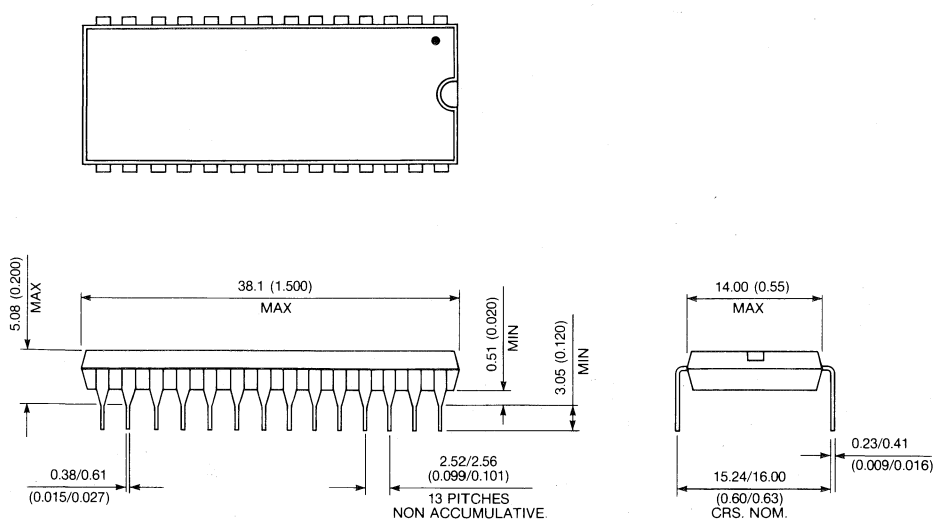
20 LEAD PLASTIC DIL – DP20



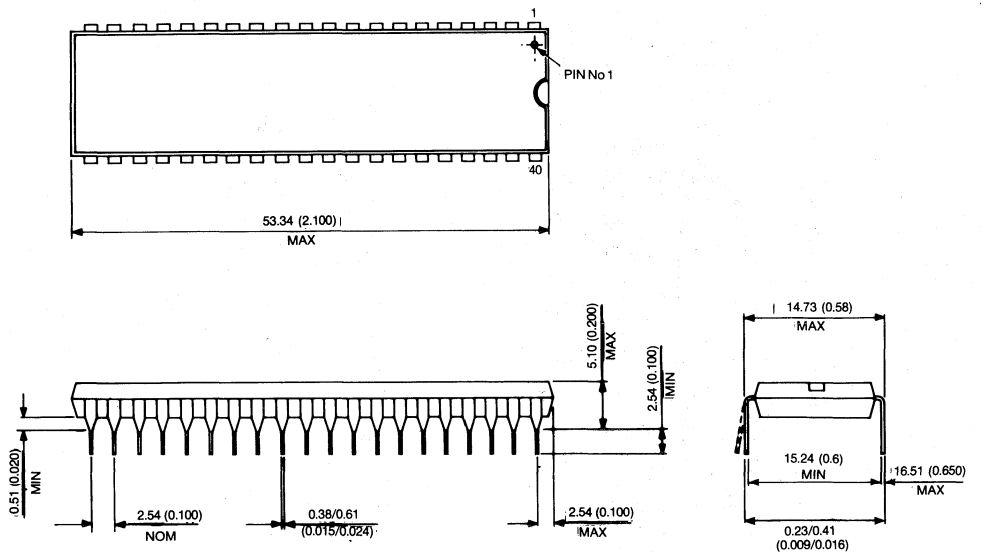
24-LEAD PLASTIC DIL - DP24



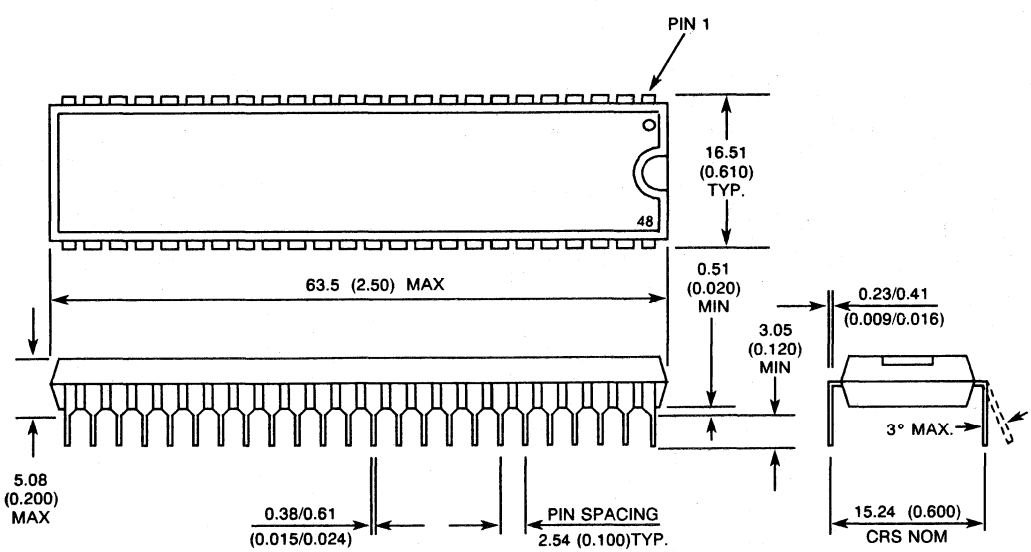
24- LEAD PLASTIC DIL (SKINNYDIP) - DP24/S



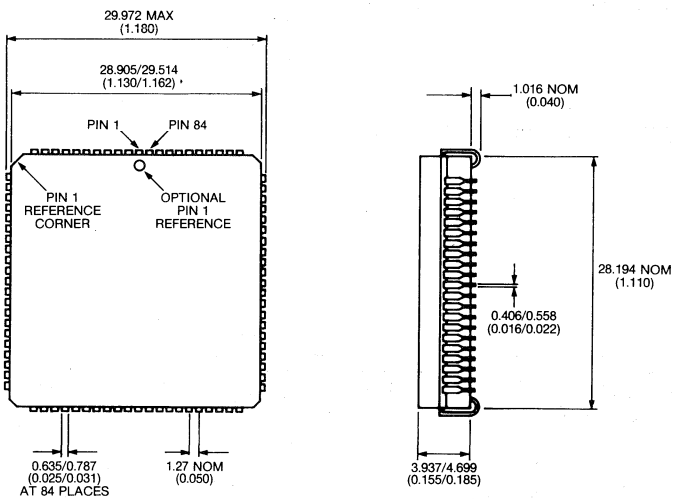
28-LEAD PLASTIC DIL - DP28



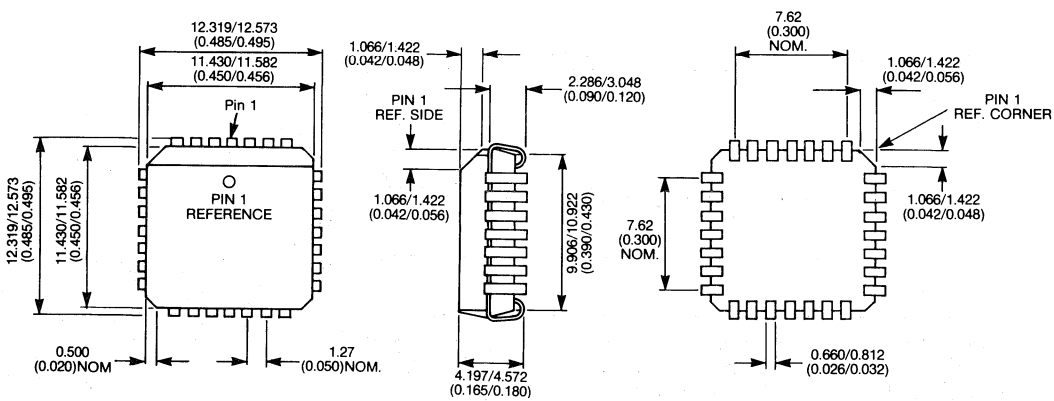
40 LEAD PLASTIC DIL - DP40



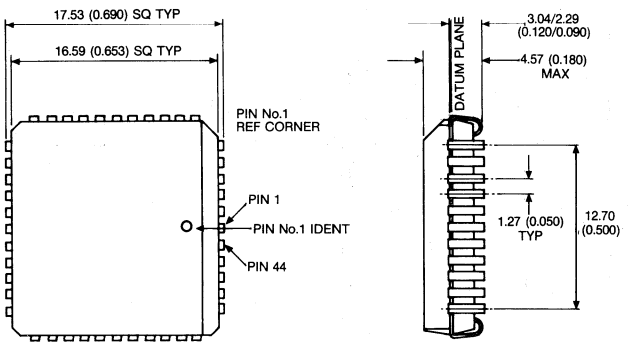
48- LEAD PLASTIC DIL - DP48



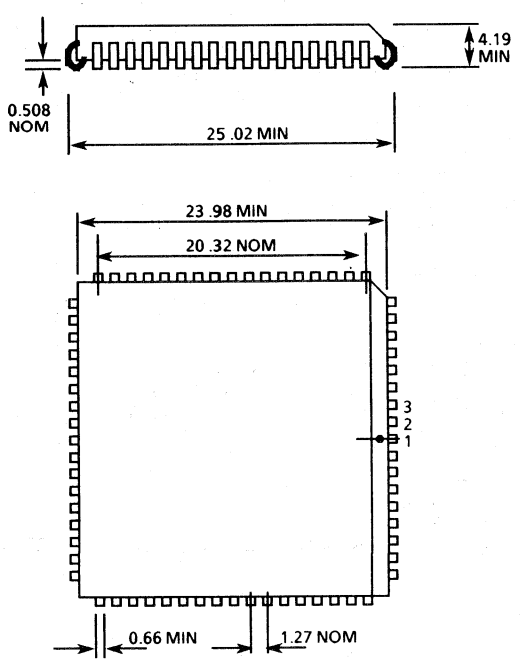
84-LEAD QUAD CERPAC CHIP CARRIER - HG84



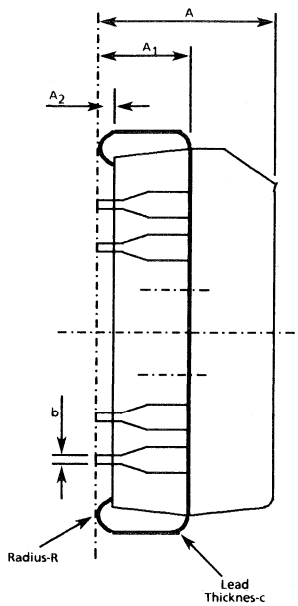
28-LEAD QUAD PLASTIC J LEAD - HP28

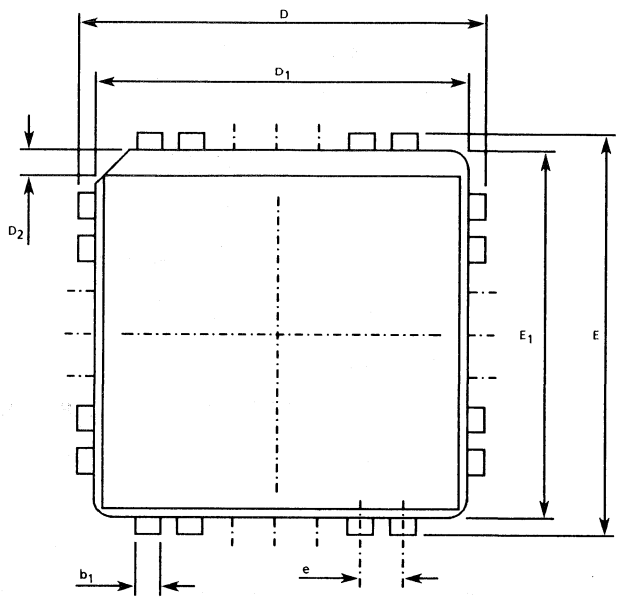


44-LEAD QUAD PLASTIC J LEAD - HP44

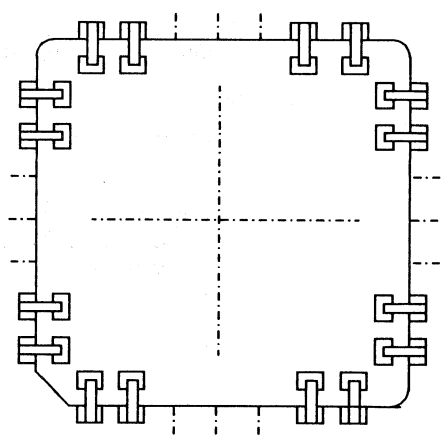


68-LEAD MOULDED PLASTIC J LEAD - HP 68

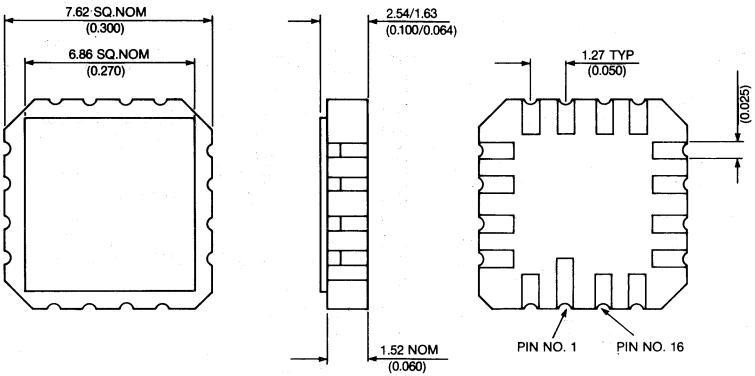




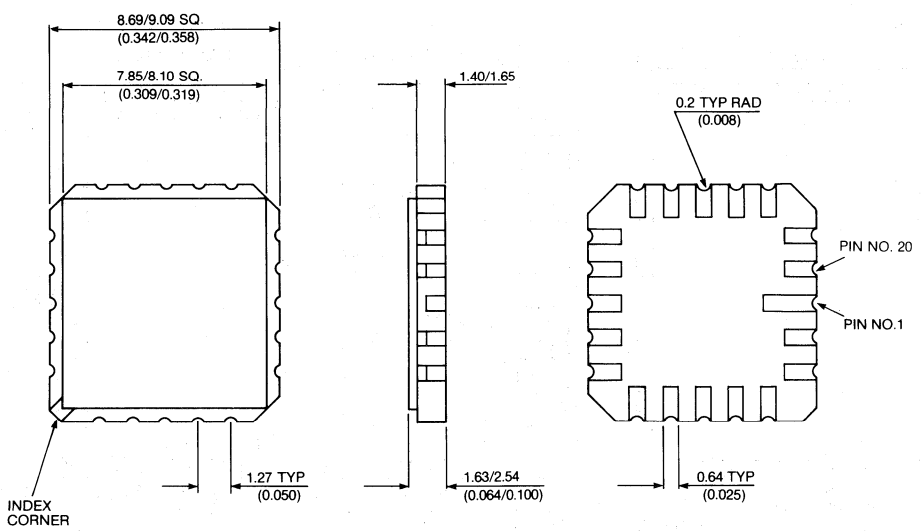
DIM.	MIN.	NOM.	MAX.
A	0.165		0.18
A_1	0.094		0.118
A_2	0.020		
b	0.013		0.021
b_1	0.026		0.032
c	0.0097		0.0103
D	1.185		1.195
D_1	1.150		1.156
D_2	0.042		0.048
E	1.185		1.195
E_1	1.150		1.156
e		0.050	
R	0.025		0.045



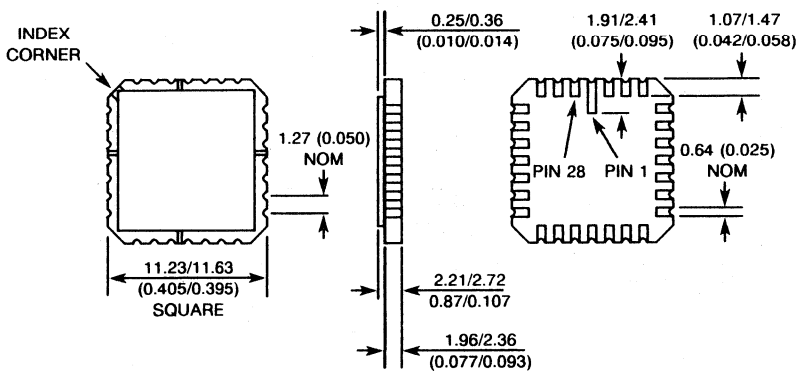
84-LEAD J- LEAD PLASTIC CARRIER - HP84



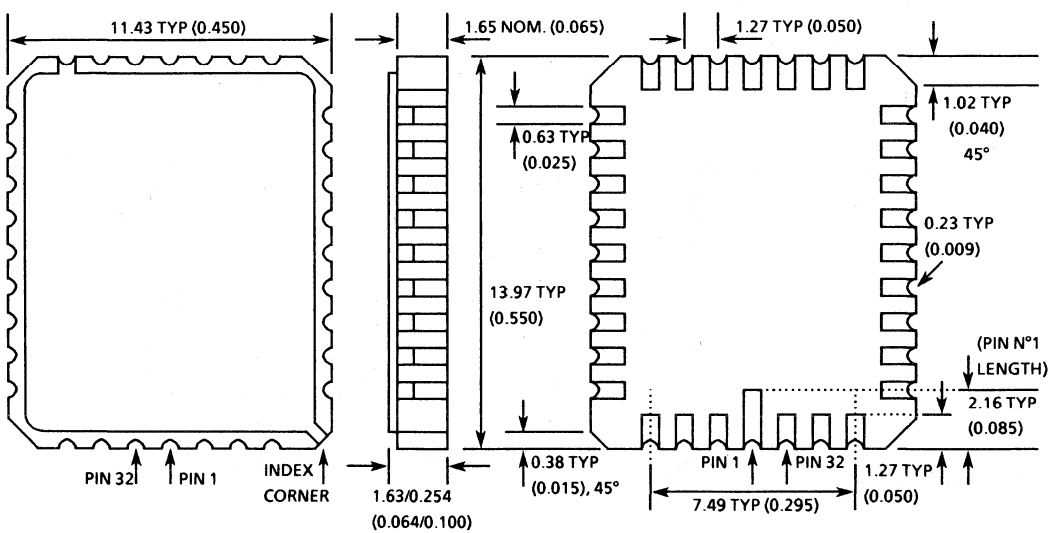
16-PIN LEADLESS CHIP CARRIER - LC16
(HERMETIC)



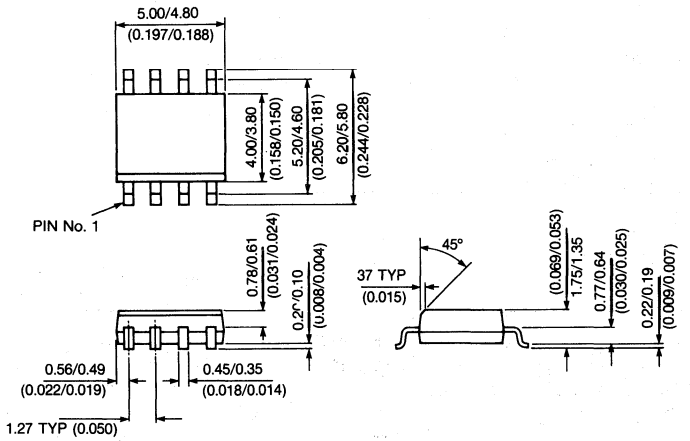
20-PIN LEADLESS CHIP CARRIER - LC20
(HERMETIC)



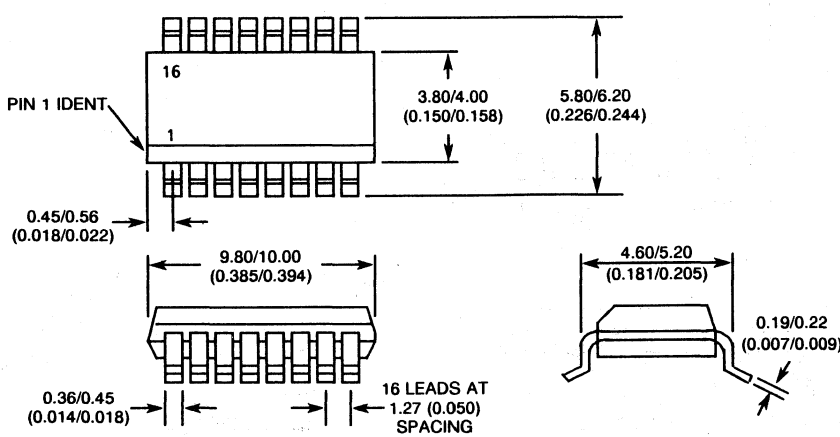
28-PIN LEADLESS CHIP CARRIER - LC28



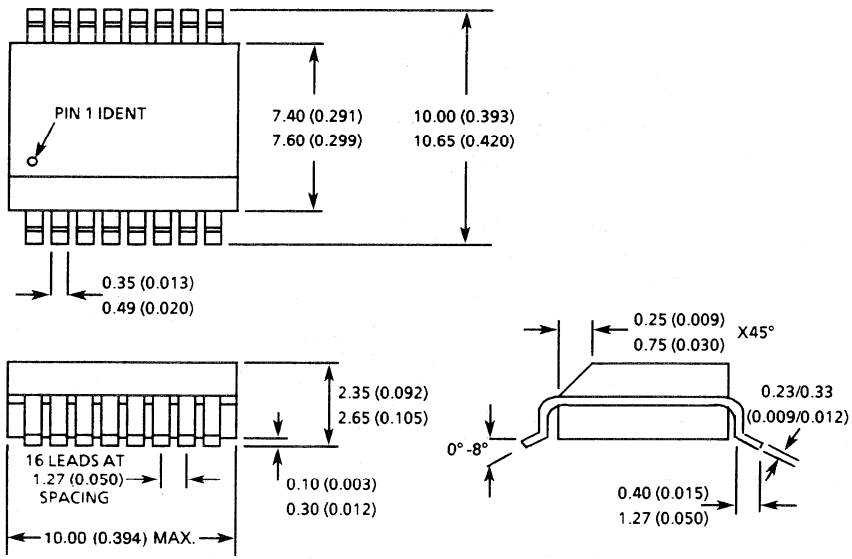
32-PIN LEADLESS CHIP CARRIER - LC32 (RECTANGULAR)



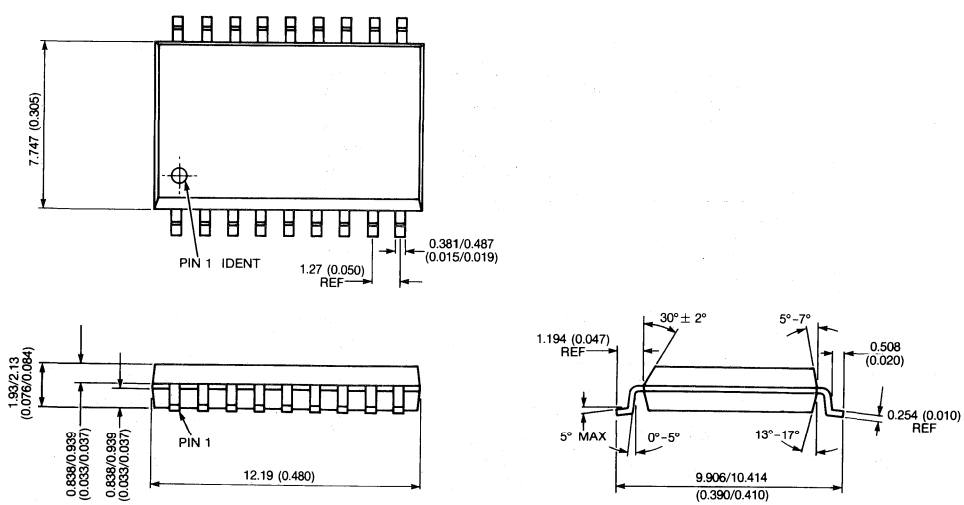
8-LEAD MINIATURE PLASTIC DIL - MP8



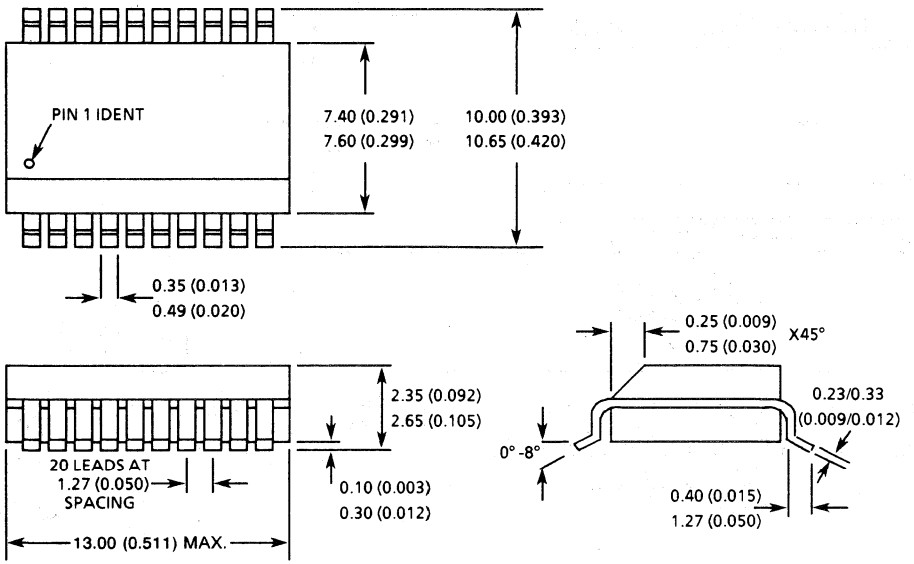
16-LEAD MINIATURE PLASTIC DIL - MP16



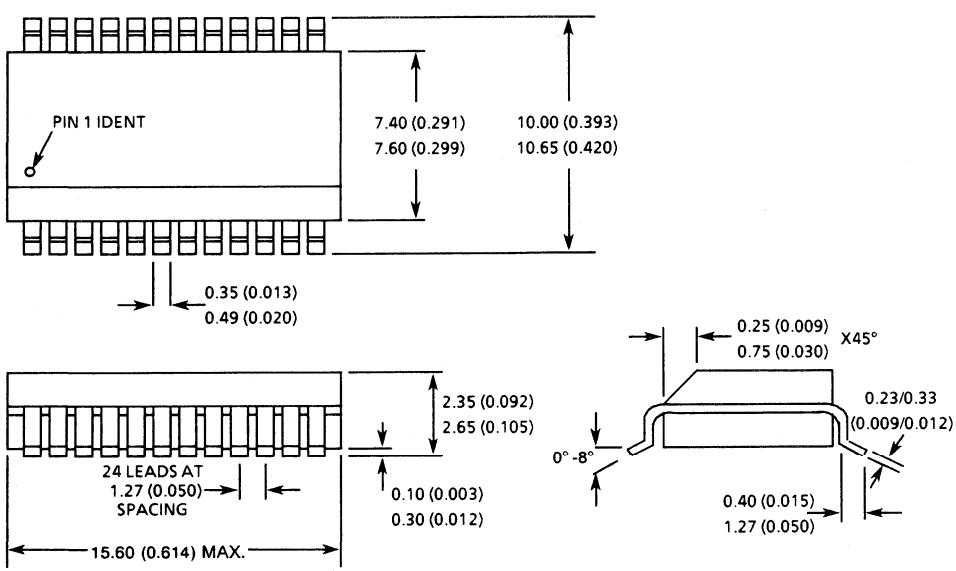
16-LEAD MINIATURE PLASTIC DIL (WIDE BODY) - MP16/W



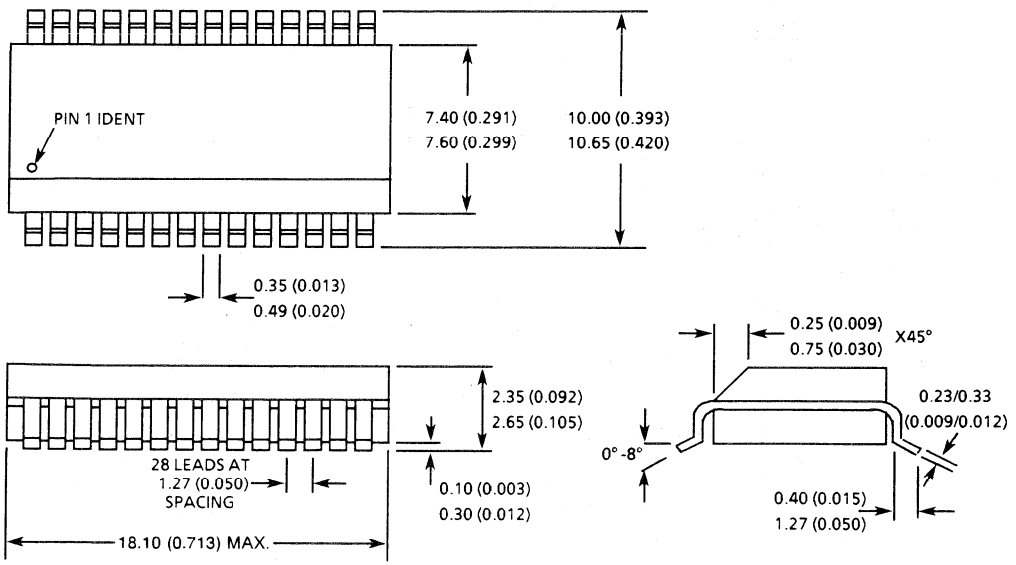
18-LEAD MINIATURE PLASTIC DIL - MP18



20-LEAD MINIATURE PLASTIC DIL (WIDE BODY) - MP20/W



24-LEAD MINIATURE PLASTIC DIL (WIDE BODY) - MP24/W



28-LEAD MINIATURE PLASTIC DIL (WIDE BODY) - MP28/W

Section 9
GPS Locations

HEADQUARTERS OPERATIONS

UNITED KINGDOM	Cheney Manor, Swindon, Wiltshire SN2 2QW, United Kingdom. Tel: (0793) 518000 Tx: 449637 Fax: 0793 518411
NORTH AMERICA	Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, USA. Tel:(408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576

CUSTOMER SERVICE CENTRES

FRANCE & BENELUX	Z.A. Courtaboeuf, Miniparc-6, Avenue des Andes, Bat. 2-BP 142, 91944, Les Ulis Cedex A. France. Tel: (1) 64 46 23 45 Fax: (1) 64 46 06 07 Tlx: 602 858 F
GERMANY, AUSTRIA and SWITZERLAND	Ungererstraße 129, 8000 Munchen 40, Germany. Tel: 089/36 0906-0. Fax: 089/360906-55 Tx: 523980
ITALY	Viale Certosa, 49 20149 Milano. Tel: (02) 33 00 10 44/45. Fax: (GR3) 31 69 04. Tlx: 331347
JAPAN	Nichiyo Building 6F, 11-12, Kanda - Mitoshirocho, Chiyoda-ku, Tokyo 101. Tel: (03) 3296-0281. Fax: (03) 3296-0228
NORTH AMERICA	**Integrated Circuits** Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, USA. Tel: (408) 438 2900 ITT Twx: 4940840 Fax: (408) 438 7023 **SOS, Microwave and Hybrid Products** 160 Smith Street. Farmingdale, NY11735, USA. Tel: (516) 293 8686 Fax: (516) 293 0061.
SOUTH EAST ASIA	152 Beach Road, #04-05 Gateway East, Singapore 0718. Tel: 2919291. Fax: 2916455
SWEDEN	Ostmästargränd 4, GS-12173 Johanneshov. Tel: 46 8 7228690 Fax: 46 8 7227879
UNITED KINGDOM and SCANDINAVIA	Unit 1,Crompton Road,Groundwell Industrial Estate, Swindon, Wilts SN2 5AY, U.K. Tel: (0793) 518510. Tx: 444410 Fax: (0793) 518582.

WORLD-WIDE AGENTS

AUSTRALIA and NEW ZEALAND	**GEC George Brown Electronics,** Unit 1, 38 South Street, Rydalmere, NSW 2116, Australia. Tel: 612 638 1888. Fax: 612 638 1798.
EASTERN EUROPE	**CTL Empexion Ltd..** Falcon House, 19 Deer Park Road, London SW19 3WX, U.K. Tel: (081) 543 0911. Tx: 928472. Fax: (081) 540 0034. **FA Bernhart GmbH,** Melkstattweg 27, PO Box 1628, D 8170 Bad Toelz., Germany. Tel: 80 41 41 676 Fax: 80 41 71 504 Tx: 526246 FABD.
HONG KONG	**YES Products Ltd.,** Block E, 15/F Golden Bear Industrial Centre, 66-82 Chaiwan Kolk Street,Tsuen Wan, N.T. Hong Kong. Tel: 4144241-6. Tx: 36590. Fax: 4136078.
INDIA	**Mekaster Telecom PVT Ltd.,** 908 Ansal Bhawan, 16 Katuba Ghandi Marg, New Delhi, 100 001 India Tel: 11 3312110 Fax: 11 3712155.
JAPAN	**Cornes & Company Ltd.,** Maruzen Building, 2-3-10 Nihonbashi, Chuo-ku. Tokyo 103. Tel: 3 272 5771. Tx: 24874. Fax: 3 271 1479. **Cornes & Company Ltd.,** 1-Chome Nishihonmachi, Nishi-Ku, Osaka 550. Tel: 6 532 1012.Tx: 525-4496. Fax: 6 541-8850. **Microtek Inc.,** Itoh Bldg, 7-9-17 Nishishinijuku. Tokyo 160. Tel: 3 371 1811. Tx: 27466. Fax: 3 369 5623.
KOREA	**KML Corporation,** 3rd Floor, Bang Bae Station Building, 981-15 Bang Bae, 3-Dong Shucho-Gu, Seoul, Korea, CPO Box 7981. Tel: 2 588 2011/6. Tx: K25981. Fax: 2 588 2017.
MALAYSIA	**Adequip Enterprise Sdn Bhd,** #6-01 6th Floor, Wisjma Stephens, 88 Jalan Raya Chulan, 50200 Kualar Lumpur, Malaysia. Tel: 2423522. Fax: 2423264.
SCANDINAVIA: Denmark	**Scansupply A/S,** 18 Nannasgade, DK-2200 Copenhagen N. Tel: 31 83 50 90. Tx: 19037. Fax: 31 83 25 40. **Scansupply A/S,** Marselisborg Havnevej 36, 8000 Arhus C. Tel: 45 86 12 77 88. Fax: 45 86 12 77 18.
Finland	**Oy Ferrado AB,** P.O.Box 54, SF-00381 Helsinki 38. Tel: 98 0550 002. Tx: 122214. Fax: 98 0551 117.
Norway	**Skandinavisk Elektronikk A/S,** Ostre Aker Vei 99, 0596 Oslo. Tel: 2 64 11 50. Tx: 71963 Fax: 2 643443.
TAIWAN	**King and King's Technology Ltd.,** 4, Alley 6, Lane 118, Sec 2, Ho Ping East Road, Taipei 106, Taiwan. Tel: (886-2) 732-6170. Fax: (886-2) 738-9146.
THAILAND	**Westech Electronics Co. Ltd,** 77/113 Moo Ban Kitikorn, Ladprao Soi 3, Ladprao Road, Ladyao, Jatujak, Bangkok 10900. Thailand. Tel: 2 5125531. Fax: 2 2365949.

WORLD-WIDE DISTRIBUTORS

AUSTRALIA **GEC George Brown Electronics,** Unit 1, 38 South Street, Rydalmere, NSW 2116, Australia.
Tel: 612 638 1888. Fax: 612 638 1798.

AUSTRIA **Moor Lackner GmbH,** Lamezanstrasse 10, A-1230 Wien Tel: 222 610620. Tx: 135701. Fax: 222 61062151.

BELGIUM **Heynen,** De Koelen 6, B-3530 Koutmalen. Tel: 011/52 57 57. Tx: 39047. Fax: 011/52 57 77.

Tekelec Airtronic NV, Bergensesteenweg 501, B-1500 Halle. Tel: 02 362 1288 Fax: 02 360 3807

FRANCE **Mateleco:**

Ile de France, 66 Avenue Augustin Dumont, 92240 Malakoff. Tel: 010 33 1 46 57 70 55. Tx: 203436.

Rhône-Alpes, 2, Rue Emile Zola, 38130 Echirolles. Tel: 010 33 76 40 38 33 Tx: 980837.

ICC:

Bordeaux, Rue de la Source, 33170 Gradignan. Tel: 56 31 17 17 Tx: 541539 Fax: 61 48 11 25.

Clermont-Ferrand, 2 bis, Avenue Fonmaure, 63400 Chamalières. Tel: 73 36 71 41 Tx: 990928.

Marseille, Z.A. Artizanord 11, 13015 Marseille. Tel: 91 03 12 12. Tx: 441313.

Toulouse, 78, Chemin Lanusse, 31200 Toulouse. Tel: 61 26 14 10. Tx: 520897.

CGE Composants SA:

Ile de France-6, Avenue Maréchal-Juin - Z.I, Grange-Dame-Rose, 92363 Meudon La Forêt.
Tel: (1) 40 94 84 00. Tx: 632253. Fax: (1) 46 30 01 29.

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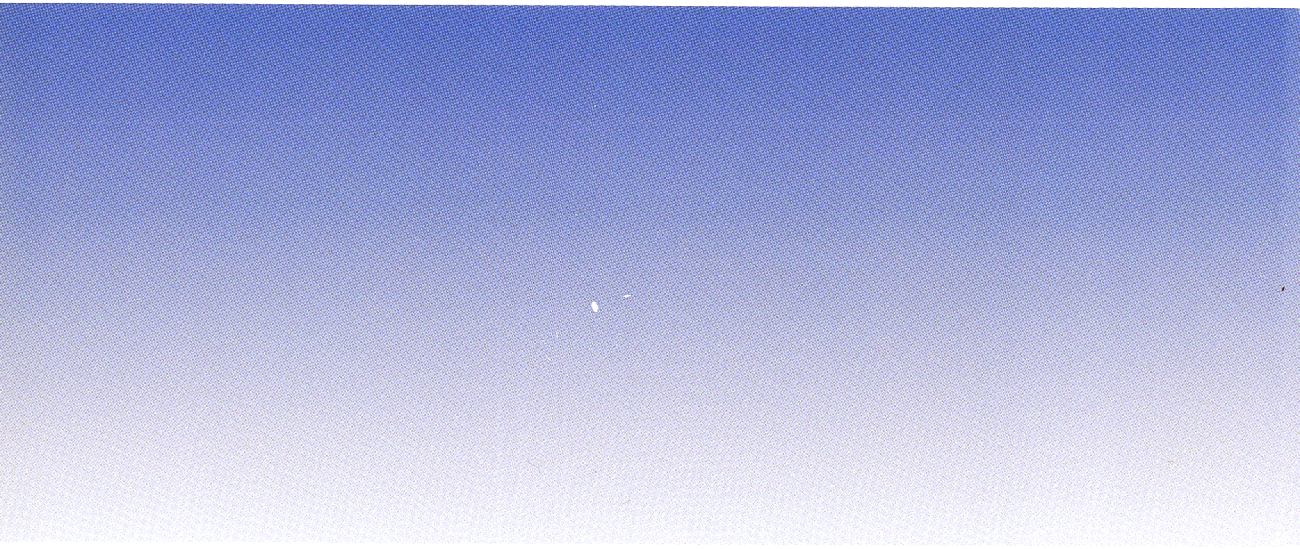

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